

High-Speed FIR Digital Filter with CSD Coefficients Implemented on FPGA

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Abstract- A very fast and low-complexity FIR digital filter on FPGA is presented. Multipliers in the filter whose coefficients are expressed as canonic signed digit (CSD) code are realized with wired-shifters, adders and subtractors. The critical path is minimized by insertion of pipeline registers and is equal to the propagation delay of an adder. The number of pipeline registers is limited by using an equivalent transformation on a signal flow graph. The price paid for the 100% speedup is 5% increase in the area. The maximum sampling frequency is 78.6MHz.

1. INTRODUCTION

In the implementation of high speed FIR digital filters, computational speed and the die area of the multiplier are the main key issues. Multipliers with CSD coefficients can be realized using wired shifters, adders and subtractors without using conventional multipliers[1]. We show an FPGA implementation example of FIR digital filters having CSD coefficients, where pipelining and other techniques are used to minimize the critical path and to reduce the die area. In this method, the critical path can be made the minimum as the delay of a single adder. Therefore, the critical path is properly shorter than [1]'s.

2. DESIGN PROCEDURE

Design of these filters is formulated as the integer programming with the FIR filter's coefficient as variables [2]. The tolerant range of desired frequency response of the filter is specified as constraints of the integer programming. Table 1 shows the specifications and the resultant filter coefficients of the design example. Figure 1 shows the frequency response and Fig.2 shows the block diagram of the designed filter.

Table 1: Specifications

# of taps : 15	$h_0, h_{14} = -1$	$h_4, h_{10} = -19$
Coefficient : 8 bit	$h_1, h_{13} = 0$	$h_5, h_9 = 0$
Nonzero digit : 3	$h_2, h_{12} = 6$	$h_6, h_8 = 78$
DC gain : 2^8	$h_3, h_{11} = 0$	$h_7 = 128$

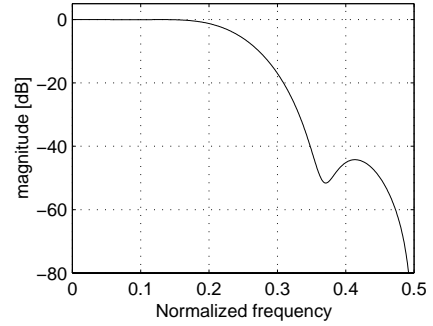


Figure 1: Design example of a half-band filter

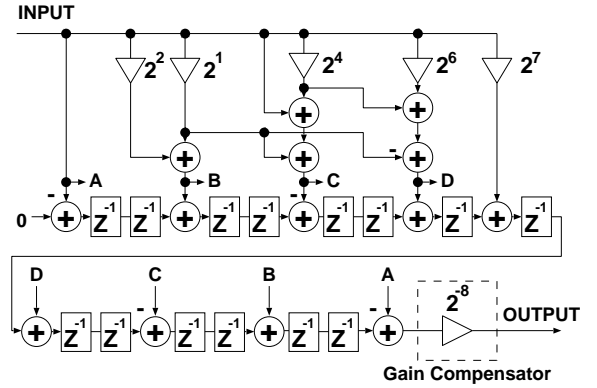


Figure 2: Block diagram of the designed FIR filter

3. FEATURE OF FPGA

FPGAs consist of large logic blocks that are configured. The logic blocks consist of a D-type flip-flop (DFF) and a configurable look-up table (LUT) which has several inputs. Figure 3(a) shows the case where the only an adder is implemented in a logic block, and Fig.3(b) shows the case where an adder and a delay element are implemented. In the latter case, a delay element is implemented by enabling the DFF which is included in the adder's logic block. Thus putting a delay element just after an adder does not increase the area at all.

The above observation shows that delay elements can be inserted between consecutive adders or subtractors as

pipeline registers to minimize the critical path of the filter without increasing the area.

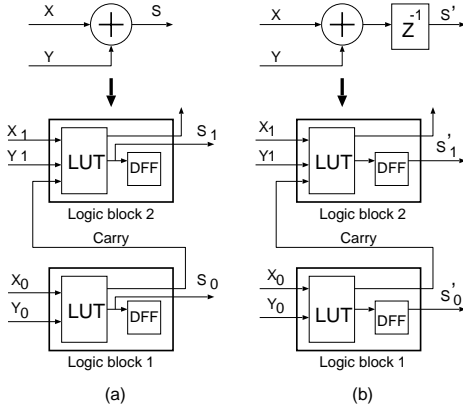


Figure 3: Implementation of an adder and an adjacent delay element in FPGAs

4. MINIMIZATION OF CRITICAL PATH

The input signal word length is specified as 12-bit in this design and the maximum internal word length is 20-bit.

First, in order to reduce the critical path, delay elements are inserted between adders which act as a part of multiplication. Suppose the propagation delay of an adder is T_a , and the number of nonzero digits of the filter coefficients is N_z . In the conventional signal flow shown in Fig.2, the length of the critical path is $N_z T_a$. After the pipeline registers are inserted, it becomes minimum of T_a , the propagation delay of a single adder. In this case, the length of the critical path decreases to 33 % as shown in Table 2.

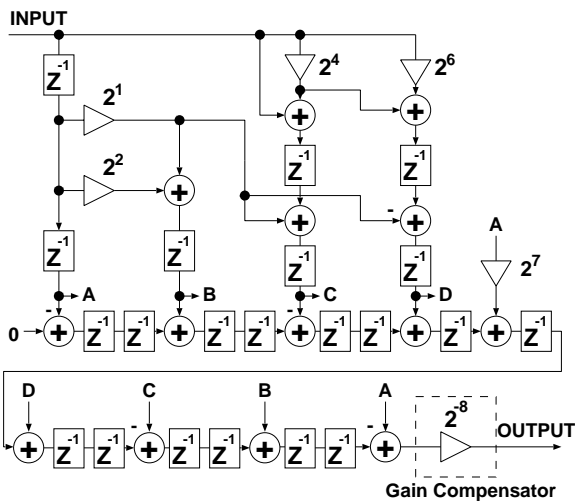


Figure 4: Designed FIR filter after pipeline register insertion and equivalent transformation from Fig.2

Second, the number of delay elements is reduced by an equivalent transformation. The order of a shifter and a delay element is reversed and the delays having the same input are unified. Figure 4 shows the resultant structure.

5. IMPLEMENTATION RESULT

The circuit of the proposed FIR filter is described by VHDL for implementation. The circuit is actually implemented on XC4028XL-1(Xilinx) using FPGA Compiler(Synopsys), and Alliance M1.4 device-fitter(Xilinx). Table 2 shows the results of the implementation.

Table 2: Implementation result for the FPGA

	Fig.2	Fig.4
Signal word length	12 bit	12 bit
# of adders	14	14 (100 %)
# of delay elements	14	21 (150 %)
Critical path length (Adder)	3	1 (33 %)
Group-delay	7	9 (129 %)
Area (Logic block)	204	215 (105 %)
Actual critical path length	25.3 ns	12.7 ns (50 %)
Sampling frequency	39.5 MHz	78.6 MHz

Minimization of the critical path increases the area to 105 %, where the area is measured by the number of logic blocks used. Although the critical path length is estimated to decrease to 33 %, the actual critical path decreases to 50 %. Thus the maximum sampling frequency is obtained as 78.6 MHz.

This FPGA device is installed onto an evaluation board with an A-D converter and a D-A converter. The observed response is the same as Fig.1 by using an analog gain-phase analyzer.

From the above, in implementation on FPGAs, the length of critical path of the FIR filter with CSD coefficients can be reduced without much increase in the area. Improvement of operating speed for FIR filters by using the proposed method is confirmed to be effective for FPGAs.

6. CONCLUSIONS

A special feature in internal structure of FPGAs is presented. With that in mind FIR digital filter structures are modified so that the length of critical path becomes minimum of a single adder. It is proved that despite delay elements are inserted into the designed FIR filter, the area increase is only a little. Therefore, high speed, compact and linear-phase FIR digital filters are obtained.

REFERENCES

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- [2] M. Yamada, A. Nishihara, "Design of FIR Digital Filters with CSD Coefficients Having Power-of-Two DC gain", Technical Report of IEICE, DSP99-145 (1999-12), pp. 99-105, Sept. 1999.