Layout Tools for Analog ICs and Mixed-Signal SoCs: A Survey

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Abstract*—*Layout for analog circuits has historically been a time-consuming, manual, trial-and-error task. The problem is not so much the size (in terms of the number of active devices) of these designs, but rather the plethora of possible circuit and device interactions: from the chip substrate, from the devices and interconnects themselves, from the chip package. In this short survey we enumerate briefly the basic problems faced by those who need to do layout for analog and mixed-signal designs, and survey the evolution of the design tools and geometric/electrical optimization algorithms that have been directed at these problems.

1 Introduction

Layout for digital integrated circuits is usually regarded as a difficult task because of the *scale* of the problem: millions of gates, kilometers of routed wires, complex delay and timing interactions. Analog designs and the analog portions of mixed-signal systems-on-chip (SoCs) are usually vastly smaller—up to 100 devices in a cell, usually less than 20,000 devices in a complete sub-system—and yet they are nothing if not *more* difficult to lay out. Why is this? The answer is that the complexity for analog circuits is not so much from the sheer number of devices, as from the complex *interactions* among the devices, among the various continuous-valued performance specifications, and with the fabrication process and the operating environment.

This would be less of a problem if analog circuits and subsystems were rare or exotic commodities, or if they were sufficiently generic that a few stable designs could be easily retargeted to each new application. Unfortunately, neither is true. The markets for application-specific ICs (ASICs), application-specific standard parts (ASSPs) and high-volume commodity ICs are characterized by an increasing level of integration. In recent years, complete systems that before occupied separate chips are being integrated on a single chip. Examples of such "systems on a chip" include telecommunications ICs such as modems, wireless designs such as components in radio frequency receivers and transmitters, and networking interfaces such as local area network ICs. Although most functions in such integrated systems are implemented with digital (or especially digital signal processing) circuitry, the analog circuits needed at the interface between the electronic system and the "real" world are now being integrated on the same die for reasons of cost and performance.

The booming market share of mixed-signal ASICs in complex systems for telecommunications, consumer, computing, and automotive applications is one direct result of this. But along with this increase in achievable complexity has come a significant increase in design complexity. And at the same time, many present ASIC application markets are characterized by shortening product life cycles and time-to-market constraints. This has put severe pressure on the designers of these analog circuits, and especially on those who lay out these designs. If cell-based library methodologies were workable for analog (as they are for semi-custom digital designs) layout issues would be greatly mitigated. Unfortunately, such methodologies fare poorly here. Most analog circuits are one-of-a-kind, or at best few-of-a-kind on any given IC. Today, they are usually designed by hand, and laid out by hand. The problem recurs at the system level: the discipline of row-based layout as the basis for large function blocks that is so successful in digital designs is not (yet) as rigorously applied in analog designs.

Despite the problems here, there is a thriving research community working to make custom analog layout tools a practical reality. This brief survey attempts to describe the history and evolution of these tools; it extends two earlier reviews [1,2]. Our survey is organized as follows. We begin with a brief taxonomy of problems and strategies for analog layout in Sec 2. Then, in Sec. 3 we review attacks on the cell-level layout problem. In Sec. 4 we review mixed-signal system-level layout problems. In Sec. 5 we review recent work on field programmable analog arrays. Sec. 6 offers some concluding remarks. We end with an extensive, annotated bibliography.

2 Analog Layout Problems and Approaches

Before trying to categorize the various geometric strategies that have been proposed for analog layout, it is essential first to understand what are the electrical problems that affect analog design. We enumerate here briefly the salient effects that layout can have on circuit performance. References Cohn [35], Verghese [76], and Stanisic [101] together comprise a fairly complete treatment of these issues. There are really three core problems, which we describe first below. We then briefly survey solution strategies here.

2.1 Loading problems

The non-ideal nature of inter-device wiring introduces capacitive and resistive effects which can degrade circuit performance. At sufficiently high frequencies, inductive effects arise as well. There are also parasitic RLC elements associated with the geometry of the devices themselves, e.g., the various capacitances associated with MOS diffusions. All these effects are remarkably sensitive to detailed (polygon-level) layout For example, in MOS circuits, layout designers have a useful degree of freedom in that they can fold large devices (i.e., devices with large width-to-length ratios), thus altering both their overall geometric shape and detailed parasitics. Folding transforms a large device (large channel width) into a parallel connection of smaller devices. The smaller devices are *merged*: parallel side-by-side alignment allows a single source or drain diffusion to be shared between adjacent gate regions, thus minimizing overall capacitance. Every diffused structure also has an associated parasitic resistance which varies with its shape. These resistances can be reduced by minimizing the aspect ratio of all dif-

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fusions (reducing the width of the device), merging diffusions when possible, and strapping diffusion with low resistance layers such as metal where possible. Of course, this "strapping" may interfere with signal routing. Cohn [35] offers a careful treatment of the layout issues here for MOS devices.

One of the distinguishing characteristics of analog layout, in comparison to digital layout, is the amount of effort needed to create correct layouts for atomic devices. MOS devices with large width-to-length rations, bipolar devices with large emitter areas, etc., are common in analog designs and require careful attention to detail. Passive components that implement resistors or capacitors or inductors are also more frequent in analog design, and require careful layout. (See, for example, Bruce [15] as an example of procedural generation of complex MOS devices.) Extremely low-level geometric details of the layout of individual devices and passives can have a significant circuit-level impact.

2.2 Coupling problems

Layout can also introduce unexpected signal coupling into a circuit which may inject unwanted electrical noise or even destroy its stability through unintended feedback. At lower frequencies, coupling may be introduced by a combination of capacitive, resistive, or thermal effects. At higher frequencies inductive coupling becomes an issue. Especially in the modern deep submicron digital processes in which analog systems are being integrated, coupling is an increasing problem. Metal conductors couple capacitively when two metal surfaces are sufficiently close, e.g., if wires run in parallel on a single layer or cross on adjacent layers. If a parallel run between incompatible signals is unavoidable, a neutral wire such as a ground or reference line can be placed between them as a coupling shield.

Current flowing through a conductor also gives rise to a fluctuation in the voltage drop across the conductor's finite resistance. This fluctuation is then coupled into all devices attached to the conductor. This effect is particularly problematic in power supply routing for analog cells on digital ICs. Sensitive analog performance often depends on an assumption of moderate stability in the power rails--this may not be true if the power distribution network is improperly laid out. See Stanisic [99, 100, 101] for a detailed treatment of the issues in mixed-signal power distribution.

Signals can also be coupled through the silicon substrate or bulk, either through capacitive, resistive, or thermal effects. Because all devices share the same substrate, noise injected into the substrate is capacitively or resistively coupled into every node of the circuit. This is particularly problematic when analog circuits must share a substrate with inherently noisy high speed digital logic. On mixed-signal ICs conventional solutions focus on *isolation*: either by locating the sensitive analog far away from the noise-injecting source, or surrounding the noise-sensitive circuits with a low impedance diffusion guard-ring to reduce the substrate noise level in a particular area. Unfortunately, the structure of the substrate and details of the layout of the power supply network that biases the substrate greatly affect even the qualitative behavior of this coupling. For example, epitaxial substrates have such low resistivity that injected noise can "reappear" far from its origin on the chip surface; simple isolation schemes do not always work well here. Bulk substrates are somewhat more resistive and noise may remain more local. Evolving silicon-on-insulator processes (SOI) may dramatically reduce this problem, but these are not yet in widespread use for commodity mixed-signal designs. References [68, 85, 100] are a good starting point for analysis of the substrate coupling problem in mixed-signal design.

In addition, since silicon is an excellent conductor of heat, local temperature variations due to current changes in a device can also cause signal coupling in nearby thermally sensitive devices. This phenomenon is most prevalent in Bipolar or Bi-CMOS processes. Placing thermally sensitive devices far away from high-power thermally dissipating devices can reduce this effect. Placing matching devices symmetrically about thermally "noisy" sources can also be effective in reducing the effects of thermal coupling.

2.3 Matching problems

Unavoidable variations which are present in all fabrication processes lead to small mismatches in electrical characteristics of identical devices. If these mismatches are large enough, they can effect circuit performance by introducing electrical problems such as offsets. Four major layout factors can affect the matching of identical devices: *area*, *shape*, *orientation*, and *separation*.

Device area is a factor because semiconductor processing introduces unavoidable distortions in the geometry which make up devices. Creating devices using identical geometry (identical shape) improves matching by insuring that both devices are subject to the same (or at least *similar*) geometric distortions. Similarly, since the proportional effect of these variations tends to decrease as the size of the device increases, matching devices are usually made as large as the circuit performance and area constraints will allow. Since many processing effects, *e.g.*, ion-implantation, introduce anisotropic geometric differences, devices which must match should also be placed in the same orientation. Finally, spatial variations in process parameters tend to degrade the matching characteristics of devices as their separation increases. This is largely due to process induced gradients in parameters such as mobility or oxide thickness. Sensitivity to these effects can be reduced by placing devices which must match well in close proximity. Devices which must be *extremely* well matched may be spatially interdigitated in an attempt to cancel out the effects of global process gradients.

Device matching, particularly of bipolar devices, may also be degraded by thermal gradients. Two identical devices at different points on a thermal gradient will have slight differences in VBE for a given collector current. To combat this, it is common practice to arrange thermally sensitive matching devices symmetrically around thermally generating noise sources. Parasitic capacitive and resistive components of interconnect can also introduce problems of matching in differential circuits, i.e., those circuits which are comprised of two matching halves. A mismatch in the parasitic capacitance and resistance between the two matching halves of the circuit can give rise to offsets and other electrical problems. The most powerful technique used to improve interconnect parasitic matching is layout symmetry, in which the placement and wiring of matching circuits are forced to be identical, or in the case of differential circuits, mirror symmetric.

2.4 Layout solution strategies

We mentioned a variety of solution techniques in the above enumeration of layout problems: careful attention to atomic device layout, MOS merging, substrate noise isolation, symmetric layout, etc. However, these are really low-level *tactics* for dealing with specific problems for specific circuits in specific operating or fabrication environments. The more general question we wish to address next is how the analog portion of a large mixed-signal IC is laid out—what are the overall geometric *strategies* here?

We note first that, like digital designs, analog designs are attacked hierarchically. However, analog systems are usually significantly smaller than their digital counterparts: 10,000 to 20,000 analog devices versus 100,000 to 1,000,000 digital gates. Thus, analog layout hierarchies are usually not as deep as their digital counter-

parts. The need for low-level attention to coupling and interaction issues is another force that tends to flatten these hierarchies. The typical analog layout hierarchy comprises two fundamentally different types of layout tasks:

- **Cell-level layout:** The focus here is really device-level layout, placement and routing of individual active and passive devices. At this level, many of the low level matching, symmetry, merging, reshaping, and proximity-management tactics for polygon-level optimization are applied. The goal is to create cells that are suitably insulated not only from fluctuations in fabrication and operating environment, but from probable coupling with neighboring pieces of layout.
- **System-level layout:** The focus here is cell composition, arranging and interconnecting the individual cells to complete an analog subsystem. At this level, isolation is one major concern: from nearby noisy digital circuits coupled in via substrate, power grid, or package, The other concern is signal integrity. Some number of digital signals from neighboring digital blocks need to penetrate into any analog regions, and these signals may be fundamentally incompatible with some sensitive analog signals.
- **Programmable layout:** The focus here is applying field programmable gate array (FPGA, see for example, Rose [114]) ideas to analog designs. The idea is to bypass completely the need to do custom cells. Rather, a set of programmable active and passive elements is connected with programmable wiring to achieve low-performance analog functions. This is a relatively recent implementation strategy, but we expect to see it grow.

We visit the ideas behind each of these layout strategies in the following three sections.

3 Analog Cell Layout Strategies

For our purposes a "cell" is a small analog circuit, usually comprising not more than about 100 active and passive devices which is designed and laid out as a single atomic unit. Common examples include operational amplifiers, comparators, voltage references, analog switches, oscillators, and mixers.

The earliest approaches to custom analog cell layout relied on procedural module generation. These approaches are a workable strategy when the analog cells to be laid out are relatively static, *i.e.*, necessary changes in device sizing or biasing result in little need for global alterations in device layout, orientation, reshaping, *etc.* Procedural generation schemes usually start with a basic geometric template (sometimes called a *topology* for the circuit), which specifies all necessary device-to-device and device-to-wiring spatial relationships. Generation completes the template by correctly sizing the devices and wires, respacing them as necessary. References [6-11] are examples dedicated mainly to opamps. The mechanics for capturing the basic design specifications can often be as familiar as a common spreadsheet interface, e.g., [12]. Owen [12] is a more recent example focused on opamp generation, and describes both a language for specifying these layouts and several optimized layout results. The system at Philips [13] is another good example of practical application of these ideas on complex circuits. Bruce [15] shows an example of module generation useful for atomic MOS devices.

Often, however, changes in circuit design require full custom layout, which can be handled with a *macrocell-style* strategy. The terminology is borrowed from digital floorplanning algorithms, which manipulate flexible layout blocks, arrange them topologically, and then route them. For analog cells, we regard the flexible blocks as devices to be reshaped and reoriented as necessary. Module generation techniques are used to generate the layouts of the individual devices. A placer then arranges these devices, and a router interconnects them—all while attending to the numerous parasitics and couplings to which analog circuits are sensitive.

The earliest techniques used a mixed of knowledge-based and constructive techniques for placement, with routers usually adapted from common semicustom digital applications [18,20,21,24]. For example, a common constructive placement heuristic is to use the spatial relationships in a drawn circuit schematic as an initial basis from mask-level device placement [23]. Unfortunately, these techniques tended to be rather narrow in terms of which circuits could be laid out effectively.

The ILAC tool from CSEM was an important early attempt in this style [17,22]. It borrowed heavily from the best ideas from digital layout: efficient slicing tree floorplanning with flexible blocks, global routing via maze routing, detailed routing via channel routing, area optimization by compaction. The problem with the approach was that it was difficult to extend these primarily-digital algorithms to handle all the low-level geometric optimizations that characterize expert manual design. Instead, ILAC relied on a large, very sophisticated library of device generators.

ANAGRAM and its successor KOAN / ANAGRAM II from CMU kept the macrocell style, but reinvented the necessary algorithms from the bottom up, incorporating many manual design optimizations [19,25,27,35]. For example, the device placer KOAN relied on a very small library of device generators, and migrated important layout optimizations into the placer itself. KOAN could dynamically fold, merge and abut MOS devices, and thus discover desirable optimizations to minimize parasitic capacitance during placement. KOAN was based on an efficient simulated annealing algorithm [3]. (Recent placers have also extended ideas from sequence-pair module-packing representations [5] to handle analog layout tasks [38].) KOAN's companion, ANAGRAM II, was a maze-style detailed area router capable of supporting several forms of symmetric differential routing, mechanisms for tagging compatible and incompatible classes of wires (*e.g.*, noisy and sensitive wires), parasitic crosstalk avoidance, and over-the-device routing. Other device placers and routers operating in the *macrocell-style* have appeared (e.g., [26, 31, 32, 33, 34]), confirming its utility.

In the next generation of cell-level tools, the focus shifted to quantitative optimization of performance goals. For example, KOAN maximized MOS drain-source merging during layout, and ANAGRAM II minimized crosstalk, but without any specific, quantitative performance targets. The routers ROAD [29] and ANAGRAM III [30] use improved cost-based schemes that route instead to minimize the deviation from acceptable parasitic bounds derived from designers or sensitivity analysis. The router in [39] can manage not just parasitic sensitivities, but also basic yield and testability concerns. Similarly, the placers in [28, 36, 37] augment a KOAN-style model with sensitivity analysis so that performance degradations due to layout parasitics can be accurately controlled. Other tools in this style include [40].

In the newest generation of CMOS analog cell research, the device placement task has been separated into two distinct phases: device *stacking*, followed by *stack placement*. By rendering the circuit as an appropriate graph of connected drains and sources, it is possible to identify natural clusters of MOS devices that ought to be merged—called *stacks*—to minimize parasitic capacitance. Malavasi [43, 44, 47] gave an exact algorithm to extract all the optimal stacks, and the placer in [45, 46] extends a KOAN-style algorithm to dynamically choose the right stacking and the right placement of

each stack. Basaran [48] offers another variant of this idea: instead of extracting all the stacks (which can be time-consuming since the underlying algorithm is exponential), this technique extracts one optimal set of stacks very fast (in linear time). The technique is useful in either the inner loop of a layout algorithm (to evaluate quickly a merging opportunity) or in an interactive layout editor (to stack a set of devices optimally, quickly).

The notion of using sensitivity analysis to quantify the impact on final circuit performance of low-level layout decisions (*e.g.*, device merging, symmetric placement / routing, parasitic coupling due to specific proximities, *etc.*) has emerged as a strategy to link the various approaches being taken for cell level layout and system assembly. Several systems from U.C. Berkeley are notable here. The influential early formulation of the sensitivity analysis problem was Choudhury [59] which not only quantified layout impacts on circuit performance, but also showed how to use nonlinear programming techniques to map these sensitivities into constraints on various portions of the layout task. Charbon [61] extended these ideas to handle constraints involving nondeterminiistic parasitics of the type that arise from statistical fluctuations in the fabrication process. In related work, Charbon [60] also showed how to extract critical constraints on symmetry and matching directly from a device schematic.

One final problem in the macrocell style is the separation of the placement and routing steps. In manual cell layout, there is no effective difference between a rectangle representing a wire and one representing part of a device: they can each be manipulated simultaneously. In a place-then-route strategy, one problem is estimating how much space to leave around each device for the wires. One solution strategy is *analog compaction, e.g.*, [49,51,52], in which we leave extra space during device placement and then compact. A more radical alternative is *simultaneous device place-and-route.* An experimental version of KOAN [61] supported this by iteratively perturbing both the wires and the devices, with the goal of optimally planning polygon-level device and wire layout interactions.

As wireless and mobile design has proliferated, more radio frequency designs have appeared. These offer yet another set of challenges at the cell level. Radio frequency (RF) circuits and higher frequency microwave circuit have unique properties which make their automated layout impossible with the techniques developed for lower frequency analog cells. Because every geometric property of the layout of an individual wire—its length, bends, proximity to other wires or devices—may play a key role in the electrical performance of the overall circuit, most RF layouts are optimized for performance first and density second.

Most layout work targeting RF circuits comprises interactive tools that aid the designer to speed manual design iterations [54, 55]. Other work in the area includes semi-automated approaches that rely on knowledge of the relative position of all cells [53]. However, these template-based approaches with predefined cells do limit the design alternatives possible. Recently, Charbon introduced a performance-driven router for RF circuits [56]. In their approach, sensitivity analysis is employed to compute upper bounds for critical parasitics in the circuit, which the router then attempts to respect. Aktuna [57,58] recently introduced the idea of device-level floorplanning for these circuits; using a genetic algorithm, the tool simultaneously evolves placement and detailed routing under constraints on length, bends, phase, proximity and planarity.

There are several open problems in cell-level layout. For example, the optimal way to couple the various phases of cell layout—stacking, placement, routing, compaction—to each other and back to circuit design (or redesign) remains a challenging problem. However, there is a maturing base of workable transistor-level layout techniques now to build on. We note that commercial tools offering device-level analog layout synthesis have just recently appeared, and are in now in production use. Figure 1, an industrial analog cell produced by a commercial analog layout synthesis tool, is one such automatic layout example [41,42].

4 Mixed-Signal System Layout

A mixed-signal *system* is a set of custom analog and digital functional blocks. At the system-level the problem is really an *assembly* problem [2]. Assembly means block floorplanning, placement, global and detailed routing (including the power grid). As well as parasitic sensitivities, the two new problem at the chip level are *coupling* between noisy signals and sensitive analog signals, and *isolation* fro digital switching noise that couples through the substrate, power grid, or package.

Just as at the cell level, procedural generation remains a viable alternative for well-understood designs with substantial regularity. Many signal processing applications have the necessary highly stylized, regular layout structure. Procedural generation has been successful for many switched capacitor filters and data converters [13,62-66], and especially regular, array-style blocks [16].

More generally though, work has focussed on custom placement and routing at the block level, with layout optimization aimed at not only area, but also signal coupling and isolation. Trnka [89] offered one very early attempt aimed at bipolar array-style (i.e., fixed device image) layout, adapting semicustom digital layout tools to this analog layout image. For row-based analog standard cell layout, an early elegant solution to the coupling problem was the *segregated channels* idea of [86,87] to alternate noisy digital and sensitive analog wiring channels in a row-based cell layout. The strategy constrains digital and analog signals never to be in the same channel, and remains a practical solution when the size of the layout is not too large. However, in modern multi-level interconnect technologies, this rigorous segregation can be overly expensive in area.

For large designs, analog channel routers were developed. In Gyurscik [90], it was observed that a well-known digital channel routing algorithm [88] could be easily extended to handle critical analog problems that involve varying wire widths and wire separations needed to isolate interacting signals. Work at Berkeley substantially extended this strategy to handle complex analog symmetries, and the insertion of shields between incompatible signals

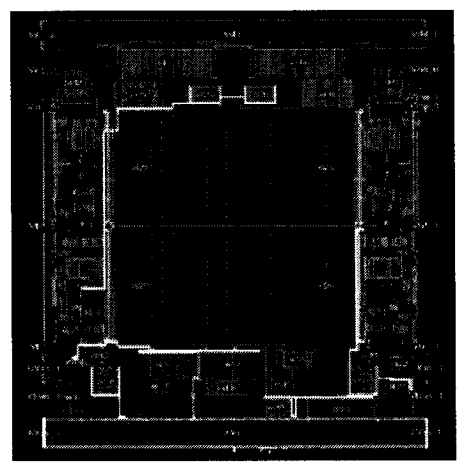

Figure 1. Bootstrapped fully differential amplifier in 0.25um CMOS process. (Courtesy Rocketchips, and NeoLinear, Inc.)

[91,92,94]. This work also introduced the idea of *constraint mapping*, which begins with parasitic sensitivities available from analysis of the system (or the cell) to be laid out, and transforms these into hard bounds on the allowable parasitics of each wire in each channel. The mapping process is itself a nonlinear programming problem, in this case a quadratic programming formulation. These tools are particularly effective for stylized row-based layouts such as switched capacitor filters, where complex routing symmetries are necessary to balance subtle parasitics, and adjoint simulation methods can yield the necessary sensitivities.

The WREN [93] and WRIGHT [95,96] systems from CMU generalized these ideas to the case of arbitrary layouts of mixed functional blocks. WREN comprises both a mixed-signal global router and channel router. WREN introduced the notion of *SNR-style* (signal-to-noise ratio) constraints for incompatible signals, and both the global and detailed routers strive to comply with designer-specified noise rejection limits on critical signals. WREN incorporates a constraint mapper (influenced by [59]) that transforms input noise rejection constraints from the across-the-whole-chip form used by the global router into the per-channel per-segment form necessary for the channel router (as in [94]). WRIGHT uses a KOAN-style annealer to floorplan the blocks, but with a fast substrate noise coupling evaluator so that a simplified view of substrate noise influences the floorplan. WRIGHT used a coarse resistive mesh model with numerical pruning to capture substrate coupling; the approach in Charbon [83] uses semi-analytical substrate modeling techniques which allow fast update when blocks move, and can also support efficient noise sensitivity analysis.

The substrate coupling problem is an increasingly difficult one as more and faster digital logic is placed side-by-side with sensitive analog parts. One avenue of relevant work here seeks to model the substrate accurately, efficiently extract tractable electrical models of its conduction of overall chip noise, and understand qualitatively how various isolation mechanisms (e.g., separation, guard rings) will work. This has been an active area of late. References [67,69-71,73-80] address basic computational electromagnetics attacks on modeling and analysis of substrate coupling. The approaches vary in their discretization of the substrate, their numerical technique to solve for the point-to-point resistance between two devices in the substrate, and their model-order reduction techniques to reduce potentially large, extracted circuit-level substrate models to smaller, more efficient circuit models. Su [68] offers experimental data from test circuits on the mechanisms of substrate noise conduction for CMOS mixed-signal designs in epitaxial substrates. Charbon and Miliozzi [82,83] address substrate coupling in the context of linking substrate modeling with the generation of constraints on allowable noise in the synthesis and layout process. Mitra [72] and Miliozzi [81] address the problem of estimating substrate current injection; Mitra [72] uses a circuit-level switching model and circuit simulation, and transforms simulation results into an equivalent single-tone sinusoid with the same total energy as the original random switching waveform. Miliozzi [81] uses a digital simulator to capture simple digital switching waveforms, which are then combined with precharacterized circuit-level injection models to estimate block-level injection. Tsukada [84] suggests an active guard ring structure to mitigate substrate noise, based on some of these modeling ideas. Verghese [85] offers a recent survey of substrate modeling, extraction, reduction, and injection work, along with a review of how substrate issues are dealt with in current mixed-signal design methodologies

Another important task in mixed-signal system layout is power grid design. Digital power grid layout schemes usually focus on connectivity, pad-to-pin ohmic drop, and electromigration effects. But these are only a small subset of the problems in high-performance mixed-signal chips which feature fast-switching digital systems next to sensitive analog parts. The need to mitigate unwanted substrate interactions, the need to handle arbitrary (non-tree) grid topologies, and the need to design for transient effects such as current spikes are serious problems in mixed-signal power grids. The RAIL system [97-101] addresses these concerns by casting mixed-signal power grid synthesis as a routing problem that uses fast AWE-based [4] linear system evaluation to electrically model the entire power grid, package and substrate during layout. By allowing changes in both grid topology (where segments are located, where power pins are located, where substrate contacts are located) and grid segment sizing, the tool can find power grid layouts to optimize ac, dc, and transient noise constraints. Techniques such as [72, 81] are useful to estimate the digital switching currents needed here for power grid optimization. Chen [102] discusses a similar power distribution formulation applied to digital circuits.

Most of these system layout tools are fairly recent, but because they often rely on mature core algorithms from similar digital layout problems, many have been prototyped both successfully and quickly. Several full, top-to-bottom prototypes have recently emerged, *e.g.,* [83, 103-106].

There are many open problems here. Signal coupling and substrate/package isolation are still addressed via rather *ad hoc* means overall. There is still much work to be done to enhance existing constraint mapping strategies and constraint-based layout tools to handle the full range of industrial concerns, and to be practical for practicing designers.

5 Field-programmable analog arrays

We mention finally one very recent analog layout style which is radically different from those mentioned above. In the digital realm, field programmable gate arrays (FPGAs) have revolutionized digital prototyping and rapid time-to-market designs [114]. Integrating programmable logic elements and programmable interconnect, these allow rapid customization with no fabrication steps. An obvious question is: can a similar technology be adapted for analog and mixed-signal designs. The apparent answer is a qualified "yes".

Early work such as [107-109] mimicked directly the FPGA style of small primitive functions connectable by programmable interconnect. However, the loading which is already problematic in digital designs proved even more deleterious here. Later designs such as [110-113] moved up to higher-level buildinng blocks (e.g., opamps, switches, capacitor arrays) and also focussed new energy on sensitive analog design of the programmable interconnect. Field programmable analog arrays (FPAAs) are just now beginning to be commercially available. They are currently so small, however, that layout is not really a problem. It will be interesting to see if these designs become larger (e.g., larger digital blocks with smaller analog blocks), and if so, if automatic layout becomes a requirement.

6 Conclusions

There has been substantial progress on tools for custom analog and mixed-signal circuit layout. Cast mostly in the form of numerical and combinatorial optimization tasks, linked by various forms of sensitivity analysis and constraint mapping, leveraged by ever faster workstations, these tools are beginning to have practical--even commercial--application. There remain many open problems here, and some newly created problems as analog circuits are increasingly embedded in unfriendly digital deep submicron designs. Given the demand for mixed-signal ICs, we expect no diminishment in the interest in various layout tools to speed the design of these important circuits.

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For clarity here, we have grouped the references by topic, in roughly the order in which each topic area is visited in our review.

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