Energy-Efficient 32 x 32-bit Multiplier in Tunable Near-Zero Threshold CMOS

Vjekoslav Svilan
Dept. Electrical Engineering
Stanford University
350 Serra Mall
Stanford, CA 94305-9515
vsvilan@stanford.edu

Masataka Matsui
System ULSI Engineering Lab
Toshiba Corporation
580-1 Horikawa-cho,
Saiwai-ku
Kawasaki, 210-8520, Japan
masataka.matsui@toshiba.co.jp

James B. Burr
Sun Microsystems
Laboratories
2600 Casey Avenue, Bldg. 29
Mountain View, CA 94043
jim.burr@eng.sun.com

ABSTRACT

An 80,000 transistor, low swing, 32 x 32-bit multiplier was fabricated in a standard 0.35 μm, V_{th}=0.5 V CMOS process and in a 0.35 μm, back-bias tunable, near-zero V_{th} process. While standard CMOS at V_{dd}=3.3 V runs at 136 MHz, the same performance can be achieved in the low-V_{th} version at V_{dd}=1.3 V, resulting in more than 5 times lower power. Similar power reductions are obtained for frequencies down to 10 MHz. In addition, the low-V_{th} version is able to run at 188 MHz, which is 38% faster than standard CMOS.

1. INTRODUCTION

An increasing number of applications, especially portable ones, are becoming limited by power, rather than performance. Reducing supply voltage [1, 2] or signal swing [3] have been shown effective in reducing power. However, to maintain performance with lower supply voltage, the transistor threshold voltage (V_{th}) also needs to be lowered [4], resulting in increased leakage power.

In this work we used near-zero threshold V_{th} devices, combined with variable threshold CMOS (VTCMOS) techniques [5, 6] to achieve the ratio of dynamic and static power which minimizes total power. Unlike standard CMOS where leakage power is usually a negligible portion of the total power, we show that the leakage power should be a significant portion of the total power if one is to achieve minimum energy per operation.

2. CIRCUITS AND TECHNOLOGY

A 32 x 32-bit signed integer multiplier [7] (Figure 1) designed using dynamic, low-swing differential circuit techniques has been used to demonstrate the advantages of tunable, near-zero threshold CMOS technology over standard CMOS. It

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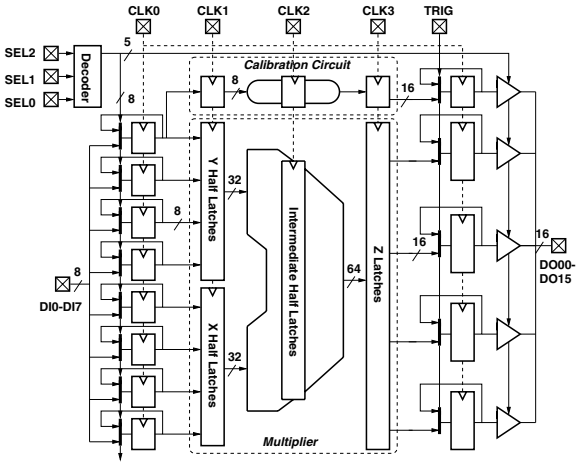

Figure 1: Multiplier block diagram

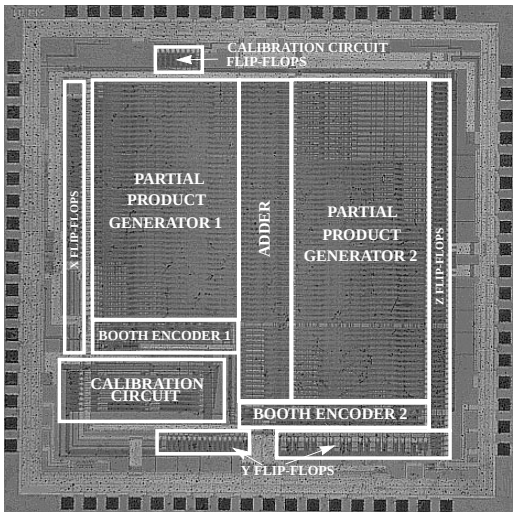

Figure 2: Chip micrograph

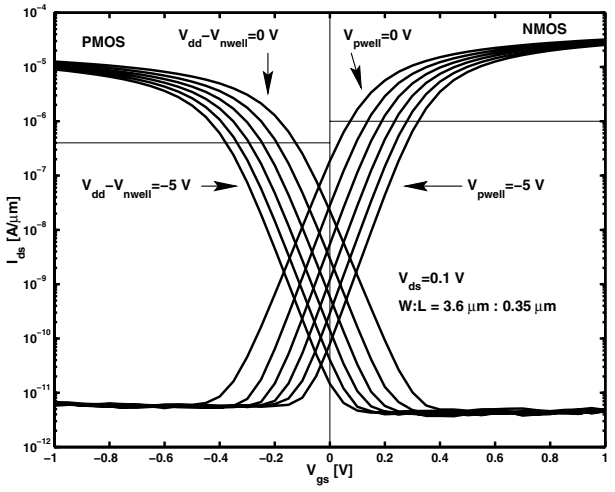

Figure 3: 3.6 μm : 0.35 μm NMOS and PMOS low-V_{th} transistor I-V curves showing large threshold tunability

uses 4-bit Booth encoding and tree reduction by a 4-2 adder. It was fabricated both in a 0.35 μm standard CMOS technology, and in a 0.35 μm low-threshold process. It occupies 3.1 x 3.1 mm area and contains about 80,000 transistors (Figure 2).

Figure 3 shows I_{ds} vs. V_{gs} transistor characteristics of a 3.6 μm : 0.35 μm PMOS and NMOS device for back-bias (V_{dd}-V_{nwell}, V_{pwell}) voltages ranging from 0 to −5 V. It demonstrates a wide range of threshold tunability which can be used to balance static and dynamic power over wide frequency range, circuit activity and effective logic depth.

3. RESULTS

Figure 4 shows a Shmoo plot of the low-V_{th} CMOS multiplier. For supply voltages of 0.8 V and above, the multiplier is fully functional regardless of the values of the back-bias voltages. At lower supply voltages, a balance between the two biases is required to maintain minimum values of $I_{onNMOS}/I_{offPMOS}$ and $I_{onPMOS}/I_{offNMOS}$ to ensure proper circuit operation. In addition, since the NMOS transistors have lower built-in (V_{pwell}=0 V) threshold voltage than the PMOS transistors, the zone of valid operation at low supply voltages is offset with respect to the diagonal. The multiplier was found to be functional down to V_{dd}=0.16 V while a calibration circuit fabricated on the same die and containing inverters, latches, a one-bit adder, multiplexers and level-shifting circuits was error-free down to V_{dd}=0.12 V.

Figure 5 shows multiplier performance vs. supply voltage for both technologies. The range of points at each value of V_{dd} corresponds to various combinations of (V_{dd}−V_{nwell}) and V_{pwell} ranging from (0,0) to (−4,−4). Standard CMOS runs at 136 MHz at V_{dd}=3.3 V. Low threshold CMOS runs at 188 MHz at V_{dd}=2.0 V, 136 MHz at V_{dd}=1.3 V and at 40 MHz at V_{dd}=0.4 V.

In low threshold CMOS, the key to achieve minimum power at the required performance is to choose the optimum ra-

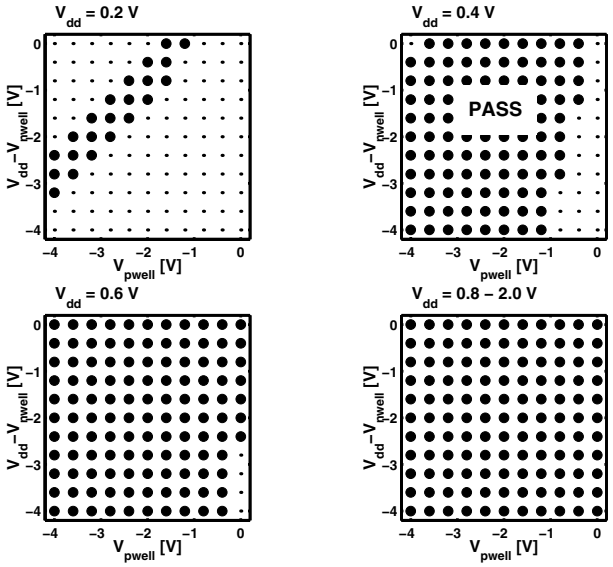

Figure 4: Shmoo plot for low-V_{th} CMOS multiplier implementation

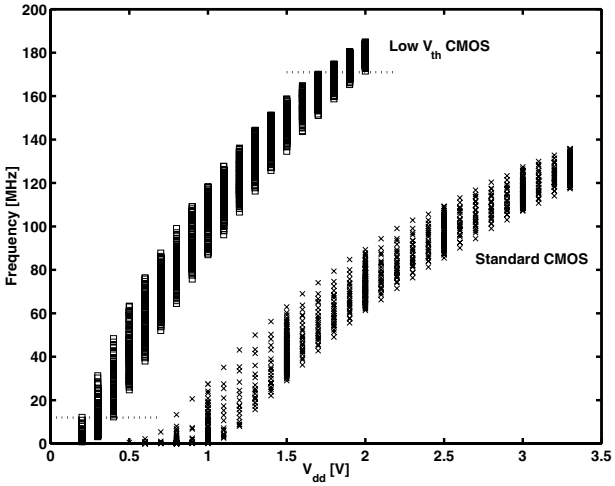

Figure 5: Multiplier frequency vs. supply voltage for standard and low-V_{th} implementation

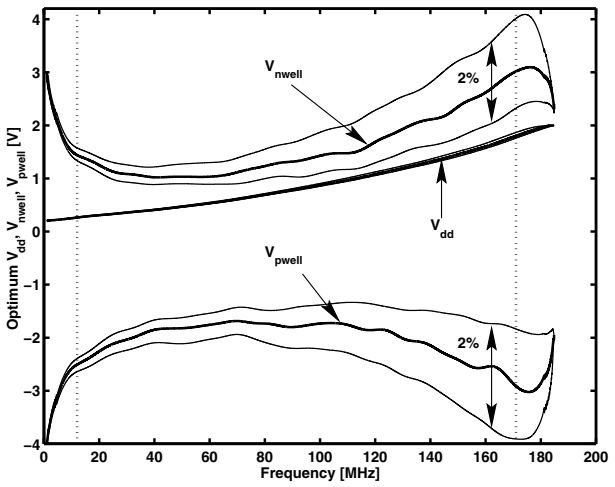

Figure 6: Optimum supply and well voltages vs. frequency for low-V_{th} implementation

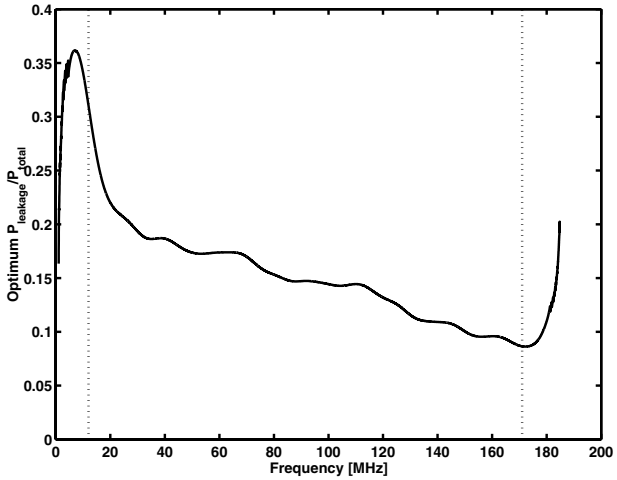

Figure 7: Optimum ratio of leakage power to total power vs. frequency for low-V_{th} implementation

tio of leakage power to total power. For example, for the multiplier to run at 40 MHz, one can choose the a supply voltage ranging from 0.37 to 0.6 V. Although a lower supply voltage may seem advantageous, it requires very low thresholds which in turn makes leakage power too large. Figure 6 shows the supply and well voltages which result in minimum total power at the given frequency. Values are guaranteed to be optimum only in the frequency range between 12 and 171 MHz. Namely, at highest frequencies it is more efficient to run at higher supply and threshold voltages. However, since we limited our supply voltage to 2 V, the only way to achieve the highest frequencies is to run at maximum supply voltage and lowest thresholds.

In addition to optimum supply and well voltages, Figure 6 also gives the ranges of these variables within which total power is within 2% of the minimum. It shows that if one is to achieve the highest efficiency, the supply voltage has to be controlled to within 3%, while the well voltages have significantly larger margin.

Figure 7 gives the optimum ratio of leakage power to total power vs. frequency. At 12 MHz the optimum ratio is as high as 30% and it decreases to 8% at 171 MHz. This variation is caused by different rates of change of leakage and active power as a function of the available ranges of supply and threshold voltage needed to achieve a desired frequency.

Figure 8 shows energy per multiplication vs. frequency of operation for standard CMOS and low-V_{th} CMOS technology. The first curve shows standard CMOS operating at V_{dd}=3.3 V. This is the typical mode of operation for most power-insensitive applications. The increase in energy per operation with decreasing frequency is attributed to the nature of the small-swing circuits used in the multiplier. Namely, the increase in amount of time between consecutive clock cycles increases the voltage swing of the small-swing nodes. The second curve shows standard CMOS at the minimum supply that is functional at that frequency. The third curve shows low-V_{th} CMOS operating at V_{dd}=2.0 V, V_{nwell}=V_{dd}, V_{pwell}=Gnd. Here, the increase in energy per

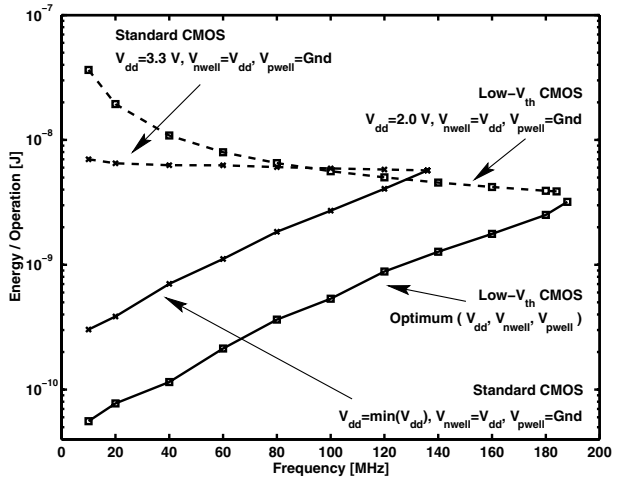

Figure 8: Energy per multiplication vs. frequency for standard and low-V_{th} CMOS implementation

operation with decreasing frequency is attributed to leakage. The fourth curve minimizes the power consumption at each frequency by optimizing V_{dd}, V_{nwell} and V_{pwell} as given in Figure 6. Although low-V_{th} CMOS with fixed V_{dd} is the least efficient at frequencies less than 100 MHz, low-V_{th} CMOS with optimum V_{dd}, V_{nwell} and V_{pwell} is the most efficient regardless of the frequency of operation. It is 5 times more energy efficient than standard CMOS with variable V_{dd}, and up to 100 times more efficient than standard CMOS at V_{dd}=3.3 V.

(Energy x Time) is often considered as metric of choice for low-power applications [8]. In Figure 9, it is plotted vs. supply voltage for the two technologies. The most optimum (Energy x Time) point for the low-V_{th} multiplier occurs at V_{dd}=0.36±0.01 V, $V_{dd}-V_{nwell}$=−0.8±0.2 V and V_{pwell}=−2±0.2 V, and is 5.6 times smaller than the lowest (Energy x Time) value attainable in standard CMOS at V_{dd}=1.2 V.

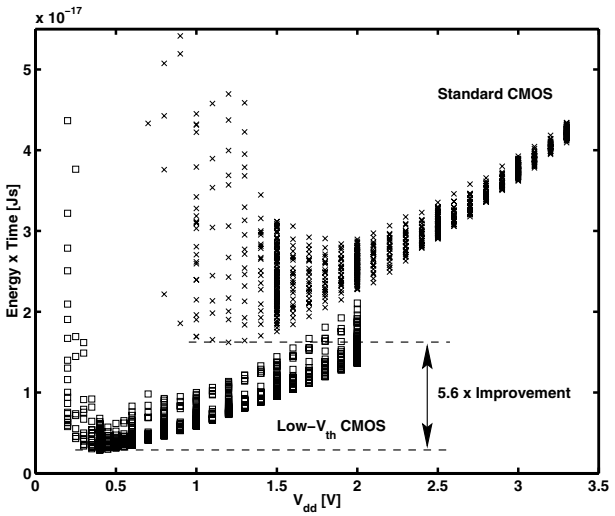

Figure 9: (Energy x Time) vs. supply voltage for standard and low-V_{th} CMOS implementation

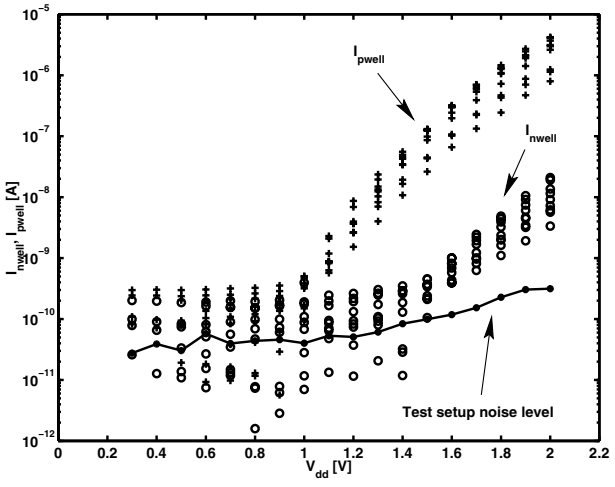

Figure 10: I_{pwell} and I_{nwell} vs. supply voltage for low-V_{th} CMOS implementation

Figure 10 shows well currents (I_{pwell} and I_{nwell}) as a function of supply and well voltages measured at the maximum frequency of operation achievable at those voltages. While below 1 V both well currents are independent of supply voltage, above 1 V there is strong dependence of well currents on supply voltage. Most of this current can be attributed to the source/drain to body junction leakage. At V_{dd}=2 V, the ratio of supply current to well current is about 7×10^4 and at V_{dd}=1 V the ratio drops below 1.2×10^8.

4. CONCLUSIONS

We have demonstrated that tunable, near-zero threshold CMOS under optimum balance of leakage and total power leads to significant power savings as compared to standard CMOS. In addition, if desired, tunable, near-zero threshold CMOS also offers performance advantages over standard CMOS. We show that in medium size chips well currents are small and that well voltages can be loosely controlled without sacrificing energy efficiency. We believe that near-zero threshold CMOS, in combination with active supply and well voltage control [9, 10, 11], which is used to compensate for circuit style, activity, logic depth, global threshold variations and temperature, is a viable alternative to standard CMOS.

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6. ADDITIONAL AUTHORS

Additional authors: Takayasu Sakurai (Institute for Industrial Science, University of Tokyo, Japan, email: `tsakurai@iis.u-tokyo.ac.jp`)

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