# Hierarchical Interconnect Circuit Models†

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## ABSTRACT

**The increasing size of integrated systems combined with deep submicron physical modeling details creates an explosion in RLC interconnect modeling complexity of unmanageable proportions. Interconnect extraction tools employ hierarchy to manage complexity, but this hierarchy is discarded via eliminating far away coupling terms when the equivalent RLC circuits are formed. The increasing dominance of capacitance coupling along with the emergence of on-chip inductance, however, makes the composite effect of far-away couplings increasingly evident. Even if newly enforced design rules and practices will ultimately obviate the need for modeling these couplings for design verification, some approximation of the "exact" solution is required to validate these rules. This paper proposes an efficient hierarchical equivalent circuit representation of interconnect parasitics that utilizes the efficient hierarchical long–distance modeling *already existing within extractors*. Results from a prototype simulator based on these hierarchical models demonstrates the simulation inaccuracy incurred when the far-away coupling terms are ignored. Such a form of interconnect modeling may provide the key to hierarchical modeling of electro-magnetic interactions between large components on future gigascale systems.**

## I. INTRODUCTION

Technology improvements for integrated circuits are continually decreasing minimal feature sizes such that the task of modeling short–range parasitic interconnect couplings is becoming increasingly complex. The same technology improvements are facilitating larger integrated circuits/systems that are realized via component–based design methods to cope with the overwhelming design complexity and time-to-market constraints. The parasitics and the component based methods make it necessary to model couplings between large portions of a chip for which the individual wire–to–wire couplings are largely insignificant but the collective effect of all couplings are important. Hierarchical models for interconnect parasitics become imperative for such systems.

At the lowest levels of modeling detail, hierarchical approaches have been used extensively for interconnect parasitic extraction via the *fast multipole method* [1] and the *hierarchical refinement method* [5]. These strategies reduce the extraction complexity usually to order linear in the number of source objects in the system. Conceptually this complexity reduction is made possible by representing the collective couplings/interactions between *groups* of conductors. Unfortunately, this hierarchy is generally destroyed when the RLC equivalent circuit models are created for simulation.

To map the extraction models to equivalent circuits, the far-away coupling terms are typically discarded, or treated as couplings to ground. But with the increasing dominance of coupling capacitance, and the recent emergence of on-chip inductance, modeling and design management of electromagnetic interactions between wires becomes increasingly important. Even though the individual couplings between wire segments in adjacent components can be inconsequential, the composite couplings between the collective wires in each component can have a significant impact on performance. This will be demonstrated in examples at the end of this paper by comparing exact and truncated parasitics models. In addition, truncation of far field couplings to localize parasitic couplings can cause instabilities in the localized models [6].

In many cases design rules and rigid design practices will be enforced so that simpler models and analyses can be applied for final design verification. However, even in such cases, some understanding of the "exact" solution, hence the actual electromagnetic couplings, is required to validate the design rules.

This paper proposes a first-step toward hierarchical RLC circuit models to capture parasitic-interconnect interactions. This new circuit modeling approach proposes the concept of a *global circuit node (gcn)* (see Fig. 1). Instead of modeling the coupling between two parts of a circuit by including all individual couplings, two new auxiliary nodes are introduced to model the entire coupling by a single value. Short range couplings are still modeled individually, but are not included in Fig. 1 for clarity.

The new global circuit node variables represent "averaged" source and potential values over an entire group of conductors and manifest themselves in the equivalent hierarchical circuit implementation in terms currents and voltages for the additional nodes. The interaction between global and local nodes is modeled via controlled sources which accumulate node voltages and filament currents for larger groups within an RLC network and redistribute the resulting higher–level currents and charges down to the lower levels of the hierarchy. The key to this approach is the wavelet expansion used to provide the averaging function for this interaction.

This modeling approach is the circuit equivalent to the accumulation and distribution processes seen in the fast potential evaluation methods employed in parasitic extractors. The sparse RLC circuit models are generated *directly* from the hierarchical extraction results (such as in [2] or [3]) rather than creating, then reducing a large, flattened RLC circuit.

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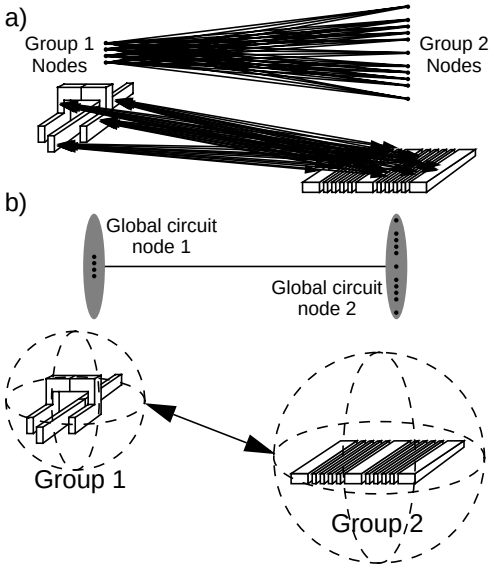


**Figure 1:** Concept of Hierarchical Coupling. Individual couplings are very small but collective effect is significant.
*a) Conventional:* Every small coupling must be included to model the entire interaction.
*b) Hierarchical:* Significant mutual coupling is stored as one single *global* coupling. Couplings within each region are still included in detail (not drawn in both cases for clarity).

The hierarchical equivalent circuit models are incompatible with certain features of existing simulators, therefore we have implemented a prototype simulator in *Matlab* to compare the standard, flat representation of interconnect parasitics with this new hierarchical equivalent circuit model approach. Results are shown which demonstrate the accuracy and efficiency of this hierarchical approach.

## II. Background

Present–day parasitic extractors represent far and near field couplings hierarchically to reduce the memory and runtime requirements for the potential matrix evaluation to order *O(N)*, with *N* being the number of units (panels, filaments) into which the interconnect has been subdivided for a boundary element method (BEM) solution (see [4]). The hierarchical approach exploits that the potential of a point charge or a localized current distribution decays with at least *1/r* with increasing distance *r* from the source (charge, current). Groups of sources, therefore, appear as point sources (monopoles) at sufficiently large distances.

It follows that it is unnecessary to model couplings between each unit pair separately if the desired potential evaluation (and thus extraction) accuracy is limited. Couplings are only necessary if the distance of the two units is comparable to the minimal distance between them. Far range couplings are only represented as couplings between pairs of *groups of units* whose group size is comparable to the minimal distance between the groups.

Since the average number of neighbors (directly coupled groups) of each unit and group is only dependent on the desired accuracy (which is assumed to be given and fixed) (see [5]), the total number of couplings for the entire interconnect system is of the order *O(N)*. If the number of nodes in the hierarchical tree is fixed and the accuracy is increased, the number of couplings will increase (more couplings at lower levels).

Unfortunately, this efficient hierarchical representation of interconnect parasitics is not generally exploited to create sparse parasitics netlists for subsequent simulation or timing analysis (Fig. 2). The extraction tool typically produces a netlist with coupling capacitances and inductances between only the smallest units of the interconnect circuit representation: the nodes and branch self–inductances. To cope with the resulting huge RLC circuits in timing analysis, model order reduction methods have been developed to represent the linear interconnect by equivalent circuits modeling only its dominant dynamic features. But even these reduction methods cannot cope with the full $O(N^2)$ couplings that the extractor would nominally generate.

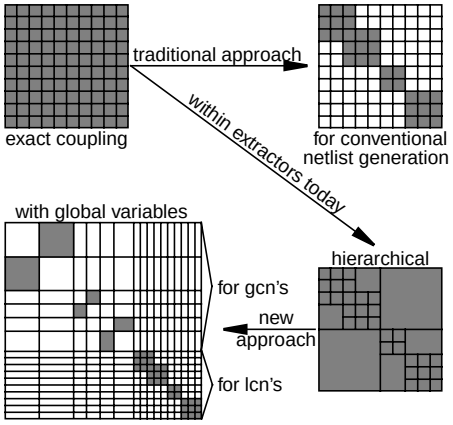


**Figure 2:** Conventional vs. hierarchical sparsity. Each small square symbolizes one number with the grey fields being nonzeros.

The standard approach to interconnect matrix sparsification has been to *remove* long range couplings by simply truncating them or mapping them to the near field couplings to preserve stability. This makes model order reduction feasible and is appropriate as long as the far-away couplings are actually negligible. Removal of long range couplings makes extraction more efficient, since an entire chip can be broken down into a set of small interconnect patterns which are precomputed and stored in a database. Simulation becomes more efficient since the coupling matrices (capacitance, inductance) of the circuit contain mainly zeroes and are, therefore, *conventionally sparse*(Fig. 2).

Increasing density of IC interconnect and the high-performance component-based design styles, however, render the electromagnetic influence between different parts of a chip significant even when the individual wire–to–wire couplings may be negligible. To address this problem we must exploit the *hierarchical sparsity*, which manifests itself in a different way than conventional sparsity (see Fig. 2).

## III. Hierarchical Equivalent Circuit Models

Since simulators today are only able to take direct advantage of conventional sparsity, we convert the hierarchically sparse parasitics representation within the extractor into a conventionally sparse structure via the introduction of *global circuit nodes (gcn)*. These nodes, which represent groups of conductors, augment the currently used *local circuit nodes (lcn)* which describe single conductors (see Fig. 1).

We have developed a methodology to translate the hierarchically sparse representation within the extractor into a hierarchical equivalent circuit that can be simulated by a variation of modified nodal analysis. Voltage controlled voltage and current controlled

current sources are used to redistribute the accumulated node voltages and filament currents for larger groups within an RLC circuit from the higher–level (global) currents and charges down to the lower levels of the hierarchy. This is the circuit equivalent to the accumulation and distribution processes seen in the fast potential evaluation methods employed in parasitic extractors. The key to such an approach lies in the derivation of the coefficients for the controlled sources, which is described in the following two subsections.

### *A. Capacitance*

#### *a) Accumulation of Node Potentials*

For the example in Fig. 3, let $V_{Ai}$ be the potential of the $i^{th}$ node in the aggressor group *A*. Let $Q_{Gj,A}$ be the charge at the $j^{th}$ node in the victim group *G* due to the potentials of the conductors in *A*. Similarly for groups *B* and *H*. Then

$$Q_{Gj,\,A} = \sum_{i \in A} C_{ji} V_{Ai} \tag{1}$$

Where $C_{ji}$ is the *short circuit capacitance* between nodes *i* and *j*. Current relationships can be found by taking the time derivative of the corresponding charge relations. The total charge induced in *G* and *H* by the potential of conductors in *A* is

$$Q_{GH,\,A} = \sum_{i \in A} V_{Ai} \sum_{j \in GH} C_{ji} \tag{2}$$

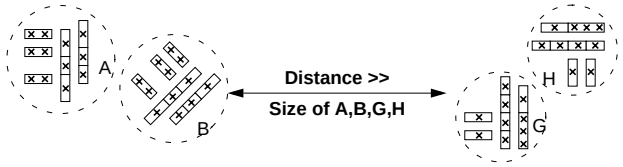


**Figure 3:** Example system: *A,B* — aggressor groups; *G,H* — victim groups

Total charge on *G* and *H* separately is defined similarly. The fraction of charge induced in *G* from (2) is $Q_{G,A}/Q_{GH,A}$. However, this expression depends on the aggressor node potentials:

$$(Q_{G,\,A}/Q_{GH,\,A})_{exact} = \frac{\left(\sum_{i \in A} V_{Ai} \sum_{j \in G} C_{ji}\right)}{\left(\sum_{i \in A} V_{Ai} \sum_{j \in GH} C_{ji}\right)} \tag{3}$$

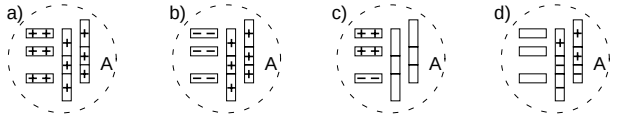


**Figure 4:** Wavelet expansion of aggressor group *A* from Fig. 3. *a)* Order 0 *b)* Order 1 *c),d)* Order 2. Note the potential signs.

The node potential accumulation rule for the hierarchical equivalent circuit must be linear in the aggressor node voltages to be implemented as a controlled source, so (3) needs to be approximated by an expression independent of the $V_{Ai}$. For this, we expand the $V_{Ai}$ in terms of a wavelet–like expansion (up to second order shown in Fig. 4). Using only the zeroth order term for the $V_{Ai}$ (all $V_{Ai}$ equal to 1) we find the approximation

$$(Q_{G,\,A}/Q_{GH,\,A})_{est} = \left(\sum_{i \in A} \sum_{j \in G} C_{ji}\right) / \left(\sum_{i \in A} \sum_{j \in GH} C_{ji}\right) \tag{4}$$

The accuracy of this approximation can be increased by increasing the minimal distance between conductor groups to which this coupling approximation is applied (increasing the window size). Weighting the total charge induced by *A* with the factor in (4) yields an approximation for $Q_{G,A}$ which depends linearly on the composite potential of *A*:

$$(Q_{G,\,A})_{est} = \tag{5}$$
$$\left[\left(\sum_{i \in A} V_{Ai} \sum_{j \in GH} C_{ji}\right) / \left(\sum_{i \in A} \sum_{j \in GH} C_{ji}\right)\right] \cdot \left(\sum_{i \in A} \sum_{j \in G} C_{ji}\right)$$

The first factor in (5) represents the accumulated node potentials of *A* which preserves the charge induced from *A* into *each of its victim groups* with a high level of accuracy:

$$V_A^{est} = \left(\sum_{i \in A} V_{Ai} \sum_{j \in GH} C_{ji}\right) / \left(\sum_{i \in A} \sum_{j \in GH} C_{ji}\right) \tag{6}$$

When using a hierarchical extractor to find the couplings, the individual $C_{ij}$ will not be available. One must approximate the individual couplings on a per instance basis by local extraction. The second factor in (5) is the composite coupling from *A* to *G*. This composite coupling is regularly generated within hierarchical extractors in use today [2], so there is no extra effort necessary to get this value.

#### *b) Distribution of Node Charge (Current)*

The higher level charge for the victim nodes must be redistributed onto the child nodes using controlled sources in the hierarchical equivalent circuit model. We will, for maximum accuracy, distribute the higher level charge as close as possible to the exact distribution. In the exact case, the fraction of charge on node *Gj* is

$$(Q_{Gj,\,AB}/Q_{G,\,AB})_{exact} = \tag{7}$$
$$\left(\sum_{i \in A} C_{ji} V_{Ai} + \sum_{i \in B} C_{ji} V_{Bi}\right) / \left(\sum_{j \in G} \left(\sum_{i \in A} C_{ji} V_{Ai} + \sum_{i \in B} C_{ji} V_{Bi}\right)\right)$$

Applying again the zeroth order of the expansion for the aggressor potential distribution shown in Fig. 4 (but now for all aggressors combined), we find

$$(Q_{Gj,\,AB}/Q_{G,\,AB})_{est} = \left(\sum_{i \in AB} C_{ji}\right) / \left(\sum_{j \in G} \sum_{i \in AB} C_{ji}\right) \tag{8}$$

This ratio can be used to find the approximate amount of charge induced on *Vj* by all aggressors in *A* and *B*:

$$(Q_{Gj,\,AB})^h_{est} = (Q_{G,\,AB})^h \cdot \left(\sum_{i \in AB} C_{ji}\right) / \left(\sum_{j \in G} \sum_{i \in AB} C_{ji}\right) \tag{9}$$

### *B. Inductance*

#### *a) Accumulation of Branch Currents*

Cartesian coordinates are used in the following and bold characters denote *xyz*–vectors. For the example in Fig. 5 let $\boldsymbol{I}_{Ai}$ be the current in the $i^{th}$ segment in the aggressor group *A*. Let $\Phi_{Gj,A}$ be the magnetic flux through the ∞–loops[1] in *x*–, *y*– and *z*–direction of the $j^{th}$ segment in the victim group *G* due to the currents of the segments in *A*. Similarly for *B* and *H*. Then

$$\Phi_{Gj,\,A} = \sum_{i \in A} \boldsymbol{L}_{ji} * \boldsymbol{I}_{Ai} \tag{10}$$

1. Perpendicular loops to infinity used in defining partial inductance.

where '*' denotes an element–by–element multiplication. Each $\boldsymbol{L}_{ji}$ is an *xyz*–vector specifying the partial inductive coupling in *x*, *y* and *z*–direction. In the following, branch voltage relations can be found by taking the time derivative of the corresponding flux relations. The total flux induced through the ∞–loops of *G* and *H* by the current in conductors in *A* is

$$\Phi_{GH,\,A} = \sum_{i \in A} \Big[ \bigcup_{j \in GH} \boldsymbol{L}_{ji} \Big] * \boldsymbol{I}_{Ai} \tag{11}$$

Total flux through *G* and *H* separately is defined similarly.

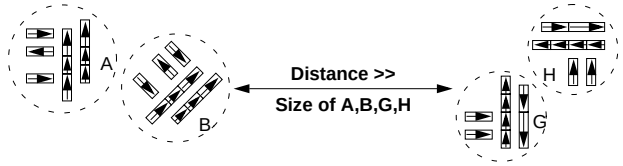


**Figure 5:** Example system: *A,B* — aggressor groups; *G,H* — victim groups. Pre–defined segment current directions shown.

$\cup_{j \in Y} \boldsymbol{L}_{ji}$ is defined as the *composite partial inductance* between an aggressor segment *i* and all segments in a victim group *Y* (see Fig. 6). This is *not* the sum of all individual partial inductances, but the amount of flux flowing through the composition of the ∞–loops of all segments in *Y* if unit current is flowing through the aggressor segment *i*. Overlapping loops are only counted once.

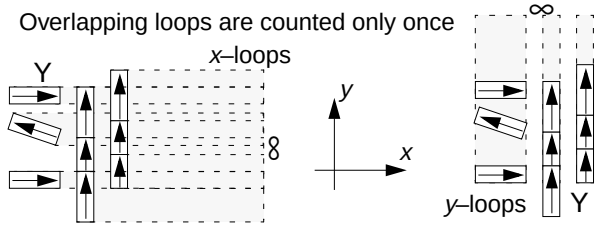


**Figure 6:** Composition of ∞–loops and definition of $\cup_{j \in Y} \boldsymbol{L}_{ji}$

The fraction of flux induced in *G* from (11) is $\Phi_{G,A} \backslash \Phi_{GH,A}$, where '\' denotes an element–by–element division. However, this expression depends on the aggressor branch currents:

$$(\Phi_{G,\,A} \backslash \Phi_{GH,\,A})_{exact} = \frac{\Big( \sum_{i \in A} \big[ \bigcup_{j \in G} \boldsymbol{L}_{ji} \big] * \boldsymbol{I}_{Ai} \Big)}{\Big( \sum_{i \in A} \big[ \bigcup_{j \in GH} \boldsymbol{L}_{ji} \big] * \boldsymbol{I}_{Ai} \Big)} \tag{12}$$

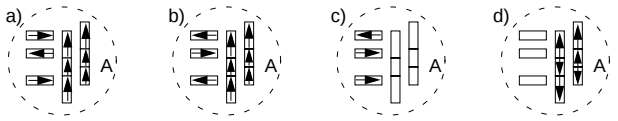


**Figure 7:** Wavelet expansion of aggressor group *A* from Fig. 3. *a)* Order 0 *b)* Order 1 *c),d)* Order 2. Note the current directions.

The branch current accumulation rule for the hierarchical equivalent circuit must be linear to be implemented as triplet of controlled sources, so (12) needs to be approximated by an expression independent of the $\boldsymbol{I}_{Ai}$. For this, we expand the $\boldsymbol{I}_{Ai}$ in terms of a wavelet–like expansion (up to second order shown in Fig. 7). Using only the zeroth order term for the $\boldsymbol{I}_{Ai}$ (all $\boldsymbol{I}_{Ai}$ equal to unit in their current directions) we find the approximation:

$$(\Phi_{G,\,A} \backslash \Phi_{GH,\,A})_{est} = \Big( \sum_{i \in A} \bigcup_{j \in G} \boldsymbol{L}_{ji} \Big) \backslash \Big( \sum_{i \in A} \bigcup_{j \in GH} \boldsymbol{L}_{ji} \Big) \tag{13}$$

The accuracy of this approximation can be increased by increasing the minimal distance between conductor groups to which this coupling approximation is applied (increasing the window size). Weighting the total flux induced by *A* with the factor in (13) yields an approximation for $\Phi_{G,A}$ which depends linearly on the composite branch currents of *A*:

$$(\Phi_{G,\,A})_{est} = \tag{14}$$

$$\Big[ \sum_{i \in A} \bigcup_{j \in G} \boldsymbol{L}_{ji} \Big] \cdot \Big[ \Big( \sum_{i \in A} \big[ \bigcup_{j \in GH} \boldsymbol{L}_{ji} \big] * \boldsymbol{I}_{Ai} \Big) \backslash \Big( \sum_{i \in A} \bigcup_{j \in GH} \boldsymbol{L}_{ji} \Big) \Big]$$

The second factor in (14) represents the averaged branch currents of *A* in all three directions which preserves the magnetic flux induced from *A* into *each of its victim groups* with a high level of accuracy:

$$\boldsymbol{I}_A^{est} = \Big[ \Big( \sum_{i \in A} \big[ \bigcup_{j \in GH} \boldsymbol{L}_{ji} \big] * \boldsymbol{I}_{Ai} \Big) \backslash \Big( \sum_{i \in A} \bigcup_{j \in GH} \boldsymbol{L}_{ji} \Big) \Big] \tag{15}$$

The first factor in (14) is the composite inductive coupling from *A* to *G*. This composite coupling is regularly generated within hierarchical extractors in use today [3], so there is no extra effort necessary to get these values.

*b) Distribution of Branch Magnetic Flux (Voltage)*

The higher level magnetic flux for the victim groups must be redistributed onto the child segments using controlled sources in the hierarchical equivalent circuit model. We will, for maximum accuracy, distribute the higher level flux as close as possible to the exact distribution. In the exact case, the fraction of flux through the ∞–loop of segment *Gj* is

$$(\Phi_{Gj,\,AB} \backslash \Phi_{G,\,AB})_{exact} = \Big( \sum_{i \in A} \boldsymbol{L}_{ji} * \boldsymbol{I}_{Ai} + \sum_{i \in B} \boldsymbol{L}_{ji} * \boldsymbol{I}_{Bi} \Big) \backslash \Big( \sum_{i \in A} \big[ \bigcup_{j \in G} \boldsymbol{L}_{ji} \big] * \boldsymbol{I}_{Ai} + \sum_{i \in B} \big[ \bigcup_{j \in G} \boldsymbol{L}_{ji} \big] * \boldsymbol{I}_{Bi} \Big) \tag{16}$$

Applying again the zeroth order of the expansion for the aggressor branch current distribution shown in Fig. 7 (but now for all aggressors combined), we find

$$(\Phi_{Gj,\,AB} \backslash \Phi_{G,\,AB})_{est} = \Big( \sum_{i \in AB} \boldsymbol{L}_{ji} \Big) \backslash \Big( \sum_{i \in AB} \big[ \bigcup_{j \in G} \boldsymbol{L}_{ji} \big] \Big) \tag{17}$$

This ratio can be used to find the approximate amount of flux induced through the ∞–loop of *Gj* by all aggressors in *A* and *B*:

$$(\Phi_{Gj,\,AB})_{est}^{h} = (\Phi_{G,\,AB})^{h} * \Big[ \Big( \sum_{i \in AB} \boldsymbol{L}_{ji} \Big) \backslash \Big( \sum_{i \in AB} \big[ \bigcup_{j \in G} \boldsymbol{L}_{ji} \big] \Big) \Big] \tag{18}$$

*C. Couplings:*

The long–distance couplings, such as those represented by hierarchical or multipole expansions, are modeled by introducing relatively few group–to–group coupling capacitors and inductors between auxiliary higher–level nodes to represent global interactions within the system.

Using our equivalent model, we capture the long–range couplings efficiently, while avoiding an overwhelming number of minuscule separate L's and C's. This is in contrast to most methodologies which discard these terms all together, even though

their aggregate long-distant coupling impact can be significant when all of the single components are not. We believe that these aggregate couplings are becoming more important for controlling electromagnetic interactions on high-performance component-based designs.

## IV. Present–Day Simulator Restrictions

Commercial circuit simulators, such as SPICE [7], allow only independent voltage sources as controllers for current controlled sources. This arbitrary restriction would require approximately *2N* additional nodes for our hierarchical equivalent circuit models (where *N* is the number of filaments). In addition, SPICE would require mutual inductors between zero–valued self–inductors to model the long range magnetic interaction. since a mutual inductor $M_{12}$ between two self–inductors is specified by its *coefficient of induction* $M_{12}/\sqrt{L_1 L_2}$. This representation breaks down for our hierarchical equivalent circuit model since the coefficient of induction would be infinite for the global circuit nodes. One could work around these restrictions with elaborate controlled source elements in the SPICE netlist, however, doing so would reduce the performance gains introduced by the hierarchy.

To allow a fair comparison of the original, flat circuit and our hierarchical equivalent circuit model, we have implemented a prototype simulator in *Matlab* without the restrictions listed above. It handles couplings between zero–valued self–inductors and allows current controlled sources to be controlled by any element which introduces a current variable in the MNA matrix representation. In addition, self–inductors and their associated voltage controlled voltage sources are represented by single *composite inductors*. All of this is possible since the prior restrictions were not rooted in the algorithms commonly used for circuit simulation (like modified nodal analysis, which we applied), but were obsolete conventions for simulators which were written for systems with much simpler interconnect circuits when nonlinear devices dominated the circuit behavior.

## V. Circuit Examples

Large signal busses are especially sensitive to on–chip interconnect parasitics while being very costly to analyze. We chose such examples to demonstrate the efficiency of our hierarchical circuit models.

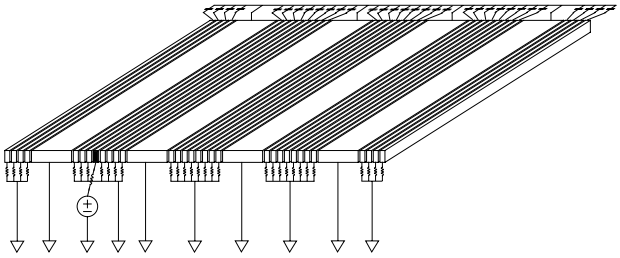

**Figure 8:** 32 bit bus structure with four return lines.

### *A. 32bit Bus Example with In–Plane Return Lines*

Fig. 8 shows a 32 bit bus in which line 8 is active. For all signal lines driver resistance is 70Ω, load capacitance 25pF, thickness 2µm, spacing 2µm, length 1000µm and width 2µm. The width of returns is 7µm. System size is about 1015µm. Materials are copper (ρ=17.5nΩm) and $SiO_2$ ($\varepsilon_r$=3.9, $\mu_r$=1.0).

In Fig. 9 the voltage responses at the far end of the active line are compared for four cases: The full RLC system, hierarchical model for a lowest–level window of 25% system size (72% sparsity), truncation for same window size (and truncation with comparable accuracy to hierarchical case. Here the window size is roughly 62% system size (20% sparsity).

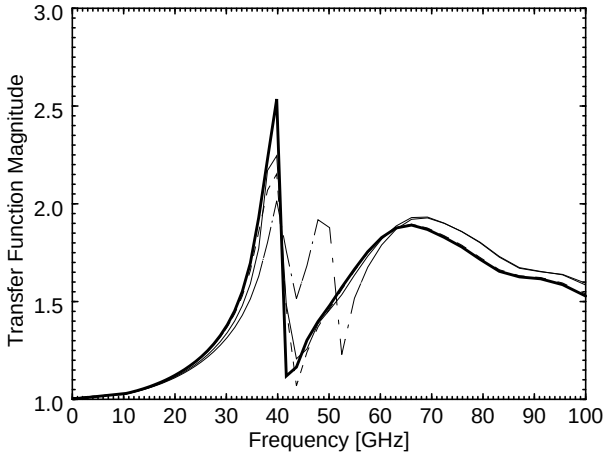


**Figure 9:** Transfer function from near to far end node of active line in Fig. 8. Shown are the frequency dependencies for the full system (**solid bold**), small window hierarchical (solid), small window truncation (dash–dot) and large window truncation (dashed).

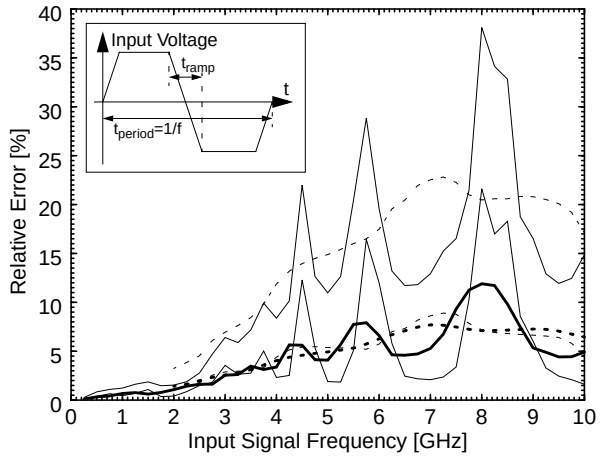


**Figure 10:** Active line far end node signal error vs. signal frequency. Signal is ramp–rectangular wave shown in upper left ($t_{ramp}$=$t_{period}$/20). Hierarchical small window (**bold**), truncate small window (upper thin curve), truncate large window (lower thin curve). Running averages shown dotted.

The hierarchical accuracy is clearly much better around the resonance peak at about 40GHz than that for truncate for the same window size. This explains in turn the lower signal error of the hierarchical model in Fig. 10. Since the Fourier transform of the ramp wave shown in Fig. 10 is a *sinc* wave, the resonance peak from Fig. 9 is repeated periodically in Fig. 10 every time a peak of the *sinc* wave passes through the resonance region of the interconnect system. This causes the choppy behavior of all results. However, the variance of the hierarchical signal error is smaller than for truncate–only, showing higher stability of the hierarchical model.

For the same small window size (72% sparse) the hierarchical model has not only a 2–3x higher accuracy than truncation, but also shows the resonance peak at 40GHz clearly which the truncation approach only shows when considering 80% of all individual couplings. This shows that composite long–range interactions are not negligible, but must be included for accurate

modeling of the interconnect parasitics. Table 1 shows that for large window, truncation requires a runtime about 3.5x that of the hierarchical model, although the error is still higher. For comparable sparsity, runtime and memory consumption of the hierarchical model are moderately larger than for truncation, due to the overhead caused by the global circuit nodes. As a consequence, however, the accuracy is better for the hierarchical approach due to the inclusion of composite long distance interactions.

| | Full | Hier. small | Tr. small | Tr. large |
|---|---|---|---|---|
| Runtime [s] | 16810 | 2932 | 1692 | 10777 |
| Window [μm] | 1015 | 257 | 257 | 621 |
| Capacitance Elements | 63,896 | 17,513 | 17,496 | 50,936 |
| Inductance Elements | 64,980 | 18,381 | 18,324 | 51,660 |
| Sparsity | 0% | 72.1% | 72.2% | 20.4% |

**Table 1:** Runtime and memory comparison for results in Fig. 9.

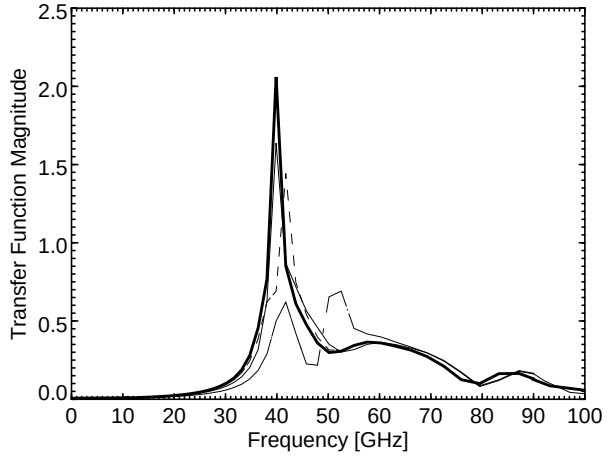


**Figure 11:** Transfer function from near to far end node of leftmost return line in Fig. 8. Shown are the frequency dependencies for the full system (**solid bold**), small window hierarchical (solid), small window truncation (dash–dot) and large window truncation (dashed).

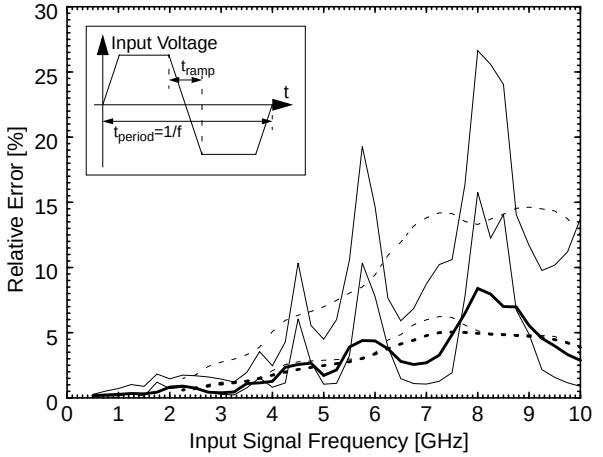


**Figure 12:** Leftmost return line far end node signal error vs. signal frequency. Signal is ramp–rectangular wave shown in upper left ($t_{ramp}=t_{period}/20$). Hierarchical small window (**bold**), truncate small window (upper thin curve), truncate large window (lower thin curve). Running averages shown dotted.

For the far end node of the leftmost return line in Fig. 8 the transfer functions in frequency domain are shown in Fig. 11. The transfer function for the hierarchical equivalent circuit matches very well with the result using the full system, while the truncated model (both for small and large window size) does not capture the resonance frequency accurately.

As a consequence, the far end signal error for the truncate models is larger than for the hierarchical model (see Fig. 12). For increasing system size the impact of long distance couplings will increase.

### *B. Five Signal Lines over Meshed Ground Plane*

As a second example we chose a five line signal bus over a ground plane which is modeled by a two–dimensional (10 x 10) filament mesh (see Fig. 13). For all signal lines driver resistance is 50 Ω, load capacitance 2 fF, thickness 3.5 μm, spacing 10 μm, length 1000 μm and width 10 μm. Spacing to ground plane is 5 μm. System size is about 1005 μm. Materials are copper ($\rho$ = 17.5 nΩm) and $SiO_2$ ($\varepsilon_r$ = 3.9, $\mu_r$ = 1.0). The middle signal line is active.

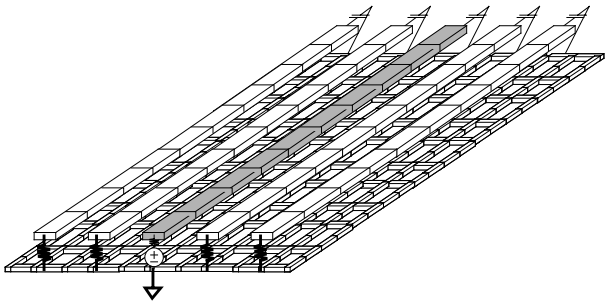

**Figure 13:** Five parallel signal wires over 10 x 10 meshed ground plane.

To accurately model the current and charge distribution for the ground plane, usually a large number of individual filaments is necessary. The full interconnect parasitic model grows very rapidly even at modest modeling accuracies. A hierarchical approach can potentially create huge runtime / memory savings, by modeling the coupling from the signal lines to larger but more distant patches of the ground plane with only few mutual capacitances and inductances. The same is true for couplings between distant parts of the same ground plane.

In Fig. 14 and 15 the accuracy of the far end voltage response for the leftmost signal line is compared for truncate–only and our hierarchical modeling approach. Again, we find that in order to reach similar accuracy for the truncated and the hierarchical electromagnetic model, the truncation window needs to be extended significantly and runtime / memory consumption increase (see Table 2).

| | Full | Hier. small | Tr. small | Tr. large |
|---|---|---|---|---|
| Runtime [s] | 1510 | 882 | 315 | 1256 |
| Window Radius [μm] | 1005 | 255 | 255 | 662 |
| Capacitance Elements | 20080 | 7884 | 7325 | 17889 |
| Inductance Elements | 18985 | 6886 | 6641 | 16894 |
| Sparsity | 0 % | 62.1 % | 64.1 % | 10.8 % |

**Table 2:** Runtime / memory comparison for results in Fig. 14.

## VI. Conclusions and Future Directions

Decreasing feature sizes, increasing chip sizes and the emergence of component–based chip design necessitate the use of hierarchy for modeling IC parasitic interconnect in the near future. This paper proposes the concept of a *global circuit node* to represent groups of conductors that model collective coupling effects efficiently. Results were shown which demonstrate the efficacy of such an approach. It is the long-term objective of this

work to create new RLC circuit models that will facilitate the modeling of interconnect couplings at higher levels of abstraction so that large gigascale systems can be verified without flattening the components to the lowest circuit level. Another aim of future research will be reducing the runtime / memory overhead of the hierarchical equivalent circuit models with respect to truncate only models further to make hierarchical models even more efficient.

In addition, the finite propagation time for electromagnetic interactions will become a significant factor for accurate on–chip timing analysis for signal frequencies from a few GHz upward. Handling retardation effects for composite long distance couplings more efficiently will become necessary. Using hierarchical equivalent circuit models to this end will be another focus of our future research.

## REFERENCES


[1] L. Greengard, *The Rapid Evaluation of Potential Fields in Particle Systems*, The MIT Press, Cambridge, MA (1987).

[2] K. Nabors, J. White, *FastCap: A Multipole Accelerated 3–D Capacitance Extraction Program*, IEEE Trans. CAD, Vol. 10, No. 11, pp. 1447–1459 (November 1991).

[3] M. Kamon, M. Tsuk, J. White, *FastHenry: A Multipole Accelerated 3–D Inductance Extraction Program*, IEEE Trans. Microwave Theory and Techniques, **42**, No. 9, pp. 1750–1758 (Sept. 1994).

[4] C. Brebbia (Ed.), *Boundary element techniques in computer aided engineering*, NATO ASI on BEM in CAD (1983).

[5] W. Shi, J. Liu, N. Kakani, T. Yu, *A Fast Hierarchical Algorithm for 3–D Capacitance Extraction*, Proc. 35th Design Automation Conference (DAC) (June 1998).

[6] M. Beattie, L. Pileggi, *IC Analyses Including Extracted Inductance Models*, 36th Design Automation Conference (DAC) (June 1999).

[7] L. Nagel, R. Rohrer, *Computer Analysis of Nonlinear circuits, Excluding Radiation (CANCER)*, IEEE Journal of Solid State Circuits, **SC–6**, pp. 162–182 (Aug. 1971).


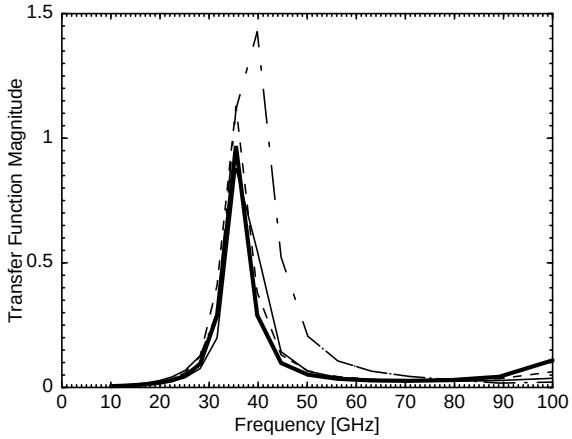


**Figure 14:** Transfer function from near to far end node of leftmost signal line in Fig. 13. Shown are the frequency dependencies for the full system (**solid bold**), small window hierarchical (solid), small window truncation (dash–dot) and large window truncation (dashed).

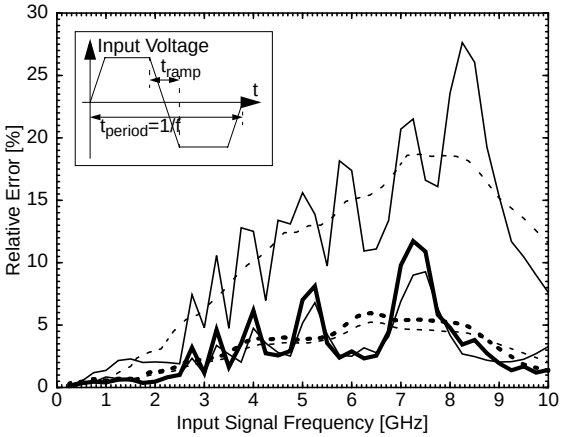


**Figure 15:** Leftmost signal line far end node voltage error vs. signal frequency. Signal is ramp–rectangular wave shown in upper left ($t_{ramp}$=$t_{period}$/20). Hierarchical small window (**bold**), truncate small window (upper thin curve), truncate large window (lower thin curve). Running averages shown dotted.