Stochastic Wire-Length and Delay Distributions of 3-Dimensional Circuits*

Rongtian Zhang, Kaushik Roy, Cheng-Kok Koh, and David B. Janes
ECE, Purdue University, West Lafayette, IN 47907-1285
{rzhang, kaushik, chengkoh, janes}@ecn.purdue.edu

ABSTRACT

3-D technology promises higher integration density and lower interconnection complexity and delay. At present, however, not much work on circuit applications has been done due to lack of insight into 3-D circuit architecture and performance. In this paper, we investigate the interconnect distributions of 3-D circuits. We divide the 3-D interconnects into horizontal wires and vertical wires and derive their wire-length distributions, respectively. Based on the stochastic wire-length distributions, we calculate 3-D circuit interconnect delay distribution. We show that 3-D structures effectively reduce the number of long delay nets, significantly reduce the number of repeaters needed, and dramatically improve the performance. With 3-D structures, a circuit can work at a much higher clock rate (double, even triple) than with 2-D. However, we also show that the impacts of vertical wires on chip area and interconnect delay may limit the number of device layers that we can integrate.

1. INTRODUCTION

The complexity of integrated circuits has grown dramatically over the past few decades. The trend is likely to continue in the next several technology generations. The *International Technology Roadmap for Semiconductors* (ITRS) projects that VLSI technology will reach tera-scale integration in the year 2014 [1], which means that more and more transistors will be closely packed and connected. To accommodate this increasing number of transistors and increasing complexity of interconnect, ITRS predicts that in 2014 (the end of the roadmap), the chip size would be well over $1000mm^2$, the feature size as small as $25nm$, and the number of metal layers as many as 10. Accompanying those trends are problems such as the strong quantum effect and short channel effect of ultra-mini devices, the complexity of global interconnection spanning over a vast single device layer, and more pronounced interconnect delay, all of which pose serious challenges to the 2-D process technology and circuit design. 3-Dimensional integration can provide a viable solution to those problems.

Although 3-D circuit concepts appeared in the early 1980s [2; 3; 4; 5], and many studies on process technology have been reported [6; 7; 8; 9], not much work has been done on circuit applications due to lack of design tools and methodologies and lack of insight into circuit architecture and performance. Most of the current circuit and physical design techniques are based on 2-D technologies, and they cannot be easily extended to handle 3-D integration. A main purpose of realizing 3-dimensional integration is to reduce the interconnect complexity and delay. Therefore, it is imperative to gain thorough understanding of wiring requirements and its impacts on the architecture and performance of 3-D circuits.

A schematic of 3-D circuit structure with 3 device layers is shown in Figure 1. Intuitively, 3-D technology offers compact logic gates and, in general, compact functional blocks and circuit structures. In 3-D circuits, transistors are stacked in several device layers, rather than spanned in a vast single device layer. Although that overcomes the problem of long and complicated wirings in 2-D layout, we foresee a new problem arising from the connections of gates in different device layers. Typically, we ignore the effects of vias in multi-metal layers of 2-D circuits. Unfortunately, the same can not be said for the vertical channels that connect one device layer to another in 3-D structures (see Figure 1). The process technology, materials, and structure of the 3-D vertical channels are completely different from those of 2-D metal contacts. A large number of vertical channels in a 3-D structure can be detrimental to the integration density due to the additional area required for such channels. The combined parasitic effects of several vertical channels may significantly impact the circuit performance, especially for circuits with large logic depth. Our study shows that more than 90% of wires go through vertical channels in a 8-device-layer structure. Without careful planning, the impact of the vertical channels may negate the advantages that 3-D structures offer.

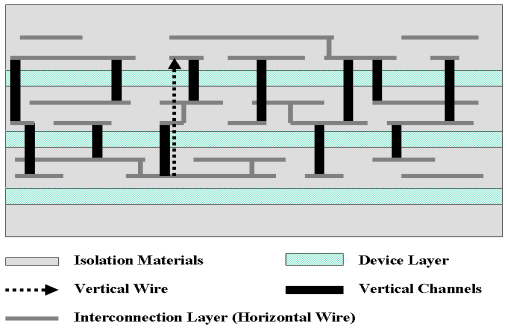

Figure 1: Schematic of 3-D circuit structure.

In this paper, we study the interconnect distributions of 3-D circuits. In order to best understand the wiring requirements, we divide the overall wires into two parts: horizontal wires and vertical wires. For a wire connecting one gate to another, we define the portions that are parallel to the device layers as a horizontal wire and the portions that are perpendicular to the device layers as a vertical wire (Figure 2). Horizontal wires determine the overall routing resources on top of each device layer, and are generally realized by metal layers. The vertical wires are realized by vertical channels and have an impact on the areas of device layers. Both horizontal and vertical wires contribute to the overall interconnection delay.

2. STOCHASTIC 3-D WIRE-LENGTH DISTRIBUTIONS

2.1 Rent's Rule

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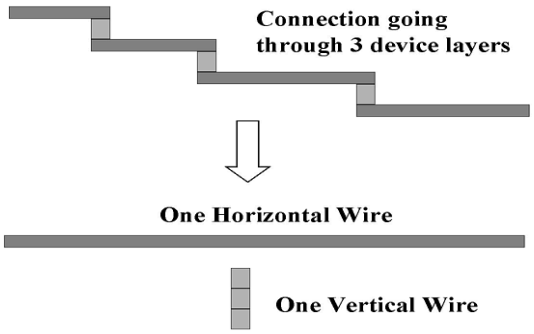

Figure 2: Definition of horizontal and vertical wire.

Several early works were very successful in predicting wire-length distribution and average interconnection length in 2-D circuits [10; 11; 12; 13; 14]. The primary assumptions in those analyses were based on a well-established empirical relationship commonly known as Rent's Rule. This relationship correlates the number of signal input and output terminals T, to the number of gates N, in a random logic network by a simple power law expression:

$$T = AN^p, \tag{1}$$

where A is a proportionality constant, and p $(0 < p < 1)$ is the interconnect complexity constant. We refer to A and p as Rent's parameters.

This empirical relationship holds for almost all large VLSI systems. For example, the number of external I/O pins for the Intel microprocessor family, from the Intel 4004 in 1971 up to the Pentium Pro in 1996, matches well with Rent's Rule [13].

Two extensions of Rent's Rule play key roles in its successful application to the characterization of 2-D wire-length distribution:

- Rent's Rule (with the same parameters) holds for all subcircuits when a circuit is partitioned.
- The number of interconnections, I, among a group of subcircuits, is proportional to the total terminal count of all the subcircuits, T_{total}, and the constant of proportionality, α, holds hierarchically [10; 11; 12]:

$$I = \alpha T_{total}. \tag{2}$$

In [13], *Davis, et. al.* presented a derivation of 2-D wire-length distribution and gave a closed form expression. In this section, we make a non-trivial extension of this approach to 3-D homogeneous circuits. By homogeneous, we assume that all gate pairs at a horizontal distance of ℓ are equally likely to connect to each other regardless of the device layers they are in.

Consider a system with N gates distributed in m device layers. To simplify the calculation, we assume that the gates are placed in a square array, as shown in Figure 3. Therefore, there are $\sqrt{\frac{N}{m}} \times \sqrt{\frac{N}{m}}$ cells in the entire array. Each cell has m gates stacked vertically. The overall connections among all gates, I_{total}, is independent of the number of device layers, m, and is given by [11]:

$$I_{total} = \alpha AN(1 - N^{p-1}). \tag{3}$$

All the connections among gates within each cell are in the vertical direction and do not contribute to the horizontal wires. The

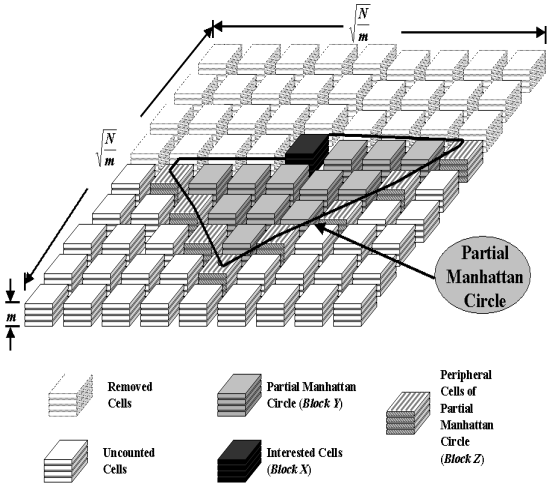

Figure 3: 4-device-layer 3-D Circuit Partitioning.

total number of such connections, I_{v_0}, can be calculated by applying Equation (3) to each cell and multiplying it by the total number of cells, $\frac{N}{m}$:

$$I_{v\_0} = \frac{N}{m}\alpha Am(1 - m^{p-1}) = \alpha AN(1 - m^{p-1}). \tag{4}$$

The total number of horizontal wires, I_{h_TOT}, is the total number of interconnections among all cells. It can be obtained by subtracting the total number of connections within each cell from the total number of connections among all gates:

$$I_{h\_TOT} = I_{total} - I_{v\_0} = \alpha AN(m^{p-1} - N^{p-1}). \tag{5}$$

2.2 Horizontal Wire-Length Distribution

Although the derivation of 3-D horizontal wire-length distribution is similar to the approach given in [13], many unique features of 3-D structures, i.e., multi-device layers, vertical wires, etc., need to be considered. For simplification, we highlight only those steps unique to 3-D structures.

To obtain the overall wire-length distribution, we first calculate the stochastic wire-length distribution of a single cell at the corner (and hence, obtain the wire-length distribution of all gates in that cell). Once the stochastic wire-length distribution is determined for the corner cell, we "remove" it from the system in order to prevent multiple counting of interconnects when we calculate the remainder of the wiring distribution. The same process is repeated for all cells in the system by scanning all cells from the top row to the bottom row and from the left to the right in each row. The wire-length distribution for all the N gates in m device layers is obtained by aggregating the wire-length distribution for individual cells (see Figure 3).

In order to count the number of horizontal connections of length ℓ that a cell at (x_0, y_0) has, we consider cells that are of a horizontal distance ℓ away from it. These cells are located on the circumference of a partial Manhattan circle with center (x_0, y_0) and radius ℓ. A Manhattan circle with center (x_0, y_0) and radius ℓ, where the radius is measured by Manhattan distance ($\ell = |x - x_0| + |y - y_0|$), is a square tilted by $45°$. It is called partial Manhattan circle as only half the cells on the circumference needs to be considered; the other half has already been counted and removed. For a large square gate array, most Manhattan circles are entirely contained within the array except for those whose centers are within distance ℓ from the

boundary. However, due to the symmetrical properties of the Manhattan circle and the gate array, and for the purpose of calculating the expected number of connections between a gate pair, we treat all partial Manhattan circles as contained within the gate array, like the one shown in Figure 3. The error caused by such an approximation is later corrected by a normalization equation (see Equation (14)). We denote the individual gates at the center of the Manhattan circle as set X, the gates within the partial Manhattan circle as set Y, and the gates on the circumference of the partial Manhattan circle as set Z. The numbers of gates in X, Y, and Z are denoted as N_X, N_Y, and N_Z, respectively. Thus,

$$N_X = m; \tag{6}$$

$$N_Y = \sum_{r=1}^{r=l-1} 2mr = m\ell(\ell-1); \tag{7}$$

$$N_Z = 2m\ell. \tag{8}$$

The expected number of connections from set X to set Z is then given by:

$$I(\ell) = \alpha A m^p[(1+\ell(\ell-1))^p - (\ell(\ell-1))^p + (\ell(\ell+1))^p - (1+\ell(\ell+1))^p]. \tag{9}$$

The total number of gate pairs between X and Z are $2m^2\ell$. Therefore, the average number of interconnects connecting each gate pair separated by a horizontal length ℓ in a given partial Manhattan circle is obtained by dividing the number of connections, $I(\ell)$, by the total number of gate pairs, $2m^2\ell$:

$$I_{exp}(\ell) = \frac{\alpha A m^{p-2}}{2\ell}[(1+\ell(\ell-1))^p - (\ell(\ell-1))^p + (\ell(\ell+1))^p - (1+\ell(\ell+1))^p]. \tag{10}$$

Applying binomial expansion, $I_{exp}(\ell)$ can be simplified as follows:

$$I_{exp}(\ell) \cong \alpha A m^{p-2} p(1-p)\ell^{2p-4}. \tag{11}$$

The total number of gate pairs $M(\ell)$ in $\sqrt{\frac{N}{m}} \times \sqrt{\frac{N}{m}}$ square array, separated by a length ℓ is given by:

$$M(\ell) = \begin{cases} m^2(\frac{\ell^3}{3} - 2l^2\sqrt{\frac{N}{m}} + 2\ell\frac{N}{m}), & 1 \le \ell < \sqrt{\frac{N}{m}}; \\ \frac{m^2}{3}(2\sqrt{\frac{N}{m}} - \ell)^3, & \sqrt{\frac{N}{m}} \le \ell \le 2\sqrt{\frac{N}{m}}; \end{cases} \tag{12}$$

where the term m^2 arises from the facts that each cell has m gates, and there are totally m^2 potential gate pairs between two cells.

The horizontal wire-length distribution, $h(\ell)$, is given by multiplying the average number of interconnects connecting each gate pair, $I_{exp}(\ell)$, by the number of gate pairs, $M(\ell)$:

$$h(\ell) = \begin{cases} \Gamma_h \alpha A m^p (1-p) p(\frac{\ell^3}{3} - 2l^2\sqrt{\frac{N}{m}} + 2\ell\frac{N}{m})\ell^{2p-4}, \\ \qquad 1 \le \ell < \sqrt{\frac{N}{m}}; \\ \frac{1}{3}\Gamma_h \alpha A m^p (1-p) p(2\sqrt{\frac{N}{m}} - \ell)^3 \ell^{2p-4}, \\ \qquad \sqrt{\frac{N}{m}} \le \ell \le 2\sqrt{\frac{N}{m}}; \end{cases} \tag{13}$$

where Γ_h is the normalization coefficient that can be determined by the following equation:

$$\sum_{\ell=1}^{\ell=2\sqrt{\frac{N}{m}}} h(\ell) = I_{h\_TOT}. \tag{14}$$

Thus, we obtain the final 3-D circuit horizontal wire-length distribution function, $h(\ell)$, as follows:

$$h(\ell) = \begin{cases} \Theta(\frac{\ell^3}{3} - 2\ell^2\sqrt{\frac{N}{m}} + 2\ell\frac{N}{m})l^{2p-4}, & 1 \le \ell < \sqrt{\frac{N}{m}}; \\ \frac{\Theta}{3}(2\sqrt{\frac{N}{m}} - \ell)^3\ell^{2p-4}, & \sqrt{\frac{N}{m}} \le \ell \le 2\sqrt{\frac{N}{m}}; \end{cases} \tag{15}$$

where

$$\Theta = \frac{\alpha A m^p \frac{N}{m}(1 - (\frac{N}{m})^{p-1})}{-(\frac{N}{m})^p \frac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{\frac{N}{m}}}{2p-1} - \frac{\frac{N}{m}}{p-1}}. \tag{16}$$

If $p = \frac{1}{2}$, applying $l'H\hat{o}spital$'s rule, Θ converges to

$$\Theta = \frac{2\alpha A m^p(\frac{N}{m} - \sqrt{\frac{N}{m}})}{\sqrt{\frac{N}{m}}(-2\ln\frac{N}{m} - 6 + 2\ln 4) + 4\frac{N}{m} - \frac{2}{3}}. \tag{17}$$

Note that when $m = 1$, Equation (15) gives the wire-length distribution of 2-D circuits derived by *Davis et. al.* [13].

2.3 Vertical Wire-Length Distribution

In this subsection, we derive the vertical wire-length distribution. Consider two m-stacked-gate cells P and Q in a homogeneous system as shown in Figure 4. There are a total of m^2 potential gate pairs. Among those m^2 potential gate pairs, m pairs are in the same device layers, $2m-2$ pairs are one device layer apart, $2m-4$ pairs are two device layers apart, and so on. Connections among gate pairs at the same device layers do not go to other device layers and thus do not contribute to the vertical wires. Therefore, only $1 - \frac{1}{m}$ of the total horizontal wires, I_{h_TOT}, is connected with vertical wires. That is, the number of wires consisting of both horizontal wires and vertical wires, I_{v_h}, is

$$\begin{aligned} I_{v\_h} &= (1 - \frac{1}{m})I_{h\_TOT} \\ &= (1 - \frac{1}{m})\alpha A N(m^{p-1} - N^{p-1}). \end{aligned} \tag{18}$$

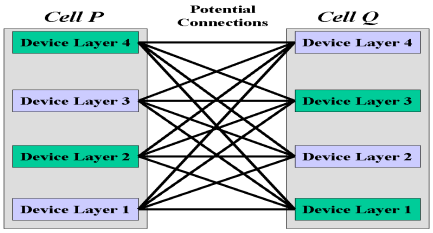

Figure 4: 4-device-layer potential connections between two cells.

The number of wires consisting of both horizontal wires and vertical wires, I_{v_h}, plus the number of wires consisting of only vertical wires, I_{v_0}, is the total number of vertical wires, I_{v_TOT}.

$$\begin{aligned} I_{v\_TOT} &= I_{v\_h} + I_{v\_0} \\ &= \alpha A N(1 - N^{p-1} - m^{p-2} + \frac{N^{p-1}}{m}). \end{aligned} \tag{19}$$

Inspecting Figure 4, the vertical wire-length distribution can be easily obtained:

$$v(k) = \Gamma_v(2m - 2k), \tag{20}$$

where $k = 1, 2, ..., m-1$ is the length of vertical wires in unit of one device layer depth (distance between two neighboring device layers). Γ_v is the normalization coefficient. The normalization is necessary for obtaining the distribution of the entire system since

the expression $(2m - 2k)$ gives only the relative number of wires with vertical length k for m^2 potential connections between two cells. The normalization equation can be written as:

$$\sum_{k=1}^{k=m-1} v(k) = I_{v\_TOT}, \quad (21)$$

Thus, we obtain the final distribution of vertical wires, $v(k)$, of the entire system as:

$$v(k) = \frac{\alpha A N (1 - N^{p-1} - m^{p-2} + m^{-1} N^{p-1})}{m(m-1)} (2m - 2k), \quad (22)$$

where $k = 1, 2, ..., m - 1$.

Note that when $m = 1$, $I_{v\_TOT} = 0$, as 2-D circuits do not have vertical wires.

3. IMPLICATIONS OF WIRE-LENGTH DISTRIBUTIONS

Figure 5 plots the horizontal wire-length distributions with respect to the number of device layers for $m = 1$, 4, 8 and 16, where $m = 1$ corresponds to the 2-dimensional case. We observe that the global interconnects as well as the local interconnects are significantly reduced by 3-D structures. We also observe that there is a higher reduction of horizontal wires when the number of device layers is larger. However, the reduction of horizontal wires is achieved at the expense of vertical wires. 3-D structures reduce the wire length by stacking devices into several smaller device layers instead of spanning them in a single, but large device layer. A connection between two gates can be realized by going through a shortened horizontal wire and a vertical wire. Some nets may go through only vertical wires.

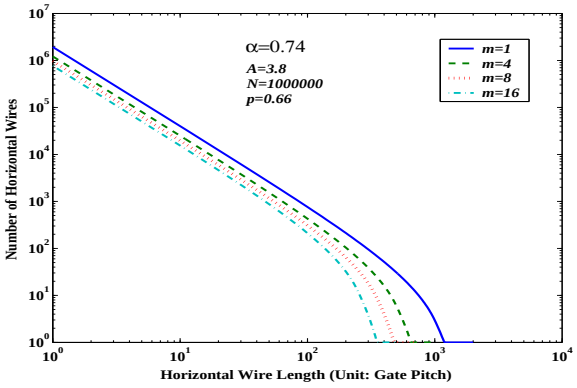

Figure 5: Horizontal wire-length distributions.

Figure 6 plots the vertical wire-length distributions. It shows that even though the number of long vertical wires is relative small, the absolute number of nets spanning long vertical wires is considerably large. The large number of long vertical wires may limit the number of the device layers that can be integrated.

To best understand the effect of the vertical wires, we also plot the percentage of the total wires that contains vertical wires (Figure 7). The percentage rapidly approaches 100% after $m = 8$. The large number of vertical wires will have significant impacts on circuit layout and fabrication process. For circuits with large logic depth, the vertical wires may even impact the performance.

4. 3-D DELAY DISTRIBUTION

To assess the impact of 3-D structures on the circuit performance, we calculate 3-D interconnect delay distribution. To simplify the calculation, we assume that each gate is a two-input NAND gate,

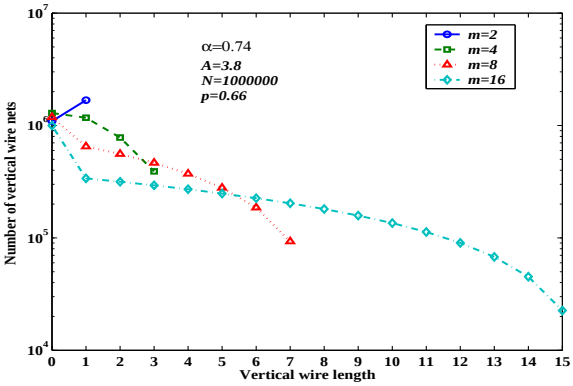

Figure 6: Vertical wire-length distributions.

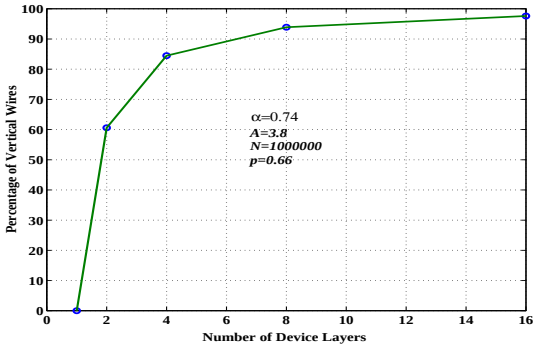

Figure 7: Percentage of wires consisting vertical wires versus number of device layers m.

as shown in Figure 8. Based on transistor density predicted by ITRS and on performance requirements, the sizes of the transistors are estimated to be $W_n/L_n = 10$ and $W_p/L_p = 10$. Also, for a net with both horizontal wire and vertical wire, we assume that the vertical wire is in the middle of the net regardless of the length of the net (Figure 9). We denote the resistance and capacitance of a horizontal wire with one gate pitch as R and C, respectively; and denote the resistance and capacitance as $Rv*R$ and $Cv*C$, respectively for a vertical wire with one device layer depth, where Rv and Cv are the coefficients that relate the resistances and capacitances of vertical wires and horizontal wires. The distributions are plotted under the assumption that tungsten plugs are used as vertical channels; Rv and Cv are estimated to be 10 and 0.85, respectively.

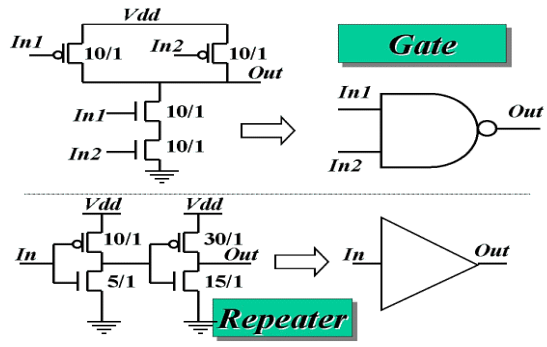

Figure 8: 2-input NAND gate and repeater.

Table 1 lists the device and interconnect parameters for $180nm$ technology node identified by ITRS [1]. Base on these data, the

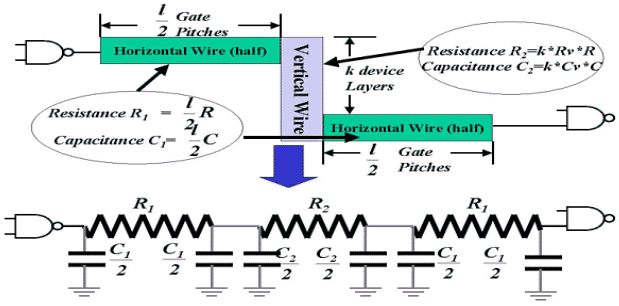

Figure 9: 3-D wire and its circuit model.

Table 1: Device and Interconnect Parameters at 180nm Technology Node

Parameter	Value
Assumed	
Transistor count	22M
Average gate fanout	3
Minimum gate length, L_n, $L_p(nm)$	140
nMOSFET switching resistance, $W_n R_{swn}(\Omega - \mu m)$	2400
Input capacitance, $C_{in}/(W_n + W_p)(fF/\mu m)$	2.54
Output capacitance, $C_{out}/(W_n + W_p)(fF/\mu m)$	2.04
Horizontal interconnect resistance, $\rho(\Omega - cm)$	3.3
Horizontal interconnect capacitance, $C_w^h(fF/\mu m)$	0.2
Length of one gate pitch, (μm)	9
Width of the wires, $2L_n(nm)$	280
Wire aspect ratio	2.2
Derived	
Gate switching resistance, $R_t(\Omega)$	1714
Gate input capacitance, $C_{in\_t}(fF)$	7.112
Gate output capacitance, $C_{out\_t}(fF)$	5.712
Horizontal wire resistance per gate pitch, $R(\Omega)$	1.719
Horizontal wire capacitance per gate pitch, $C(fF)$	1.8
Vertical wire resistance per device layer depth Ω	17.19
Vertical wire capacitance per device layer depth fF	1.53

impact of 3-D integration on circuit performance is investigated using the Elmore delay model [10].

Figure 10 plots the delay distributions with respect to the number of device layers for $m = 1$, 4, 8, and 16 ($m = 1$ corresponds to the 2-D case). Clearly we see that every 3-D delay distribution shows two distinct regions compared to 2-D distribution (solid line). We refer to the region that contains the short-delay nets as local region; and refer the region that contains the long-delay nets as the global region.

We observe that as the number of device layers increases, the range of the local region increases and the range of the global region decreases. Two factors contribute to this scenario. First, with more device layers, more long-delay nets in 2-D are reduced and converted into short-delay nets in 3-D. Thus, the local region is enlarged. The increase of nets in the local region compensates for the decrease of nets in the global region so that the conservation of total nets is maintained. We can therefore conclude that 3-D structures effectively reduce the long-delay nets to achieve high performance. Second, the influence of vertical wires is more pronounced with the increasing number of device layers and may even turn the short delay nets in 2-D to moderate delay nets in 3-D. When the contribution of vertical wires is significant enough, the local region may even be further extended and may completely cancel the benefit brought by 3-D structures. This again implies that vertical wires may limit the number of the device layers that can be integrated.

The detrimental effect of vertical wires on short interconnections

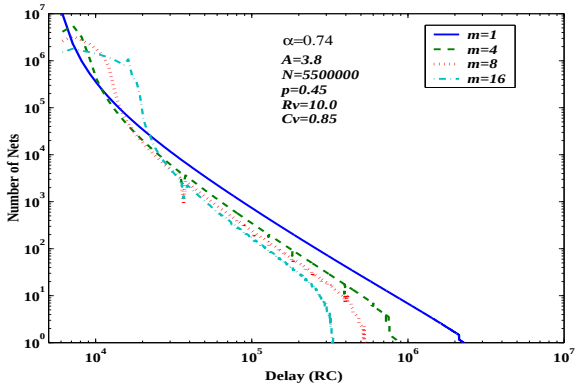

Figure 10: Delay distributions for various numbers of device layers.

can be further observed from Figure 11, where the delay distributions with respect to different vertical wire resistance and capacitance normalization coefficients is plotted. For comparison purposes, 2-dimensional distribution is also included. Figure 11 shows that the resistance and capacitance of vertical wires have almost no impact on long delay nets. However, as the resistance and capacitance of the vertical wires increase, the number of short-delay nets increases.

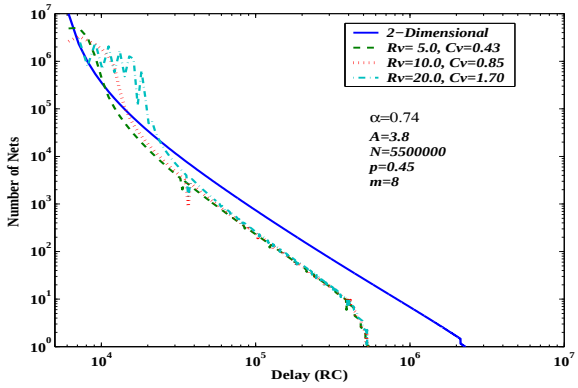

Figure 11: Delay distributions for various vertical wire resistances and capacitances.

5. REPEATER INSERTION AND CIRCUIT PERFORMANCE

When the resistance of the interconnection is comparable to or larger than the on-resistance of the driver, the propagation delay increases quadratically with respect to the interconnection length. With judicious insertion of repeaters, the delay becomes linear [10; 15]. In this subsection, we investigate the impact of 3-D structures on repeater insertion.

To simplify the calculation, we assume that all repeaters are identical. Each repeater is implemented by cascading two inverters. The circuit structure and transistor sizing of repeaters are shown in Figure 8. We use the results in [10; 15] to determine the number of repeaters required to minimize delay.

Figure 12 plots the number of repeaters needed to minimize the interconnect delay as much as possible with respect to the number of device layers for $m = 1$, 2, 4, 8, and 16. From the plot, we see that the number of repeaters is significantly reduced in 3-D structures. This is especially important for circuits with high interconnect complexity (interconnect complexity is described by Rent's constant p — higher p corresponds to higher complexity with more

global nets). For example, for $p = 0.80$, a 2-D layout needs about 30 repeaters every hundred gates, which is unacceptably high. With 8-device-layer integration, the number of repeaters can be reduced to 9 per hundred gates, and only 5 for $m = 16$. Figure 12 shows that 3-D structures significantly relieve the difficulty of placement and routing due to repeater insertion. Moreover, reducing the number of repeaters will further reduce the chip area and increase the integration density.

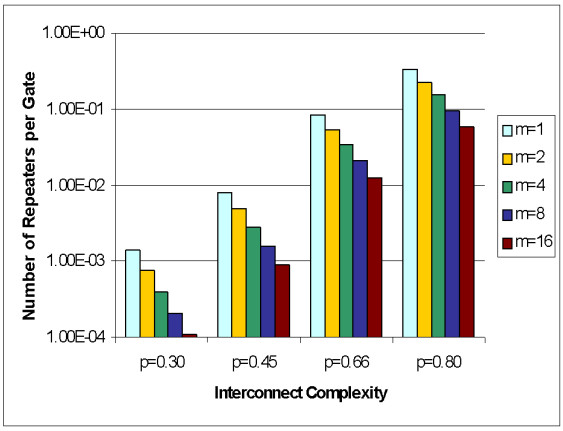

Figure 12: Number of repeaters with respect to the number of device layers.

In addition, even with a much larger number of repeaters inserted, 2-D circuits are still not able to achieve the same performance of 3-D. Figure 13 plots the worst case clock frequency versus different 3-D circuits. Here, we assume that the worst case clock period is proportional to the longest delay net after repeater insertion. For comparison, we normalize them with respect to the 2-D case at $p = 0.30$. 3-D circuits show significant performance improvement. Most of them can be clocked at rates double or even triple those of 2-D. From the plot, we observe that higher p indeed corresponds to higher interconnect complexity, which has longer delay, thus lower clock rate. Therefore, it can be a good option for high interconnect complexity circuits to adopt 3-D integration to improve the performance.

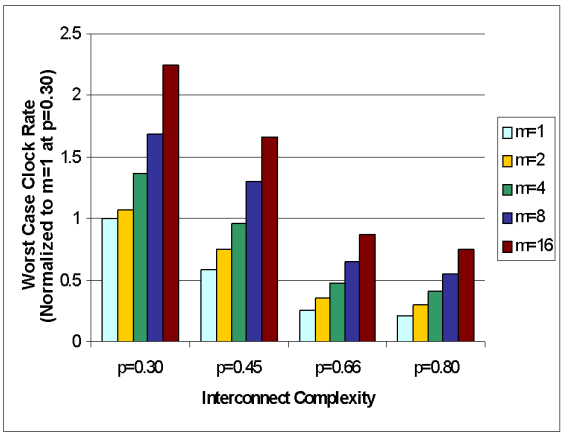

Figure 13: Worst case clock rate.

6. CONCLUSIONS

We divide the 3-D wires into horizontal parts and vertical parts. The closed form expressions for horizontal and vertical wire-length distributions are derived. We show that 3-D structures significantly reduce the global wires. However, we pay the penalty of increasing the number of vertical wires. The large number of vertical wires may impact the integration density, chip size, and circuit performance.

Based on wire-length distributions, we further study 3-D circuit delay distribution and repeater insertion. 3-D structures effectively reduce the long-delay nets, and improve the circuit performance. The increasing number of device layers would reduce the long-delay nets more, but would also turn the short-delay nets into longer delay nets. This may set a ceiling on how many device layers we can integrate. We also show that 3-D structures significantly reduce the repeaters needed to minimize the interconnect delay; such a reduction not only saves the chip area and increases the integration density, but also relieves the difficulty of pre-layout chip size estimation and layout floor planning. Finally, we show that with 3-D structures, circuits can work at much higher clock frequencies than with 2-D.

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