

Panel: When Bad Things Happen To Good Chips

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Abstract

Design of reliable chips with high yield is an extremely challenging task in UDSM technologies. Time to market pressures, which often limit the necessary verification before tape-out, typically are manifested as ramp-to-production problems on "good" designs either in the manufacturing process or in the field. Burn-in process, a reactive measure to ship reliable chips, is not effective for high volume designs. Another cause for concern is hidden failures that go undetected due to incompleteness of test vectors.

This session begins with an embedded tutorial that examines a number of "bad things that can happen to good chips" both during manufacturing and in the field. The concept of "design marginality" which can significantly affect manufacturing yield, the proximity to the "cliffs" in chip operation, and test escapes that could cause failures in the field are discussed. Then the panel, from different perspectives on yield and reliability challenges, will describe their own real-world experiences, and discuss how these challenges could be addressed in the manufacturing process, design, and EDA.

Andrzej Strojwas
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Embedded Tutorial: Yield and Reliability Challenges in Designing "Good" Chips

Achieving high yield and reliability of the complex products in the leading edge technology is an extremely challenging task. The time to market windows are so small that there is an enormous pressure on squeezing the necessary verification prior to tape-out. Moreover, the physical limits of technology in terms of device dimensions (both lateral and vertical) are pushed extremely hard and this causes many concerns in terms of both yield and reliability. Hence, a thoroughly designed and verified "good chip" may "go bad" either in the manufacturing process or after it has been installed in a system.

This tutorial will examine a number of "bad things that can happen to good chips". We will start by defining a good chip design in terms of its manufacturability and immunity to environmental factors in the system operation. Then, we will describe in more detail the "dangers in the fabrication process" such as, for example, Plasma Induced Damage (PID) or stress build-up. We will also present the concept of "design marginality" which can significantly affect manufacturing yield and also the proximity to the "cliffs" in chip operation.

We will then describe the testability issues that are a very serious concern. We will talk about the difficulties of complete verification in die sort and final test (test escapes) as well as the difficulties of mimicking the realistic chip operation in a system. Finally, we will very briefly introduce key reliability concerns that will be the focus of this panel discussion.

Position Statements

Sani R. Nassif, IBM

Design for yield is hard because (a) The fab can give you only approximations of chip-to-chip variability and wild guesses at within-chip variability which radically limits our ability to predict and null-out the impact of these variations and therefore causes a design that is either too conservative or overly sensitive; and (b) the performance analyses we are capable of performing (e.g. circuit simulation for small blocks, static timing analysis for the whole chip) are not enabled to provide accurate measurement of variability impact. Detailed low-level simulation misses the environmental interactions and efficient high-level simulation uses models that are currently too abstract to be effective variability bellwethers.

The EDA community needs to create simulation and modeling methodologies that are cognizant of the presence of variability. The accuracy of the simulation and the magnitude of the variability have to be carefully balanced at each level in order to match designer expectations and needs. If we accept the fact that complete chips are not going to run in Spice, but in some form of static analyzer, we immediately run up against the excessively simple models used at that level. Some research and tool effort in this particular area has the best potential of enabling DFY for today's large high performance designs.

Ray Hokinson, Compaq

Design reliability can only be assured through design methodology and CAD solutions. Post fabrication test and burn-in stress are costly and inefficient to accelerate chip wear out mechanisms. Reliability verification on a near complete design forces competition for engineering and computer resources with other critical design tasks. Detecting problems late in the design cycle may lead to a partial or non-ideal solution. Backend verification on large designs is getting too expensive (people and time) with arguably questionable return.

The delineation between an electrical design issue and a reliability design issue is getting vague. Many reliability issues can be considered as speed/race, coupling or noise margin issues. The inclusion of reliability wear out checks along with standard electrical verification would remove resource bottlenecks and reduce excessive design margins now in place to address reliability uncertainties. More Correct by Design, both performance and reliability, is the lofty goal.. CAD tools that stress ease of use, accuracy and reliability integration is the best way forward.

Tak Young, Monterey Design

Voltage drop and electromigration problems were found more than five years ago with designs using 0.7 micron technology. With the deep submicron technologies of 0.18 micron and below, many reliability effects which are related to manufacturing effects (e.g.

electromigration, channel hot carrier, gate oxide integrity, antennae) or yield (e.g. voltage drop, cross-talk) have become critical. Many verification tools are being developed by EDA companies. The models and algorithms implemented with the verification tools are very important for the understanding and identification of the effects. However, identification at the post-layout stage is too late for the designs to meet the time to market pressure. Solutions are required with EDA design tools.

Higher level models or design guidelines will need to be developed in order for the effects to be accounted for in the design tools. The reliability engineers, IC designers and EDA developers need to work together as a team. This will probably require a change in the business model of the working relationship between the foundry, design and tools companies. The establishment of the Design-In-Reliability group by Sematech is a good start. The classification of the different reliability effects will help the communications among the different disciplines. We now need to establish the means to fund projects within the EDA companies with active participation from reliability engineers and design engineers.

Wonjae L. Kang, Intel

Chip designs are continuously getting larger and more complex. Risks to potential reliability problems are growing rapidly as the complexity increases. Traditional approaches of manual verification and conservative design styles are no longer acceptable in dealing with present and future chip reliability problems. Also, product reliability stresses are becoming more difficult and costly to catch problems. The most important area for chip reliability is enabling chip design groups to perform Designing-In-Reliability (DIR) during the design requires CAD tools. The gaps have been increasingly noticeable as more companies are investing more resource to develop internal solutions to address the reliability issues in the design phase. Few key issues are achieving meaningful Correct-By-Construction and having key reliability point solutions such as dealing with voltage coupling and hot carrier tools. Emerging reliability issues also require automation through CAD tools. Analysis performed by the Sematech DIR team highlights low maturity levels and huge gaps of DIR tool capabilities. These tool capability gaps are expected to be larger with every generation of technologies and chip designs. Semiconductor

companies are spending significant resources in developing internal solutions that could be implemented in the EDA tools instead. Collaborations between EDA companies and semiconductor companies are needed. Developing generic data/tool interface for DIR and DIR point solutions is critical to the future of chip industry.

David Overhauser, Simplex Solutions Inc.

Designers with high-speed chip design experience understand the reliability and yield issues much better than those with background in low-speed chip design. High-speed chip design teams have reliability and yield issues as active portions of the design process. Low-speed chip designs traditionally had these issues met inherently by methodology. As more chips increase in size and speed, they begin to cross the line where reliability and yield must move from inherently addressed to overt design issues. Many designers crossing this threshold are unaware of the new risks to which they are exposed. Some design managers are aware of the risks, but do not perform analysis using existing EDA tools due to fear of finding a problem and delaying their tapeout. Until reliability and yield become overt design requirements for all designs the rate of good chips going bad will increase unnecessarily.

Steve Kang University of Illinois, Urbana-Champaign

With increasing complexity of integration, the concern for chip-level reliability has been rising steadily. In order to help achieve development of reliable VLSI chips and systems, more physical analysis is essential and thus CAD capability needs to be expanded to encompass reliability verification. One of the most important factors in VLSI reliability is temperature effect and thus electrothermal analysis has become critically important for evaluation of ESD, EM, timing failures among others. In my talk I will provide some elaborations on these issues along with introduction of new CAD tools and their application to industry products.