A Realizable Driving Point Model for On-Chip Interconnect with Inductance

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Abstract: For improved efficiency, static timing analyzers represent the interconnect driving point with a reduced order model so that the gate and interconnect delays can be calculated separately. Traditionally, the pi-circuit has been used to model the driving point of RC interconnect. As process technologies have improved, it has become necessary to include on-chip inductance during the timing analysis of high performance designs. However, the pi-model breaks down for interconnect with inductance. In this paper, we discuss the behavior of RC and RLC one ports in a circuit theoretic framework and characterize when the pi-model is not synthesizable for RLC circuits. We then present a synthesis procedure for RLC circuits that guarantees a realizable reduced order circuit using the first four moments of the input admittance. We demonstrate the efficacy of the proposed model for on-chip RLC interconnect with several examples. We see the proposed model serving the same purpose for RLC circuits that the pi-model did for RC circuits.

I. INTRODUCTION

It has been well established that interconnect effects must be accounted for to ensure accurate static timing analysis. Traditionally, gate level static timing analyzers have broken down the path delay as the sum of the gate delay and the wire or interconnect delay. Since the interconnect is a linear circuit, model order reduction techniques based on moment matching, such as [11, 6], have been employed to compute its delay efficiently. However, since gates are non-linear devices, two distinct approaches have been used for fast computation of gate delay: 1) The gate delay is precharacterized in terms of input transition time and output load capacitance using detailed circuit simulators such as SPICE [8] and implemented using lookup-tables, or 2) The gate delay is obtained "on the fly" using fast timing simulators such as [14],[4].

Regardless of the method used to compute gate delays, an accurate characterization of the loading due to the interconnect at the output of the gate must be made. While a simple approach would be to lump the total capacitance of the interconnect at the output of the gate, the resistive shielding renders such a model inaccurate. O'Brien and Savarino [9] presented a more accurate model for RC interconnect, the so called pi-model (see Fig. 1), that has been used in many timing analysis and physical design tools for modeling the driving point load. However, the pi-model can no longer be used if the inductive effects are significant; and with faster signal transition times, increasing die sizes, and the advent of newer materials such as copper, on-chip inductance can no longer be ignored [3]. In this paper, we present a new driving point model, similar in spirit to the RC pi-model, for on-chip interconnect wires with inductance. Our model is valid provided there is no DC path to ground and the interconnect is relatively damped, a reasonable assumption for on-chip interconnect.

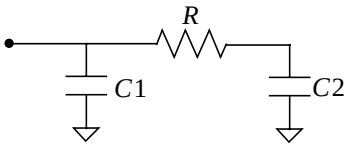


Fig. 1. The pi-model

For precharacterized gates, however, we still need to map the driving point model to an "effective" capacitance value so that the lookup-tables can continue to be used without modification. The effective capacitance methodology for RC interconnects introduced in [12] has been extended to RLC interconnects by Arunachalam et al in [2]. This approach avoids the synthesis dilemma by modeling the driving point with a reduced order pole-residue approximation, obtained from the moments of the input admittance of the interconnect. While the method is effective, the lack of a circuit model makes the procedure expensive since a Padé approximation has to be performed in the inner loop of the C_{eff} iteration.

In addition to improved efficiency, there are other compelling reasons for a circuit model to be used in the C_{eff} calculation. While the issues of stability and passivity that have plagued Padè approximations have been recently overcome with more advanced methods [10], the circuits realized from these techniques are complicated. They contain controlled sources which must be stamped into the MNA matrices of a SPICE-like simulator. In contrast, the synthesis method described in this paper works directly off the first few moments of the input impedance, does not require any controlled sources or transformers, and is simple to implement. Besides, our circuit model also provides some degree of intuition in terms of inductive and resistive shielding, something that a complicated model fails to do. As we demonstrate with numerous examples in the paper, matching the first few moments is sufficient for typical on-chip interconnect.

DAC 2000, Los Angeles, California

We note that the driving point synthesis for RLC(M)[1] circuits has been studied earlier by Brune, Bott-Duffin and others [15]. Brune's synthesis method assumes that the input impedance is known in the form of a rational function. While conceptually simple, his method requires the use of transformers to guarantee positive elements, something that is not practical for realizing on-chip circuits. Bott-Duffin's method, on the other hand, avoids the use of transformers, but a stiff price is paid in the number of components required. This method is therefore largely of a theoretical interest.

This paper is organized into five sections as follows. In the next section, we provide the circuit theoretic background that shows why the pi-model is realizable for RC circuits and when it breaks down for RLC circuits. In Section 3, we present the procedure to derive a realizable reduced order model for RLC circuits. In Section 4, we present experimental results that show the effectiveness of the proposed model. Finally, we conclude and summarize the paper in Section 5.

II. THEORETICAL CONSIDERATIONS

Suppose that $Y(s)$, the input admittance of the interconnect loading the driver, can be expanded about $s = 0$ as follows:

$$Y(s) = y_1 s + y_2 s^2 + y_3 s^3 + y_5 s^4 + \ldots \quad (1)$$

The coefficients $y_1, y_2, \ldots$ are the moments of $Y(s)$. Efficient computation of moments has been described in [11] and therefore will not be considered in this paper. Note that $y_0 = 0$ if there is no DC path to ground, a condition we will assume in the rest of the paper. By matching the first three non-zero moments of the admittance of the original interconnect with the pi-circuit shown in Fig. 1, O'Brien and Savarino [9] derived the formulas for synthesizing the element values of the pi-circuit using the first three moments of $Y(s)$. While not explicitly stated in their paper, it can be shown [15] that the first three admittance moments of general RC circuits satisfy:

$$y_1 > 0, y_2 < 0, y_3 > 0 \quad (2)$$

$$y_1 y_3 - y_2^2 > 0 \quad (3)$$

This in turn guarantees the realizability of the pi-model for RC circuits. However, as we show later in this section, while $y_1 > 0$ and $y_2 < 0$ do hold for RLC circuits, nothing can be said about the sign of y_3 and the inequality (3) which depend on the inductance in the circuit. Thus, the pi-model may be *unsynthesizable* even if the line is mildly inductive.

To facilitate the subsequent development, we shall center our arguments around the input impedance, $Z(s) = \frac{1}{Y(s)}$.

1. M stands for mutual inductance which we do not consider in this paper.

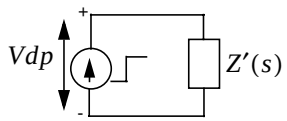


Fig. 2. Determining the sign of z_0

$Z(s)$ can also be written in terms of moments as:

$$Z(s) = \frac{z_{-1}}{s} + z_0 + z_1 s + z_2 s^2 + \ldots \quad (4)$$

The moments of $Z(s)$ are related to those of $Y(s)$ by:

$$z_{-1} = \frac{1}{y_1} \quad (5)$$

$$z_0 = -\frac{y_2}{y_1^2} \quad (6)$$

$$z_1 = \frac{y_2^2 - y_1 y_3}{y_1^3} \quad (7)$$

Since the interconnect is modeled with a lumped, passive RLC circuit, $Z(s)$ satisfies a necessary and sufficient condition, known as the Positive Real (PR) property, stated in the following two equivalent forms [15]:

- $Z(s)$ is a rational function of s with real coefficients so that $Z(s)$ is real when s is real.
- $Re[Z(s)] \geq 0$ if $Re[s] \geq 0$.

Or,

- $Z(s)$ is a rational function of s with real coefficients so that $Z(s)$ is real when s is real.
- For all real w, $Re[Z(jw)] \geq 0$
- All poles of $Z(s)$ are in the closed Left Half Plane (LHP) of the s plane i.e. inside the LHP or on the jw-axis. All jw-axis poles are simple with positive real residues.

Since there is no DC path to ground, $Z(s)$ has a pole at the origin and is of the form:

$$Z(s) = \frac{a_0 + a_1 s + \ldots + a_n s^n}{s(1 + b_1 s + \ldots + b_m s^m)} \quad (8)$$

where $n \leq m$. Separating out the pole at origin, we have:

$$Z(s) = \frac{a_1 + a_2 s + \ldots + a_n s^{n-1} - a_0 b_1 - a_0 b_2 s - \ldots - a_0 b_m s^{m-1}}{1 + b_1 s + \ldots + b_m s^m} + \frac{a_0}{s} \quad (9)$$

$$Z(s) = \frac{a_0}{s} + Z'(s) \quad (10)$$

The PR property assures us that $a_0 > 0$ thus implying $z_{-1} > 0$. As we show next, $Z'(s)$ satisfies the PR property since $Z(s)$ satisfies the PR property. From eq. (9), it is clear

that $Z'(s)$ is a rational function of s that is real when s is real. Next, $Re[Z(jw)] = Re[Z'(jw)]$. Since, for all real w, $Re[Z(jw)] \geq 0$, this implies that $Re[Z'(jw)] \geq 0$. Finally, note that $Z(s)$ can be written as:

$$Z(s) = \frac{k_0}{s} + \sum \frac{k_i}{(s - p_i)} = \frac{a_0}{s} + Z'(s) \tag{11}$$

where $a_0 = k_0$ and k_i, p_i could be complex. Note that all the poles and residues of $Z'(s)$ are the same as the poles and residues of $Z(s)$, except the pole at the origin. Therefore, we can say that all poles of $Z'(s)$ are in the closed Left Half Plane (LHP) of the s plane i.e. inside the LHP or on the jw-axis. All jw-axis poles are simple with positive real residues. As a result, $Z'(s)$ also satisfies the PR property.

Since the PR property is both a necessary and sufficient condition for the realization using lumped RLC(M) elements, $Z'(s)$ is the input impedance of some passive circuit. This observation in fact ensures that z_0 is also positive. Consider a step current source driving $Z'(s)$ as shown in Fig. 2. The voltage at the driving point is given by:

$$V_{dp}(s) = \frac{z_0}{s} + z_1 s + \ldots \tag{12}$$

Applying the Final Value Theorem, the final value of V_{dp} turns out to be z_0 which must be positive since $Z'(s)$ is passive. In fact, this is no surprise since the y_1 and y_2 moments of $Y(s)$ are independent of any inductance in the circuit. That is, even for RLC circuits, y_1 and y_2 behave as if the interconnect was a pure RC circuit. This makes $y_1 > 0$ and $y_2 < 0$ and therefore $(z_0 = -y_2/y_1^2) > 0$.

To get a better feel for the above fact and to reason about the signs of z_1 and z_2, we now derive explicit expressions for the first three moments of $Z(s)$ for an arbitrary RLC tree. Consider a general RLC tree being driven by a voltage source. We assume that the only capacitors in the circuit are capacitors to ground and that there is no DC path to ground. If $Y(s)$ is the input admittance of the tree and $V(s)$ is the input voltage source, we have:

$$\begin{aligned} Y(s)V(s) = I(s) &= s\sum_{i=1}^{n} C_i V_i \\ &= s\sum_{i=1}^{n} C_i\left[V(s) - s\sum_{j=1}^{n}(R_{ji} + sL_{ji})C_j V_j\right] \end{aligned} \tag{13}$$

where $(R_{ji} + sL_{ji})$ is the total impedance of a path common to i and j, as defined in [13].

$$Y(s) = s\sum_{i=1}^{n} C_i\left[1 - s\sum_{j=1}^{n}(R_{ji} + sL_{ji})C_j H_j\right] \tag{14}$$

where H_j is the transfer function of the j^{th} node. Expanding $Y(s)$ in powers of s and matching like powers we get $y_0 = 0$ and the next three moments as:

$$y_1 = \sum_{i=1}^{n} C_i \tag{15}$$

$$y_2 = -\sum_{i=1}^{n} C_i\left(\sum_{j=1}^{n} R_{ji}C_j\right) \tag{16}$$

$$y_3 = \sum_{i=1}^{n} C_i\left(\sum_{j=1}^{n} R_{ji}C_j m_j^{(1)}\right) - \sum_{i=1}^{n} C_i\left(\sum_{j=1}^{n} L_{ji}C_j\right) \tag{17}$$

where $m_j^{(1)}$ is the first moment (Elmore delay) of H_j and is given by:

$$m_j^{(1)} = \sum_{k=1}^{n} R_{kj}C_k \tag{18}$$

This analysis clearly shows that: the first two moments of $Y(s)$ are independent of L, the first moment is positive and the second is negative thereby implying $z_{-1} > 0$ and $z_0 > 0$, and that y_3 though initially positive, becomes negative when the inductive effects start dominating. It is clear from eq (17) and (7) that though z_1 is negative for small values of interconnect inductance, if we increase the inductance (or decrease the resistance) in all the branches of the tree, it becomes positive and stays positive. *Note that by virtue of inequality (3), a pi-circuit can not be synthesized when* $z_1 > 0$.

To summarize, while we know the signs of z_{-1} and z_0, we cannot say much about the signs of z_1, z_2 etc.[1] However, as the inductance starts dominating the resistance in the circuit, z_1 becomes positive, and z_2 which was positive for RC circuits, becomes negative. In the limiting case, when the interconnect reduces to a pure LC circuit, all the even-numbered moments $z_0, z_2, \ldots$ become zero and the odd-numbered moments alternate in sign with z_1 being positive. Any reduced order synthesis method, using the first four moments should, therefore, produce a realizable circuit for the four possible sign combinations of z_1 and z_2. We shall describe one such method in the next section.

III. SYNTHESIZING THE *RLC* DRIVING POINT MODEL

Consider the expansion of $Z(s)$ into the first four moments:

$$Z(s) = \frac{z_{-1}}{s} + z_0 + z_1 s + z_2 s^2 = Z_a(s) + Z_b(s) \tag{19}$$

where $Z_a(s) = \frac{z_{-1}}{s} + z_0$ and $Z_b(s) = z_1 s + z_2 s^2$. $Z_a(s)$ can be realized as a resistance in series with a capacitance. Suppose $Y_b(s) = \frac{y_{b0}}{s} + y_{b1} + \ldots = \frac{1}{Z_b(s)}$. Cross multi-

1. Note that $z_2 = (-z_1 y_2 - z_0 y_3 - z_{-1} y_4)/y_1$.

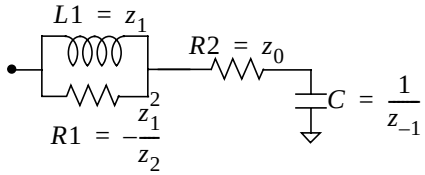


Fig. 3. One possible reduced order circuit if $z_1 > 0$ and $z_2 < 0$

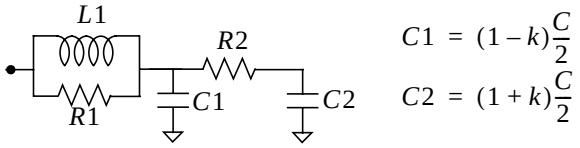


Fig. 4. A realizable reduced order circuit for all four sign combinations

plying and equating the like powers, we get $y_{b0} = 1/z_1$ and $y_{b1} = -z_2/z_1^2$. Thus, $Z(s)$ can be implemented as Fig. 3 by matching the first four moments with the original interconnect circuit. However, while $R2$ and C are guaranteed positive, for $L1 > 0$ and $R1 > 0$ we must have $z_1 > 0$ and $z_2 < 0$ which as we saw in the previous section cannot be guaranteed for RLC circuits.

However, if we modify the reduced-order circuit to the one shown in Fig. 4, then realizability is assured regardless of the signs of z_1 and z_2. Although we are still matching four moments, by introducing a fifth parameter, k - the realizability parameter introduced in [5] - we have acquired the added flexibility in assigning positive values to the elements of the reduced order circuit. Note that $-1 < k \le 1$ since $C1 > 0$ and $C2 > 0$. For $k = 1$, this circuit reduces to the one shown in Fig. 3. As in [5], k provides us with a family of circuits all having the same topology and matching the same number of moments. This enables us to choose a particular circuit by assigning an appropriate value to k, based on the signs of z_1 and z_2.

The first four moments of the reduced order circuit in Fig. 4. are given by:

$$z_{-1} = \frac{1}{C} \tag{20}$$

$$z_0 = \frac{(1+k)^2 R2}{4} \tag{21}$$

$$z_1 = L1 - \frac{1}{16} C(1-k)(1+k)^3 R2^2 \tag{22}$$

$$z_2 = \frac{1}{64} C^2 (1-k)^2 (1+k)^4 R2^3 - \frac{L1^2}{R1} \tag{23}$$

To ensure $L1 > 0$, using eq. (21) and (22), we obtain:

$$x > -\frac{z_1}{C z_0^2} \tag{24}$$

Table 3-1: Choosing the value of x

z_1	z_2	x
>0	<0	Any positive real x. We arbitrarily set $x = 0$
>0	>0	$x > \sqrt{z_2/(z_0^3 C^2)}$
<0	<0	$x > -z_1/(C z_0^2)$
<0	>0	$x > max(-z_1/(C z_0^2), \sqrt{z_2/(z_0^3 C^2)})$

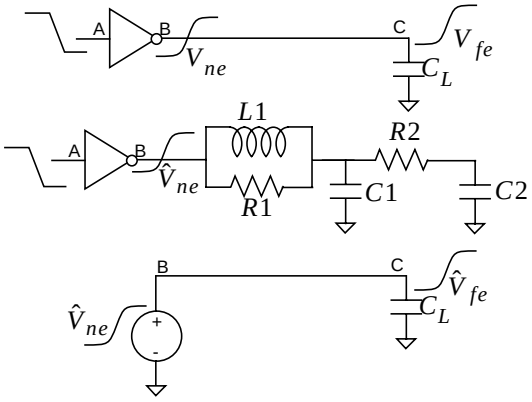


Fig. 5. Comparing V_{ne} with $\hat{V}_{ne}$ and V_{fe} with $\hat{V}_{fe}$ in experiments

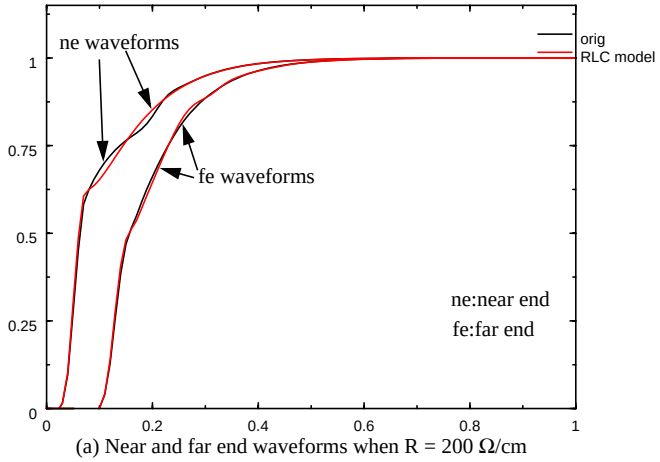
where $x = (1-k)/(1+k)$. Note that $-1 < k \le 1$ implies $0 \le x < \infty$ with $x = 0$ when $k = 1$ and $x \to \infty$ as $k \to -1$. Similarly, to ensure $R1 > 0$, we obtain:

$$z_0^3 C^2 x^2 - z_2 > 0 \tag{25}$$

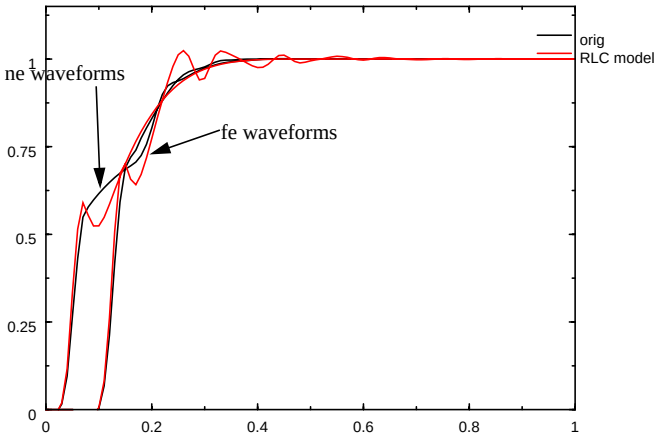
Now consider all the possible sign combinations of z_1 and z_2 and the constraints they place on the value of x as summarized in Table 3-1. When $z_1 > 0$ and $z_2 < 0$, eq. (24) and (25) are satisfied for any positive real x. When this case occurs, we choose $x = 0$ (which corresponds to $k = 1$) and our reduced order circuit reduces to the one shown in Fig. 3. When $z_1 > 0$ and $z_2 > 0$, eq. (24) is still satisfied; however, satisfying eq. (25) requires that some of the total capacitance C be moved from capacitor $C2$ to $C1$. For the remaining two sign combinations, $z_1 < 0$ and one can therefore either synthesize an RC pi-circuit (which matches the first three moments) or the circuit shown in Fig. 4 (which matches the first four moments). For all the other cases when the pi-model is not synthesizable, the driving point waveform when the driver is loaded by the circuit in Fig. 4 matches well with the driving point waveform when the driver is loaded by the original interconnect.

IV. EXPERIMENTAL RESULTS

In the following, we compare the driving point waveforms



(a) Near and far end waveforms when R = 200 Ω/cm



(c) Near and far end waveforms when R = 100 Ω/cm

Fig. 6. A 5mm uniform RLC line with varying resistance

predicted by our model with the driving point waveform when the original interconnect is present at the output of the driver. We also compare the far-end (sink) response when the interconnect is driven by the actual waveform (produced when the original interconnect loads the driver) at the driving point and when the interconnect is driven by the waveform produced when our model loads the driver (see Fig. 5). This is done to illustrate the fact that even if the near end waveform does not capture all the details of the true near end waveform, it does not impact the far end response significantly. In each example, ASX [1], a commercial SPICE-like circuit simulator was used. The interconnect and driver parameters were taken from a representative high-performance, commercial microprocessor process. We used Table 3-1 to choose the value of k to synthesize the reduced order circuit. Unless otherwise noted, interconnects were modeled by lumped RLC elements with 10 segments representing a 1 mm wire, where each segment is made of R, L and a C to ground and the buffer driving the interconnect was driven by a ramp signal having a 50ps transition time. We present the plots in terms of normalized time (the x-axis) and normalized voltage (the y-axis). In all of the following examples, the pi-model was not synthesizable.

In Fig. 6, we show the driving point waveforms when a 5 mm uniform line of varying resistance (200 and 100 Ω/cm) is driven by a buffer. The inductance and capacitance were 6.44 nH/cm and 3.28 pF/cm respectively. The buffer was sized to provide satisfactory source termination when the line resistance went to zero. In Fig. 6(a), when line resistance was 200 Ω/cm, our model agrees well with the interconnect waveform at both the near and the far ends. However, when the line resistance was reduced to 100 Ω/cm our reduced order model deviated significantly from the interconnect waveform at the near end. The source of this error is the inability of the reduced order model to capture time-of-flight effects. This shows that as the inductive effects start to dominate, four moments are no longer sufficient. This also shows

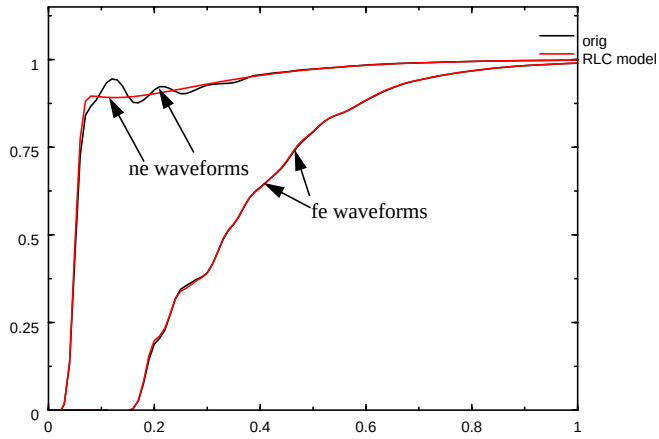


Fig. 7. Near and far end waveforms for an asymmetric RLC tree

that a low-order model such as ours is unsuitable for modeling the driving point of very low-loss interconnects like those found in MCMs and PCBs.

In Fig. 7, we show the waveforms for an asymmetric tree with 9 sinks. The closest sink was 1.5 mm from the driver and the farthest sink was 9 mm away. There were a total of 285 elements in the tree. The R, L, and C values were randomly varied between 50-100 Ω/cm, 5-7 nH/cm, and 3-4 pF/cm, respectively. The far-end waveform shown corresponds to the sink that was 9 mm away from source. It is clear from the figure that even though our model does not capture all of the details of the driving point waveform, the far end waveforms are indistinguishable.

In Fig. 8, we show the waveforms for a daisy-chain like topology with four sinks. The nearest sink was 3 mm away and the farthest sink was 6.5 mm away. The R, L, and C values were randomly varied between 50-100 Ω/cm, 5-7 nH/cm, and 3-4 pF/cm. Clearly, the driving point waveform due to the reduced order model captures the essential characteristics of the actual waveform. We also show the waveforms at the sink that was 6.5 mm away.

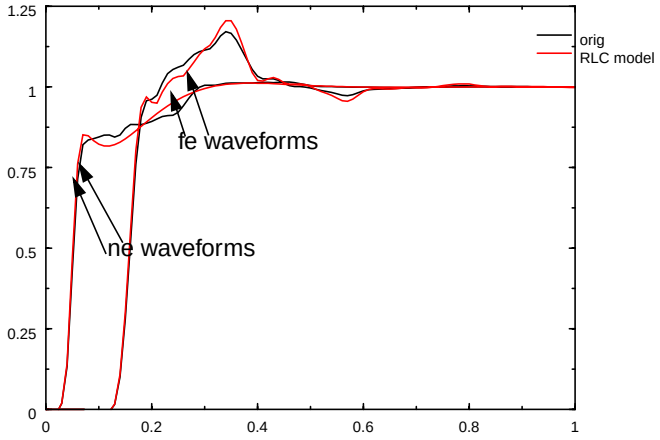


Fig. 8. Near and far end waveforms for an RLC daisy-chain topology

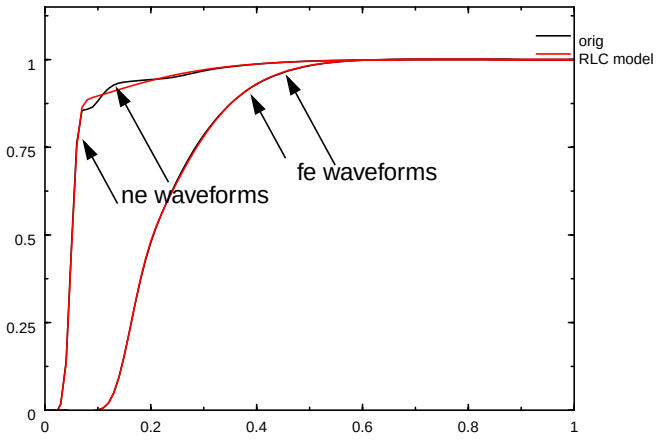


Fig. 9. Near and far end waveforms of a clock H-tree with inductance

In Fig. 9, we show the output waveforms of a clock driver. The clock tree was laid out as a two level H-tree and modeled using a frequency-dependent circuit model [7]. The clock tree was designed to operate at frequencies over 1 GHz and contained 5981 elements. As the figure shows, the proposed driving point model comprising of just four elements (since k was chosen to be one) is sufficient to capture the essential features of the waveform. We also show the waveforms at one of the leaf nodes. Note that the waveforms are indistinguishable when the waveform generated by the proposed model is used to drive the clock tree. In Fig. 10., we show the near end and far end waveforms for the clock tree, modeled with and without inductance. As can be seen, inductance improves the transition time of the waveforms.

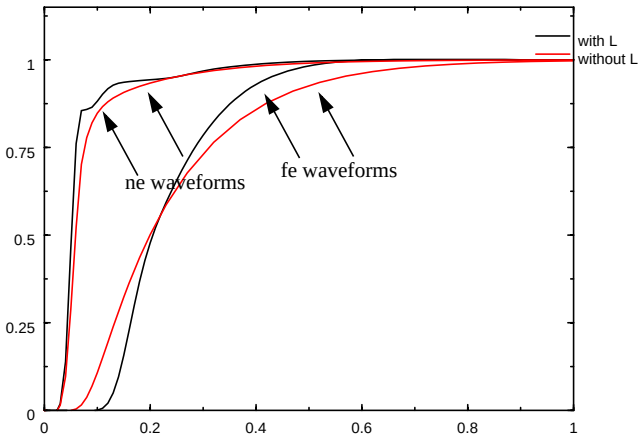


Fig. 10. Waveforms for the clock tree with and without modeling inductance

V. CONCLUSIONS

The proposed model captures the essential features of the driving point waveform for on-chip RLC interconnects. Therefore, it provides a reasonable alternative to the pi-model, which is not synthesizable in most cases where inductive effects are sufficient to affect timing. While some high frequency components in the signal are not captured by our model, their impact on timing is expected to be minimal as shown by the close agreement of the far-end waveforms.

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