A Programmable Built-In Self-Test Core for Embedded Memories

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Abstract—Testing embedded memories is becoming an industry-wide concern with the advent of deep-submicron technology and system-on-chip applications. We present a prototype chip for a programmable built-in self-test (BIST) design that is used for testing embedded memories, especially DRAMs. The BIST chip supports various memory test algorithms by a novel controller and sequencer design. The area of the core circuit is about $1,020 \times 1,020 \mu m^2$ using a $0.6 \mu m$ CMOS process, and the clock speed is over 100MHz.

I. INTRODUCTION

Embedded DRAM (eDRAM) provides high-capacity storage at a higher data rate as compared with commodity DRAM whose data rate is limited by the number of pins available. Also, eDRAM reduces overall power consumption and hardware cost. Merging DRAM and logic is expected to bene£t the system IC industry. However, there are challenges in doing so—process optimization for combining DRAM and logic, design and test methodologies for guaranteeing its performance, quality, and reliability, etc. Testing eDRAM is more dif£cult than testing commodity DRAM. First of all, accessing the deeply embedded DRAM core from an external memory tester is costly. Additionally, memory testers for full quali£cation and testing of eDRAM's will be much more expensive due to increased speed and I/O data width. It is widely believed that built-in self-test (BIST) is the most promising solution to this issue—with BIST, the tester requirement can be minimized, and the tester time can be greatly reduced throughout the entire test ¤ow of the eDRAM. Also, parallel testing of the memory banks are easier with BIST. Therefore, BIST has been considered as a basic requirement for eDRAM's. Another advantage for BIST is that it is also a good approach to protecting the intellectual property (IP).

Many BIST schemes have been proposed for embedded memories (see, e.g., [1, 2]). In this work, we present a BIST implementation for eDRAM, whose architecture has been reported in [3]. Our BIST design supports wafer test, pre-burn-in test, burn-in, and £nal test. Furthermore, it is £eld-programmable, i.e., test algorithms using predetermined test elements (such as various march elements [4], refresh modes, etc.) can be programmed by the user. The area of the core circuit of our BIST design is about $1,020 \times 1,020 \mu m^2$ using a $0.6 \mu m$ CMOS process, and the clock speed is over 100MHz. Note that the measured result was limited by the tester speed. Timemill simulation actually showed that the core circuit can function correctly at 200MHz for an 80pF load. With the proposed approach, designing and implementing appropriate BIST circuits for various eDRAM's can be done in a systematic way with little effort.

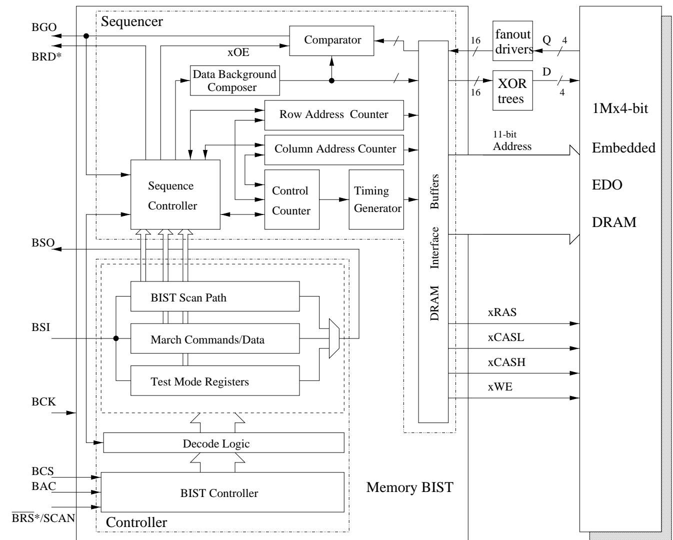

Fig. 1. Block diagram of our BIST design[3].

II. VLSI IMPLEMENTATION

Figure 1 shows the block diagram of our BIST design and the interface between the BIST logic and the eDRAM [3].

The BIST logic is activated by the BIST Activation Control (BAC) input. The BIST Controller is a £nite-state machine, whose state transition is controlled by the BIST Control Selection (BCS) input. The BIST Controller also controls the scan chains—test patterns and commands can be shifted in from the BIST Scan-In (BSI) input and results can be shifted out from the BIST Scan-Out (BSO) output. The Decode Logic and Test Mode Selection modules determine the proper data register to scan in the test commands and subsequently activate the Sequencer. The Sequencer generates the timing sequence for the

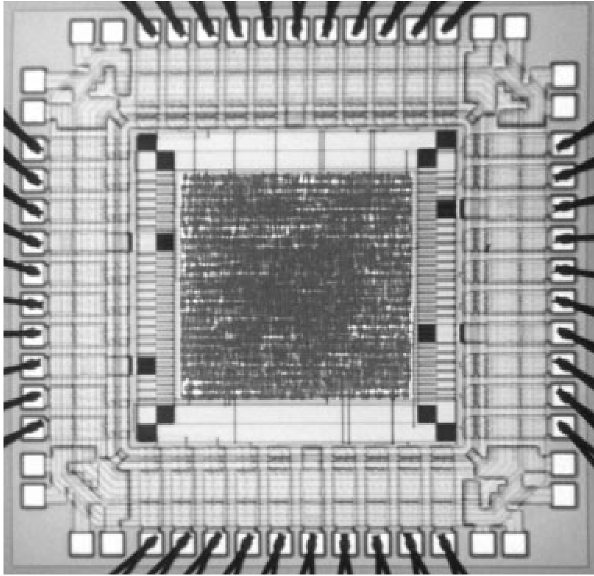

Fig. 2. Test chip photograph.

TABLE I
TEST CHIP CHARACTERIZATION.

Technology	Package	Core size	Cell count	Max. Freq.
$0.6\mu m$ CMOS 1P3M	48 S/B	$1,020^2$ μm^2	$1,197$	100MHz*

*Tested using a 100MHz logic tester.

eDRAM, with the help of some built-in counters and the Timing Generator. The output data (Q) from the eDRAM will be compared with the original input data (D) generated by the Sequence Controller.

The eDRAM is assumed to be a $1M \times 16$-bit EDO DRAM with separate data-ins and data-outs. The row address width is 11 bits and the column address width is 9 bits. The minimum CAS cycle is $10ns$. The test chip is a cell-based design using a $0.6\mu m$ single-ploy-triple-metal (1P3M) process. The die photo is shown in Fig. 2. Due to the I/O limitation, compression and decompression schemes of the input (D) and output (Q) data are implemented by the XOR trees and fanout drivers, respectively, as shown in Fig. 1. Full scan test is used to verify the BIST itself, which has 133 scan cells. Full single stuck-at fault coverage is achieved.

III. SIMULATION AND RESULTS

Timemill simulation showed that the core circuit can function correctly at 200MHz for an 80pF output load, as shown in Fig. 3. The area of the core circuit is about $1,020 \times 1,020\mu m^2$ and the measured speed is 100MHz, which is our tester's limit (see Fig. 4). Some important facts of the chip are listed in Table I.

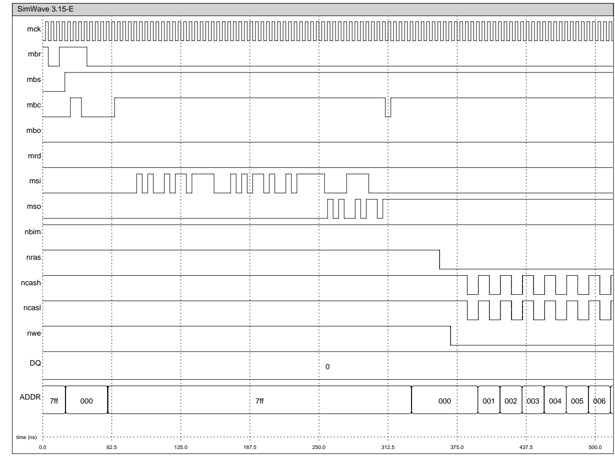

Fig. 3. Timemill simulation result at 200MHz, displaying the initial sequence and page-mode write element.

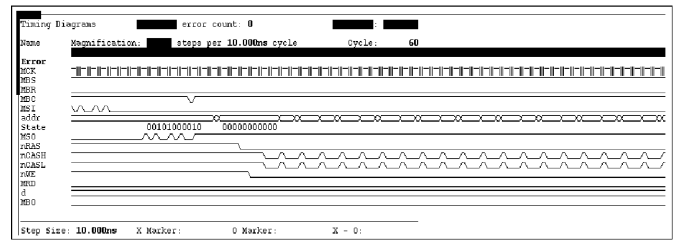

Fig. 4. Measurement result at a clock rate of 100MHz.

IV. SUMMARY AND CONCLUSIONS

In this work, we have presented a programmable BIST for embedded memories. Our approach is ¤exible because additional test commands (other than march elements) can be included with little effort. It is cost-effective since the test time is short, the hardware overhead is low, and the test coverage is high. With the proposed approach, designing and implementing appropriate BIST circuits for various eDRAM's (including SDRAM, DDR DRAM, etc.) can be done in a systematic way.

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