INTERCONNECT THERMAL MODELING FOR DETERMINING DESIGN LIMITS ON CURRENT DENSITY

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ABSTRACT

We apply 3-D finite element analysis to study the thermal coupling between nearby interconnects. We find that the temperature rise in current-carrying lines is significantly influenced by a dense array of lines in the adjacent metal level. In contrast, thermal coupling between just two neighboring lines is insignificant for most geometries. Design rules for average current density are provided for specific geometries given the requirement that the interconnect temperature be no more than 5 ^oC above the substrate temperature. Semi-empirical formulae for coupling effects are presented based on the numerical results.

1. INTRODUCTION

A design limit on the interconnect current density may be obtained by considering two mechanisms: electromigration (EM) and Joule heating. As technology evolves, Joule heating sets the limit on root-mean-square current density J_{rms} [1]. Recently, Hunter [1][2] derived self-consistent solutions for the maximum allowed J_{rms}. However, the results are overly conservative due to the simplified thermal analysis. This work investigates thermal coupling between nearby interconnects by 3-D finite element analysis and illustrates that relaxed limits on J_{rms} may be derived when thermal coupling is considered, because the temperature may be reduced by as much as 30% relative to the case of an isolated line.

Accurate estimation of temperature is also critical for simulating circuit timing and reliability. Higher temperature increases interconnect delay because the electrical resistivity of metal is a linearly increasing function of temperature. Using the temperature dependent Al resistivity values given in [3], as interconnect temperature rises from 25 ^oC (room temperature) to 100 ^oC (typical operating temperature for a high performance microprocessor), the delay goes up by 30%. Most IC failure mechanisms are temperature-dependent, including electromigration in interconnects. The EM-induced mean time-to-failure (MTF) is related to temperature by Black's equation: $MTF(T) = AJ^{-2}exp(E_a/kT)$, where J is the current density, T is the interconnect temperature, k is the Boltzmann's constant and A and E_a are technology-dependent constants [4].

According to one study, the MTF is reduced by 90% when the temperature rises from 25 ^oC to 52.5 ^oC [5]. iTEM [6], an electromigration reliability diagnosis tool, took into account the interconnect temperature and, thus, provided a more realistic estimate of MTF than previous tools which only considered the current density. However, iTEM only considered self-Joule heating and heat conduction from the substrate; it neglected heat conduction to nearby interconnects. Therefore it tends to overestimate the interconnect temperature and underestimate the MTF. In order to facilitate more accurate estimation of temperature-dependent circuit timing and reliability, we will present semi-empirical formulae based on our numerical results.

The remainder of this paper is organized as follows. In Section 2, we describe the methodology used to obtain the numerical results. In Section 3, simulation results are shown for a single isolated interconnect, an interconnect coupled to a parallel neighbor, and an interconnect coupled to a cross-at-90° line array; then, design rules are proposed in terms of J_{rms}. Semi-empirical formulae are presented in Section 4. Finally, we summarize our results.

2. COMPUTATIONAL METHODOLOGY

The simulations were carried out by ANSYS5.3, a finite element analysis package. The configuration simulated was a semi-infinite insulator block with embedded interconnects. Three-dimensional finite elements were chosen. An adaptive mesh was used. The heat generation rate Q, which is induced by current flow, was specified as the body load. The heat generation rate can be related to the current density J by $Q = J^2\rho$, where ρ is the temperature-dependent resistivity of the metal line. The temperature of the substrate $T_{substrate}$ was set to zero, which allows us to use the superposition of solutions due to various current sources. Thus, all values for interconnect temperature shown hereinafter should be added to the real substrate temperature. By taking advantage of symmetry, we simulate only a portion of a structure whenever possible. For symmetrical interfaces, we adopt the adiabatic boundary condition for computational efficiency. The infinite boundary condition was imposed on the surfaces which are sufficiently far away from the heat source, where "sufficiently far away" is defined in terms of the characteristic length for heat diffusion.

For simulation purposes, we assume that the ILD (inter-level dielectric) is SiO_2 and the interconnect material is Al. For Cu interconnects, we expect the coupling effects to be even greater due to copper's higher thermal conductivity. In the simulations, we used thermal conductivity values for bulk SiO_2 and Al evaluated at 100 ^oC [7][8], as given in Table 1. All interconnects in our simulations are infinitely

k_m	k_d	ρ
$144\ W/m/\ ^oC$	$1.4\ W/m/\ ^oC$	$5.05 \times 10^{-6}\ \Omega \cdot cm$

Table 1. Material parameters used in the simulations. All parameters were evaluated at $100\ ^oC$. k_m and k_d are the thermal conductivities of Al and SiO_2, respectively. ρ is the resistivity of Al.

long. The correlation with finite length interconnects is discussed at the end of Section 3.3.

Because we use $100\ ^oC$ values for electrical resistivity and thermal conductivity in our simulations, the results most accurately represent interconnect heating in a chip operating at about $100\ ^oC$. However, even if the chip temperature were lower, the interconnect heating effect would be quite similar to that which we simulated because the resistivity would be lower (which reduces heat generation) and the thermal conductivity of both metal and dielectric would be lower (which increases temperature for a given amount of heat generation). For a given current density, we find that ($T_{interconnect}$-$T_{substrate}$) at $25\ ^oC$ and $100\ ^oC$ differ by less than 4%. A more significant source of error is our use of bulk material values for thermal conductivities due to a lack of any well established values for thin films. The thermal conductivity of a thin film depends on the film thickness due to boundary scattering. Kumar [9] predicted the reduction in thermal conductivity of thin metal films. Lee [10] showed that the thermal conductivity of SiO_2 films decreases with film thickness for films < 50nm thick. One study indicates that the error may be as large as 15% when bulk material conductivities are used to calculate the rise of interconnect temperature over the substrate temperature [5].

3. NUMERICAL RESULTS AND DESIGN RULES

3.1. Single lines

The temperature of a single isolated interconnect (Fig. 1) is used later as a baseline for determining the change in temperature due to coupling. Fig. 2 shows the maximum temperature in a single line with constant current density as a function of line width w and distance to the substrate h. As w increases, more heat is generated and the heat flow from sides of the metal line becomes less significant, therefore the temperature increases. The temperature also increases as h increases since the thermal resistance between the metal line and the substrate, i.e., the heat sink, becomes larger.

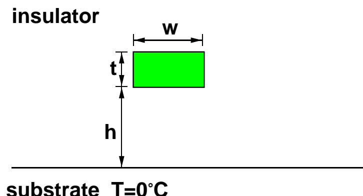

Figure 1. The single line configuration.

3.2. Parallel Coupling

To investigate thermal coupling between a pair of lines, the parallel coupling configuration shown in Fig. 3 is studied. From this point on, we shall refer to lines which carry significant current as power lines and those which do not as signal lines. This notation is used in light of the observation that the average current density in most signal lines is too low to generate significant Joule heat. Of course, Joule heating can be a concern for signal lines with a high activity factor such as clock lines. Such lines are treated as power lines for thermal analysis. Define T as the maximum temperature in the power line and T_0 as the maximum temperature in an identical power line without a neighboring signal line (T_0 was simulated in Section 3.1). The temperature reduction in the power line due to coupling, $(T_0 - T)/T_0$, is plotted in Fig. 4 with respect to s, w_2 and h. The power line temperature is virtually unaffected for $s \geq h$ (Fig. 4a). $(T_0 - T)/T_0$ becomes significant when the signal line is wider than the power line, $w_2 > w_1$, but this is not a typical IC geometry (Fig. 4b). Thermal coupling is largest in the upper metal levels, i.e., larger values of h (Fig. 4c). The simulation results show that the temperature reduction in the power line due to parallel coupling is negligible, less than 3% for typical geometries encountered in ICs.

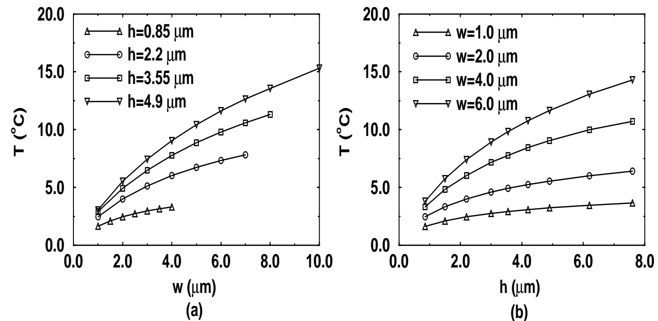

Figure 2. The peak temperature relative to $T_{substrate}$ inside a single line with thickness $0.45\mu m$ as a function of line width w and distance to the substrate h ($J_{rms} = 2.0\ MA/cm^2$).

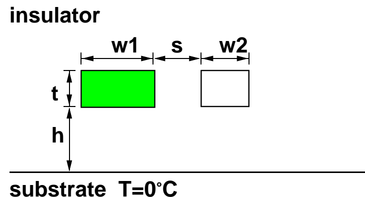

Figure 3. The parallel coupling configuration. The shaded area denotes the line with current flow, whose temperature will be monitored, and the unshaded object denotes the line with negligible current flow.

Although the signal line does not have much effect on the temperature of the power line, the power line does significantly impact the signal line temperature. This point will be addressed further in Section 4.

3.3. Cross Coupling

Unlike the case of two parallel lines, the effect of a line array on the temperature of a power line is much more significant. A cross-at-90° line array is illustrated in Fig. 5. Fig. 6 shows the temperature reduction in the power line as a function of w_2 and h (w_2 and h defined in Fig. 5). The temperature reduction may be as much as 30%. Note that we are considering the maximum temperature in the power line here. There are parts of the line which are cooled to an even greater extent. Fig. 6a shows that the thermal coupling drops off rapidly once $s > w_2$ (sparse array). Fig. 6b shows that as h increases, the effect of the substrate heat sink is reduced and proportionally more heat is conducted

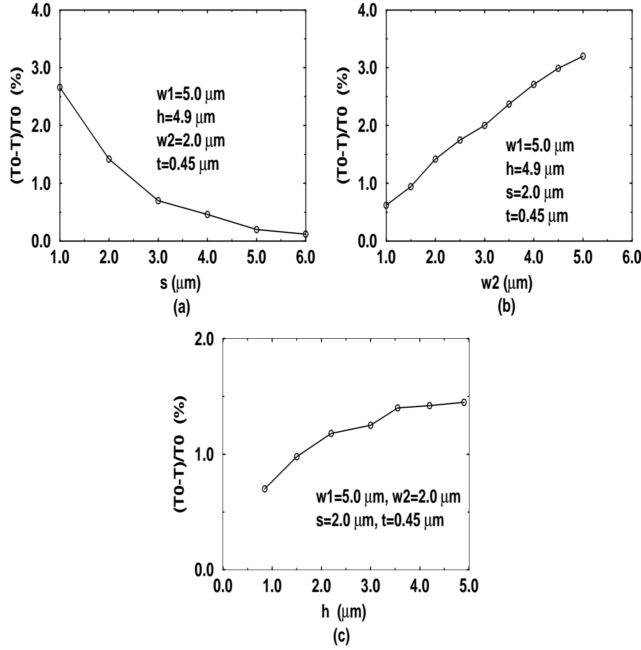

Figure 4. The temperature reduction in a power line due to parallel coupling. Current density in power line: $J_{rms} = 2.0MA/cm^2$.

away by the line array, which leads to a greater $(T_0 - T)/T_0$. Fig. 7 shows $(T_0 - T)/T_0$ as a function of s. Similar to Fig. 6a, a sparse line array is shown to produce a reduced effect. Fig. 8 investigates the effect of s on $(T_0 - T)/T_0$ for a fixed value of w_2/s. $(T_0 - T)/T_0$ depends on w_2 and s individually, not solely on the line array density w_2/s. This is explained as follows. First we note that the heat flux is non-uniform and the interconnect temperature is maximum in the center of the region without a signal line running below (or above). As w_2 and s increase with the ratio fixed, the maximum temperature in the power line increases due to the wider dielectric neighbor and thus $(T_0 - T)/T_0$ decreases.

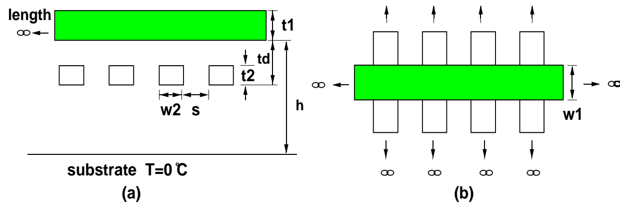

Figure 5. The cross coupling configuration: (a) side view, (b) top view. $t_d > 0$ if the line array runs above the power line and $t_d < 0$ if the array runs below the power line.

Next, we investigate the impact of power line width w_1 and signal line array placement on $(T_0 - T)/T_0$. Fig. 9a shows that for $w_1 \geq 2w_2$, the effect of w_1 is negligible. The effect of line array position is shown in Fig. 9b. When $t_d \leq 0.3h$, which typically corresponds to a power line in level 4 or higher, the results do not depend on whether the line array runs above or below the power line and we can treat the two cases as one. Note that in all of our analysis, we only consider coupling between adjacent metal levels. This is reasonable because simulation results indicate that

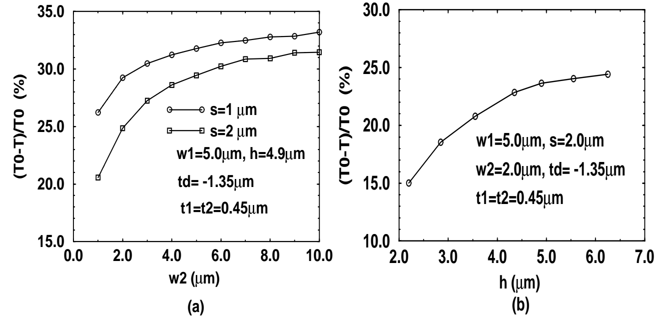

Figure 6. The temperature reduction in a power line due to cross coupling.

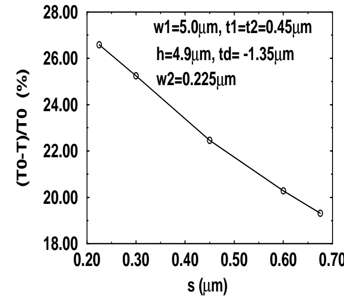

Figure 7. The effect of line array spacing on power line temperature. Note that in this example, $w_2 < t_2$, which is typical of advanced technologies.

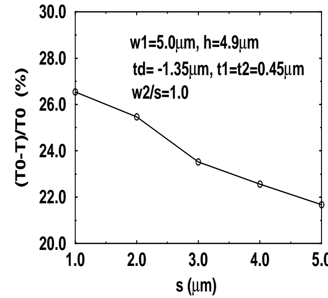

Figure 8. The temperature reduction due to cross coupling for a fixed signal line density w_2/s, showing that $(T_0 - T)/T_0$ is not merely a function of w_2/s.

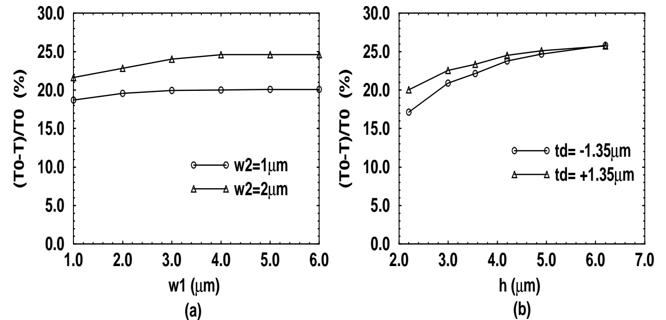

Figure 9. Cross coupling configuration. The effect of w_1 and t_d on temperature.

coupling to a line array two layers away is negligible.

Of particular importance is the case where the lines in the signal line array also carry current, denoted as J_2. Now there are two competing effects: power line cooling due to the high thermal conductivity of the signal lines and power line heating due to the additional heat sources. Shown in Fig. 10 is $(T_0 - T)/T_0$ as a function of s. As long as $J_2 \leq 0.4J_1$ where J_1 is the current density in the power line, the line array will reduce the power line temperature.

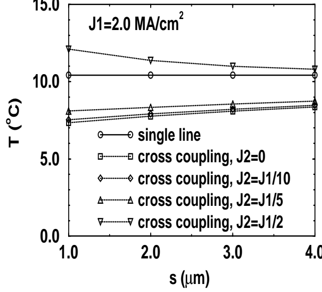

Figure 10. The temperature of the power line (relative to the substrate temperature) when current flows in both the power and the signal lines. $h = 4.9\mu m, w_1 = 5.0\mu m, w_2 = 2.0\mu m, t_d = +1.35\mu m, t_1 = t_2 = 0.45\mu m$.

In the simulations, the interconnects were assumed to be infinitely long. Real (finite) interconnects will have the same temperature as the lines simulated here in any region more than two heat diffusion lengths away from a contact to the heat sink. The heat diffusion length is defined by $(k_m t_1 h/k_d)^{1/2}$. For a typical technology, the diffusion length may vary from $5\mu m$ to $40\mu m$, depending on which metal level the line is in.

3.4. Design Rules

Existing design rules do not take into account thermal coupling to line arrays, thus they may be overly conservative. Fig. 11 shows contours of maximum allowable J_{rms} in the $w_2 - s$ plane, assuming that the maximum allowable interconnect temperature is 5 ^oC above the substrate temperature [11]. The maximum allowable J_{rms} in a single power line is noted on each figure for reference. Table 2 lists the parameters used to generate Fig. 11. These design curves indicate that J_{rms} can be increased by up to 20% from the value derived when thermal coupling is ignored.

4. THERMAL ANALYSIS

Although the simulation results help one to understand the coupling effects, they are too geometry specific to guide design. Semi-empirical formulae can be used instead.

The temperature of an isolated power line is derived based on the geometry shown in Fig. 1. A single line is embedded in a semi-infinite insulator and acts as a heat source. The maximum temperature in the line can be expressed as

$$T = q \cdot R = q \cdot \frac{h}{wlk_{eff}} \quad (1)$$

where $q = J^2 \rho wlt$ is the heat generated by a segment of interconnect with length l, width w and thickness t, R is the thermal resistance between the line and the substrate, k_{eff} is the effective thermal conductivity of the dielectric layer between the line and the substrate considering 2-D heat flow.

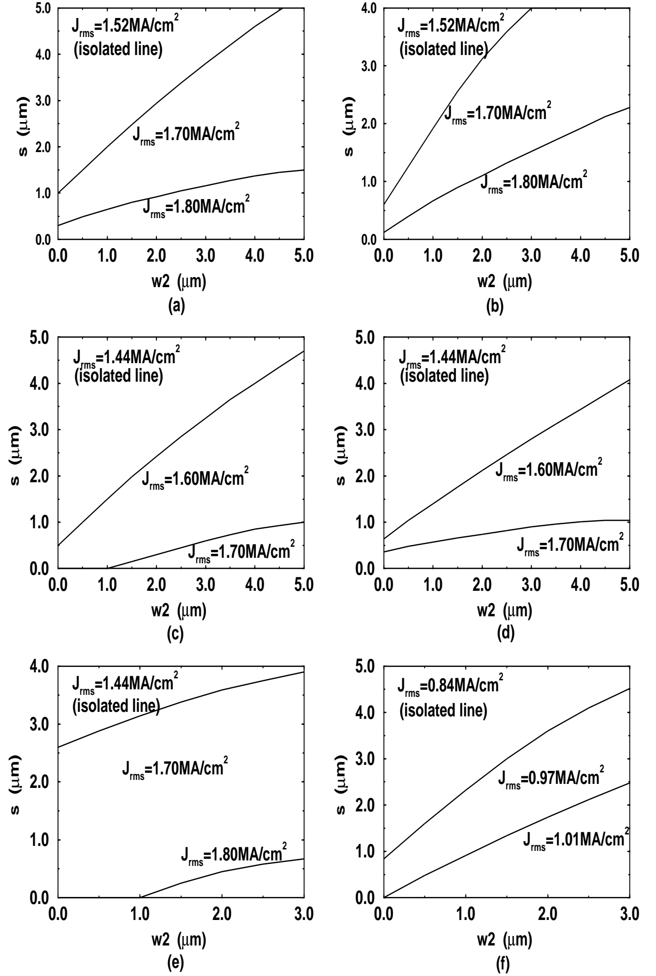

Figure 11. Design curves which yield $T_{interconnect} < T_{substrate} + 5\ ^oC$. The region below a line is the safe design space. The geometries corresponding to each design curve is given in Table 2.

One often cited approximate expression for k_{eff} is Bilotti's equation [12], which was derived assuming that heat flows only through the bottom of the heat source. This expression is given in Eq. 2.

$$k^{(1)}_{eff}(h, w) = k_d \left(1 + 0.88\frac{h}{w}\right) \quad (2)$$

In reality, the heat flows from the sides and top as well as from the bottom of the line. We take into account the conduction from all sides by using the formula presented by Andrews [13] and calibrating the parameters with simulation results. The resulting k_{eff} is given in Eq. 3.

$$k^{(2)}_{eff}(h, w, t) = k_d\ 1.86\frac{h}{w}\ [log(1 + \frac{h}{w})]^{-0.66} \left(\frac{w}{t}\right)^{-0.1} \quad (3)$$

Fig. 12 shows Eq. 3 provides more accurate results than Eq. 2.

As indicated in Section 3.2, the effect of parallel coupling on the power line temperature is negligible. Thus, the temperature of a power line, T_1, in either the isolated or parallel

curve	$w_1(\mu m)$	$h(\mu m)$	$t_1(\mu m)$	$t_2(\mu m)$	$t_d(\mu m)$
a	5.0	3.55	0.45	0.45	+1.35
b	5.0	3.55	0.45	0.45	-1.35
c	5.0	4.9	0.45	0.45	+1.35
d	5.0	4.9	0.45	0.45	-1.35
e	2.0	3.4	0.9	0.9	+1.7
f	5.0	5.1	1.3	0.9	+2.2

Table 2. The geometries corresponding to design curves in Fig. 11.

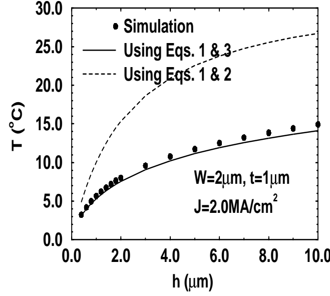

Figure 12. Comparison of formulae and 3-D simulation results for signal line temperature.

coupling configuration may be estimated by applying Eqs. (1) and (3).

Since the temperature of the signal line, T_2, is important for circuit timing analysis, we develop formulae for T_2 as well. We replace the rectangular heat source (i.e., the power line) by a cylindrical or, more generally, an elliptical heat source and then use the analytical solution [14] for temperature around a cylindrical (elliptical) source to approximate T_2. When $w_1/t_1 \leq 3$, the signal line temperature may be estimated by approximating the power line as an cylindrical heat source and applying Eq. 4.

$$T_2 = \left[\frac{1}{2} ln \left(\frac{x^2 + 4h^2}{x^2}\right) / ln \left(\frac{3.545h}{\sqrt{w_1 t}}\right)\right] \cdot T_1 \quad (4)$$

The more general elliptical heat source model is needed for wider power lines and a more complicated formula is derived for which we have provided some simplification by optimizing only for $w_1/t_1 \geq 2$.

$$T_2 = \frac{f(x, h + \frac{t}{2})}{f(\frac{w_1}{2}, h + \frac{t}{2})} \cdot T_1 \quad (5)$$

where

$$f(x, D) = ln \left(\frac{a_1 + b_1}{a_2 + b_2}\right) \quad (6)$$

$$a = \frac{w_1}{\sqrt{\pi}} \quad (7)$$

$$b = x^2 + (2D + a)^2 - a^2 \quad (8)$$

$$a_1 = \sqrt{a^2 + b_1^2} \quad (9)$$

$$b_1 = \sqrt{\frac{b + \sqrt{b^2 + 4a^2(2D + a)^2}}{2}} \quad (10)$$

$$a_2 = \sqrt{a^2 + b_2^2} \quad (11)$$

$$b_2 = \sqrt{\frac{x^2 + \sqrt{x^4 + 4a^4}}{2}} \quad (12)$$

Above, $x = \frac{1}{2}w_1 + s + \frac{1}{2}w_2$ is the distance from the center of the power line to the center of the signal line and $D = h + \frac{1}{2}t$ is the point at which the temperature is monitored.

Fig. 13 compares the fit of both equations to the numerical results for the specific case of $w_1/t_1 = 2.2$.

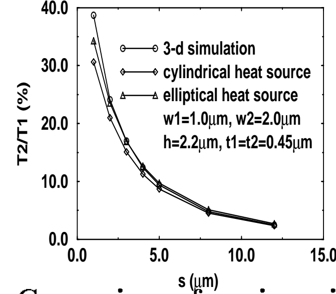

Figure 13. Comparison of semi-empirical and 3-D simulation results for signal line temperature under parallel coupling.

The temperature of the power line in the cross coupling configuration is obtained by means of a lumped thermal model. Heat flow and temperature in a thermal system are analogous to current flow and voltage in a electrical system, respectively; thus, the thermal system in Fig. 5 can be mapped to a lumped resistive network, as shown in Fig. 14a, where the R's are thermal resistances and the nodal voltages represent the nodal temperatures. The lumped

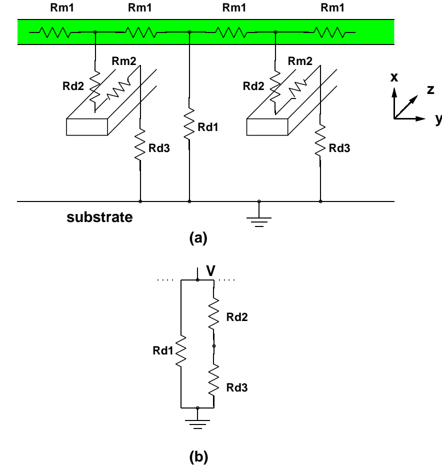

Figure 14. Lumped thermal models: (a) Including heat flow in the interconnects. (b) Neglecting heat flow in the interconnects, a simplified model is derived.

model ignores all heat flow in the y-direction; most significantly it does not reflect heat flow from the power line to the sides of the signal lines (i.e., coupling between R_{d1} and R_{d2}). This inaccuracy is corrected for empirically in the final expression for T. Due to the relatively high thermal conductivity of Al, the thermal resistance of the interconnects may be neglected, yielding the simplified lumped model shown in Fig. 14b, which we will use.

The temperature of the power line can be expressed as:

$$T = q \left[R_{d1} // (R_{d2} + R_{d3})\right] \quad (13)$$

Without cross coupling, the temperature of the power line is

$$T_0 = q R_{d0} \quad (14)$$

Thus, the temperature reduction in the power line due to coupling $(T_0 - T)/T_0$ can be calculated. Note that in Eqs. 13 and 14, $q = J^2\rho(s + w_2)w_1t_1$ (this is the Joule heat generated in a power line segment of length $s + w_2$).

The formula for each thermal resistance is given below, as derived based on our previous modeling of heat flow from an isolated line to the substrate.

$$R_{d1} = \frac{h}{w_1 s k_{eff}^{(2)}(h, w_1, t_1)} \quad (15)$$

$$R_{d2} = \frac{t_d - t_2}{w_1 w_2 k_{eff}^{(2)}(t_d - t_2, w_1, t_1)} \quad (16)$$

$$R_{d3} = \frac{h - t_d}{w_s w_2 k_{eff}^{(1)}(h - t_d, w_s)} \quad (17)$$

$$R_{d0} = \frac{h}{w_1(w_2 + s)k_{eff}^{(2)}(h, w_1, t_1)} \quad (18)$$

Note that the signal line array acts as cooling fins which expand the area over which heat flow occurs [15]. The cross-sectional area of resistor R_3 is $w_2 \cdot w_s$, where w_s is the effective distance over which the heat has been spread out in the z-direction. In our model, w_s will also account for the small amount of heat flow in the y-direction as mentioned earlier. By fitting data from 3-D simulations, an empirical formula for w_s was derived and is given in Eq. 19.

$$w_s = 36.3\ s^{0.12}\left[1 + exp\left(-\frac{w_2}{s^{0.5t_2}}\right)\right]\left(\frac{h}{t_d - t_2}\right)^{0.2t_2} \quad (19)$$

The parameters in Eq. 19 were optimized for $w_2 < w_1$, $s < w_1$ and $t_2 < 0.5t_d$. $k_{eff}^{(1)}$ is given in Eq. 2 and $k_{eff}^{(2)}$ is given in Eq. 3. Although Eq. 13 is derived for the case in which the line array lies below the power line, it is also valid for high level power lines coupled to an array which lies above since the temperature is practically independent of the line array position when $t_d \leq 0.3h$.

Comparisons between 3-D simulation and the semi-empirical formula are shown in Fig. 15. Within the geometry space we studied, the error is always less than 10%.

5. SUMMARY

In this paper, we investigated the thermal coupling effects between interconnects. Two coupling cases were considered, parallel coupling between a power line and a signal line in the same layer and cross-at-90° coupling between a power line and a line array. We showed that the temperature reduction due to the cross-at-90° case is significant even if the line array carries current, while the effect of parallel coupling is negligible. Modified design rules in terms of maximum allowed root-mean-square current density J_{rms} were proposed. J_{rms} can be increased by up to 20% when coupling effects are taken into account. By fitting the data from the simulations, we developed semi-empirical formulae for interconnect temperature. These formulae can be implemented in CAD tools to provide more accurate simulation of electrothermal circuit timing and reliability.

6. ACKNOWLEDGMENTS

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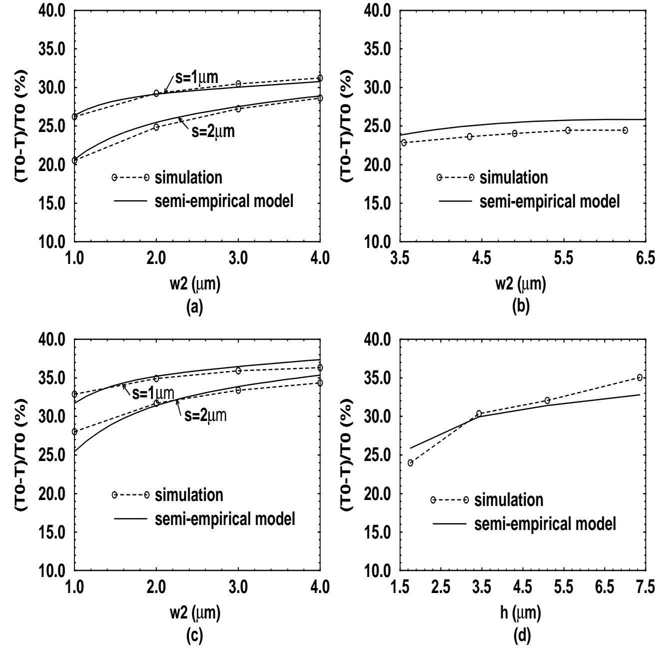

Figure 15. Comparison of semi-empirical and 3-D simulation results for cross coupling. (a) $w_1 = 5.0\mu m$, $h = 4.9\mu m$, $t_1 = t_2 = 0.45\mu m$, $t_d = -1.35\mu m$. **(b)** $w_1 = 5.0\mu m$, $w_2 = 2.0\mu m$, $s = 2.0\mu m$, $t_1 = t_2 = 0.45\mu m$, $t_d = -1.35\mu m$. **(c)** $w_1 = 5.0\mu m$, $h = 5.1\mu m$, $t_1 = 1.3\mu m$, $t_2 = 0.9\mu m$, $t_d = -1.7\mu m$. **(d)** $w_1 = 5.0\mu m$, $w_2 = 2.0\mu m$, $s = 2.0\mu m$, $t_1 = 1.3\mu m$, $t_2 = 0.9\mu m$, $t_d = -1.7\mu m$.

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