System-Level Power Optimization: Techniques and Tools

Luca Benini*

*Universitá di Bologna
Dip. Elettronica Informatica Sistemistica
Bologna, ITALY 40136

Giovanni De Micheli†

† Stanford University
Computer Systems Laboratory
Stanford, CA 94305

Abstract

This tutorial presents a cohesive view of power-conscious system-level design. We consider systems as consisting of a hardware platform executing software programs. We address the problems of power estimation and minimization for such systems.

We consider the major constituents of systems: processors, memories and communication resources. We analyze power dissipation in these components and we survey computer-aided power reduction techniques. Wa also consider global system-level control schemes, such as dynamic power management. We conclude by pointing out further research problems which are still open in this domain.

1 Introduction

Power optimization and estimation at the system level is an area of very active research. The main purpose of this tutorial is to survey the methods and techniques that have been explored in the recent past. To help organize the material, we will cluster the approaches into a few areas. For each area, we provide several bibliographical references as and a few descriptive notes. The purpose of these descriptions just to outline what type of system architectures and what power dissipation sources are addressed by the techniques in the area. At the system level, we can group the sources of power dissipation under three coarse cathegories: (i) processing units; (ii) memories; (iii) interconnects and communication. Several techniques address more than one cathegory, while others are more narrowly focused.

We can also coarsely group the architectures targeted by system-level power optimization techniques. Our classification is based on the amount of flexibility available. More specifically, we distinguish between:

- Commodidty-processor systems, where data processing is performed exclusively by a commodity processor (general purpose microprocessor, microcontroller or DSP), and the degrees of freedom are in the design and optimization of memory and communication architectures.

- Custom-processor systems, where data processing can be performed by either commodity processors or dedicated hardware resources. The design of custom processor systems is characterized by wide degrees of freedom.

It is important to realize that the classification of sources of power dissipation and of target architectures is somewhat arbitrary, and that the main purpose of our classification scheme is to help the reader in directing further investigation.

2 Memory optimization techniques

These techniques are mainly focused on reducing the power consumed by memories. Sometimes, concurrent memory and communication power dissipation is targeted. Communication is intended as data transfer between memory and processor. Both commodity and custom processor systems are targeted. Several approaches focus on creatively exploiting caching to reduce power consumption [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. Other techniques target more general memory hierarchies, where caches as well as various types of memories (SRAMs, DRAMs) are available, data tranfer and placement are tightly controlled [11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24].

3 Hardware-software partitioning

Starting from a highly abstract functional system specification (a task graph), these technques attempt to find an optimal partitioning ad assignment of tasks between hardware and software [25, 26, 27, 28, 29]. The target architectures have considerable flexibility: processing elements interconnect and memory architecture are application-specific. In principle all sources of power dissipation can be addressed at this level of abstraction, however the high abstraction level of the specification may prevent accurate assessment of power savings. A few alternative techniques have been develped for automatically constructing application-specific power-optimized processors according to a fixed template [30, 31]

4 Instruction-level power optimization

The focus of instruction-level power optimization is on commodity-processor systems. These methods are based on a processor power model where each instruction (pair of instructions) has a power cost. Power optimization is based on

selecting a minimum-power instruction mix for executing an application [32, 33, 34, 35, 36]. Some processor architectures support dedicated low-power instruction sets, designed with the purpose of facilitating instruction-level power optimization [37, 38, 39].

5 Control-Data-flow transformations

Executable specifications can be represented as control-data flow graphs (CDFGs). Mapping CDFGs to dedicated hardware is the main purpose of high-level synthesis techniques. High-level synthesis for low power is thoroughly surveyed in [40]. Several authors have proposed CDFG tranformations that can be applied before high-level synthesis [41, 42, 43, 44, 45, 46, 47, 48, 49]. These transformations have been shown to be very effective in producing dedicated hardware processors with low power consumption.

6 Variable-voltage techniques

Probably the most effective way to reduce power consumption is to lower supply voltage. Traditionally, systems have been designed to operate at fixed supply voltages. Recent research results have shown the technical viability of dynamically variable voltage supply sources [50, 51, 52, 53, 54, 55, 56, 57, 58]. Variable-voltage systems have achieved extremely low power consumption compared to their standard, fixed-voltage counterparts. Several automatic optimization techniques have been developed for supporting the design of variable-voltage systems [59, 60, 61, 62, 63, 64, 65, 66]. These techniques may prove very useful when variable-voltage circuits enter mainstream technology.

7 Dynamic power management

Dynamic power management (DPM) is a control methodology that allows systems (or systems' components) to be placed in low-power sleep states, when inactive. Related work relates to industrial standards [77, 78], general approaches to power management [67, 68], predictive [83, 84, 85] and stochastic [87, 86, 87, 88] control policies. Other research has addressed matching the system/component properties with the control policy optimization model [69, 70, 71]. DPM is currently applied to control micro-processors [72, 73, 74, 75, 76], hard-disks [79, 80, 81, 82] and handheld devices such as laptop computers.

8 Interface power minimization

A large amount of power is dissipated in data communication over heavily-loaded on-chip or off-chip busses. Several approaches have been developed to reduce switching on busses via signal encoding [90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100]. Other techniques can be applied synergically with signal encoding to produce data stream with low transition activity [89, 101, 102, 103, 104, 105].

9 Approximate signal processing

A few techniques have taken an aggressive approach to power reduction in some classes of applications where a well-controlled amount of noise can be tolerated. The key idea in these approaches is that power dissipation can be drastically reduced by allowing some inaccuracies in the computation [106, 107, 108].

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