Ultra-Low Power Digital Subthreshold Logic Circuits*

Hendrawan Soeleman and Kaushik Roy
Department of Electrical and Computer Engineering
Purdue University
West Lafayette, IN 47907, USA
Phone: (765) 494-2361
Fax: (765) 494-3371
E-mail: {soeleman, kaushik}@ecn.purdue.edu

1. ABSTRACT

Numerous efforts in balancing the trade-off between power, area and performance have been done in the medium performance, medium power region of the design spectrum. However, not much study has been done at the two extreme ends of the design spectrum, namely the ultra-low power with acceptable performance at one end (the focus of this paper), and high performance with power within limit at the other. One solution to achieve the ultra-low power requirement is to operate the digital logic gates in subthreshold region. We analyze both CMOS and Pseudo-NMOS logic families operating in subthreshold region. We compare the results with CMOS in normal strong inversion region and with other known low-power logic, namely, energy recovery logic. Our results show an energy per switching reduction of two orders of magnitude for an 8x8 carry save array multiplier when it is operated in subthreshold region.

1.1 Keywords

Ultra-low power, digital logic, subthreshold circuits

2. INTRODUCTION

In the medium performance, medium power consumption design region, numerous optimization efforts have been made[1,2,3]. However, not much study has been done at the two ends of the design spectrum, namely ultra-low power with acceptable performance at one end, and high performance design with power within specified limit at the other end. This paper focuses on design techniques for ultra-low power dissipation where performance is of secondary importance. One way to achieve this goal is by running the digital circuits in subthreshold mode. The incentive of operating the circuit in subthreshold mode is to be able to exploit the subthreshold leakage current as the operating drive current. The subthreshold current is exponentially related to the gate voltage. This exponential relationship is expected to give an exponential reduction in power consumption, but also an exponential increase in delay. The simulation results show that the reduction in power outweighs the increase in delay, and thus, giving the overall reduction in energy consumption per switching. The paper is organized as follows. Section 3 shows some of the specific application areas where subthreshold circuits are suitable. In section 4, we analyze subthreshold CMOS circuit. Subthreshold Pseudo-NMOS logic is analyzed in section 5. Section 6 shows the comparison results of subthreshold logic with other known low-power logic, such as energy recovery logic. Conclusion is given in section 7.

3. APPLICATION AREAS

Subthreshold digital circuits will be suitable only for specific applications which do not need high performance, but require extremely low power consumptions. This type of applications include medical equipments such as hearing aids and pace-maker[4,5], wearable wrist-watch computation[6], and self-powered devices[7]. Subthreshold circuits can also be applied to applications with bursty characteristics in which the circuits remain idle for an extended period of time (Figure 1). The original active time period T in strong inversion region (top half) is being extended throughout the idle time period T' running in subthreshold region (bottom half). The same number of operations is performed in both cases, but with much lower power consumption in the subthreshold operation.

4. SUBTHRESHOLD CMOS LOGIC

Subthreshold CMOS logic operates with the power supply Vdd less than the transistors' threshold voltage Vt. This is done to ensure that all the transistors are indeed operating in the subthreshold region. We use HP $0.35\mu m$ process technology for our circuit simulation with Vt of NMOS and

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PMOS transistors as 0.57V and 0.74V, respectively. In subthreshold region, for Vds>3kT/q, Ids becomes independent of Vds for all practical purposes. In analog design, this favorable characteristic has been extensively exploited as it provides an excellent current source that spans for almost the entire rail-to-rail voltage range. In digital design, circuit designers can take advantage of this characteristic by being able to use more series connected transistors. The 3kT/q drop (about 78mV at T=300K) is practically negligible compared to the Vt drop in the normal strong inversion region.

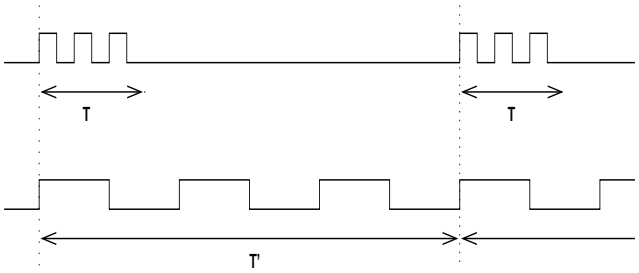

Figure 1. Subthreshold Circuit in Bursty Computation

4.1 Power Consumption

Figure 2 shows the power consumption vs. frequency for various power supply values. The figure is obtained by simulating a chain of inverter gates forming a ring oscillator. From the figure, we notice that:

- At higher frequency, the power consumption is linearly dependent with the operating frequency due to the dominant dynamic power component.
- At lower frequency, the power consumption becomes independent of operating frequency as the static power component takes over.
- At same operating frequency, subthreshold circuits consume less power than the strong inversion circuits.

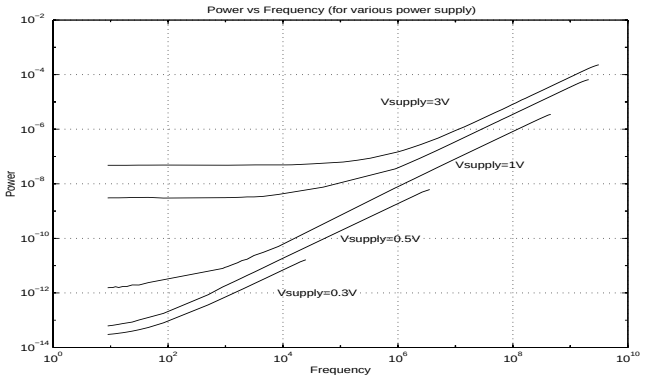

Figure 2. Power Consumption vs. Frequency

4.2 PDP, VTC, and Transistor Sizing

Subthreshold circuits has lower PDP (power-delay product) because the reduction in power consumption outweighs the increase in delay by an order of magnitude.

The VTC (voltage transfer characteristics) of the inverter gate running in subthreshold mode is closer to ideal compared to the one in strong inversion region. The improvement is mainly caused by the increase in the circuit gain. The exponential relationship between Ids and Vgs gives rise to an extremely high transconductance *gm*. The near ideal VTC also yields better static noise margin.

In the normal strong inversion region, it is well-known that the optimum NMOS to PMOS ratio which will give a minimum delay is due to the ratio of NMOS and PMOS transconductance parameters[8]. In subthreshold region, however, the optimum ratio has a much wider range, due to the exponential ratio between the NMOS and PMOS currents (figure 3).

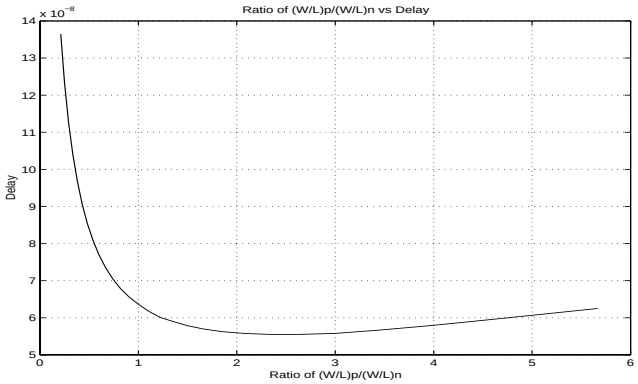

Figure 3. Ratio of PMOS to NMOS vs. Delay

4.3 Results

Table 1 and 2 show the simulation results for Inverter, 2-input NOR, 2-input NAND gates and 8x8 carry-save array multiplier in strong inversion and subthreshold regions, respectively.

Table 1: Strong Inversion Region (Vdd=3.3V)

Logic	Power (W)	Delay (s)	PDP (J)
INV	3.101e-4	5.421e-11	1.681e-14
NOR-2	4.27e-4	1.211e-10	5.171e-14
NAND-2	2.243e-4	9.307e-11	2.087e-14
Multiplier	3.339e-3	1.271e-9	4.24e-12

Table 2: Subthreshold Region (Vdd=0.5V)

Logic	Power (W)	Delay (s)	PDP (J)
INV	5.324e-10	4.493e-7	2.392e-16
NOR-2	6.842e-10	9.527e-7	6.519e-16
NAND-2	3.943e-10	7.417e-7	2.924e-16
Multiplier	1.495e-12	8.294e-2	12.40e-14

5. SUBTHRESHOLD PSEUDO-NMOS

To achieve some improvement in operating speed, we analyze subthreshold Pseudo-NMOS logic. To ensure that Pseudo-NMOS logic functions correctly, careful sizing of PMOS to NMOS ratio is a must. In subthreshold region, however, Pseudo-NMOS logic is much more robust than its strong-inversion counterpart. This is mainly because of the favorable device subthreshold characteristics, namely:

excellent voltage-controlled constant current source characteristics and exponential relationship. The gate will continue to function correctly as long as the current for PMOS is within the bands of current for NMOS. With a few decades of varying current, the sizing ratio of PMOS to NMOS becomes less critical as wider range of the ratio value is now acceptable for the logic gate to function correctly.

Subthreshold Pseudo-NMOS is comparable to CMOS in term of power and robustness, but with much less area, capacitance and improved performance. The improvement is more significant in wide NOR-like gates due to the absence of the long chain of series-connected PMOS transistors.

5.1 Experimental Results

Subthreshold Pseudo-NMOS logic is compared with subthreshold CMOS. We simulate the logic gates in ring oscillator fashion using TSMC 0.35μm process technology.

Table 3: Subthreshold CMOS and Pseudo-NMOS Logic

	CMOS		Pseudo-NMOS	
Logic	Power (W)	Delay (s)	Power (W)	Delay (s)
INV	4.886e-09	2.234e-07	3.186e-08	5.474e-08
NOR-4	6.064e-09	8.034e-07	3.187e-08	7.054e-08
NOR-8	6.852e-09	1.808e-06	3.187e-08	9.160e-08
NOR-16	7.815e-09	4.482e-06	3.187e-08	1.337e-07
Full Adder	4.691e-09	1.377e-06	2.306e-08	2.219e-07

6. ADIABATIC LOGIC

To validate the power savings of subthreshold logic, we compare it with other known low-power logic, such as adiabatic logic[9,10,11]. We chose quasi-static energy recovery logic (QSERL)[11] for comparison. QSERL is chosen due to its close resemblance to static CMOS. We implemented QSERL and simulated it using TSMC 0.35 μm process technology.

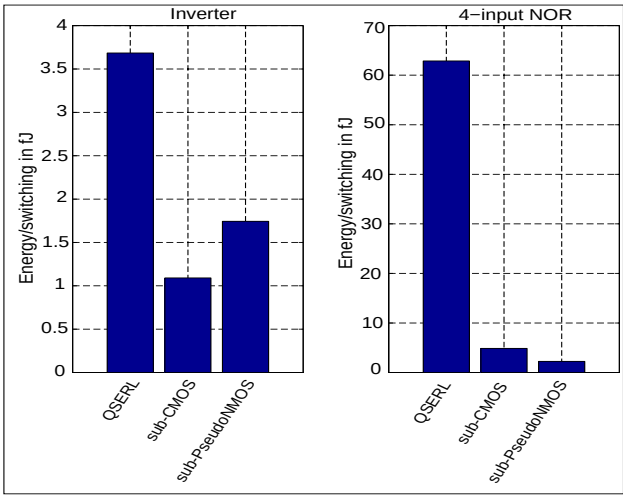

Figure 5. Energy of QSERL and Subthreshold Logic

7. CONCLUSION

In this paper, we have studied various characteristics of digital circuit operating in subthreshold region as a mean to achieve ultra-low power. The subthreshold logic can be easily implemented and derived from traditional existing circuits by lowering the supply voltage to be less than Vt. A number of advantages in subthreshold operation includes improved gain, noise margin, and tolerant to higher stack of series transistors while being more energy efficient than standard CMOS at low frequency of operation. However, due to its slow performance, subthreshold circuit is limited to only certain applications where ultra-low power is the main requirement, and performance is of secondary importance.

8. REFERENCES

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