Differential PLL for Wireless Applications Using Differential CMOS LC-VCO and Differential Charge Pump

Ayman ElSayed, Akbar Ali*, and M.I. Elmasry
Dept. of Elec. & Comp. Eng., University of Waterloo, Waterloo, ON, Canada
{aelsayed, elmasry}@vlsi.uwaterloo.ca
*Conexant Systems Inc., Newport Beach, California
akbar.ali@nb.conexant.com

Abstract

A Differentially controlled monolithic LC-VCO along with a differential charge pump are used to implement a differential PLL for substrate noise immunity. The differential VCO control is achieved with minimal increase in the power consumption and without sacrificing the tuning range. In a 0.5μm CMOS technology the measured VCO phase noise is -119dBc @1.0MHz and the tuning range is 26% of the 1.25GHz center frequency, at a total power consumption of 4.0mA from 3V supply. The common mode rejection of the VCO control lines is more than 2000 at DC. The new differential charge pump architecture provides common mode correction without the need for a clean reference.

1 Introduction

The VCO, being the heart of any PLL based frequency synthesizer, consumes a major fraction of the overall power of the synthesizer, and its performance determines to a large extent that of the whole synthesizer. The total power consumption of the whole synthesizer could be drastically reduced by integrating the VCO. This is mainly because the RF pre-amplifier that buffers the VCO input to the prescalar could be eliminated. In a fully integrated VCO, the tuning range should be large enough to cover for the frequency variations over temperature and process corners. For a typical control voltage from 0 to 3 volts, this means a very large VCO gain. This high VCO gain increases its sensitivity to supply, ground and substrate noise, and makes it very difficult to integrate with other components on the same chip. A differentially controlled VCO could significantly reduce this sensitivity.

In LC VCO's the differential frequency control is not straight forward (as will be discussed later) and usually results in reduction in the varactor tuning range. This reduction in the varactor tunability increases the required VCO power consumption in order to maintain the same tuning range without degrading the phase noise performance. This extra power requirement could be understood by noting that the varactor value needs to be increased to maintain the same ratio of the variable capacitance to the fixed tank and circuit parasitics. For the same oscillation frequency this increase in capacitance mandates a smaller inductor value. To maintain the same phase noise, the current should be increased to produce the same output power on the tank.

The objective of this work is to design a differentially controlled CMOS LC-VCO without sacrificing the tuning range and with minimal increase in power consumption. To integrate this VCO in a PLL we use a differential charge pump with a very simple common mode correction circuit which doesn't need a clean reference. The CMOS technology to be used here adds even more challenge to our objectives, specially in terms of power consumption. It is, however, cheaper and has more potential for higher integration. In addition, the CMOS has some unique beneficial characteristics that are being used to achieve our goals, namely: the availability of fast PMOS devices as opposed to the very slow lateral PNP's in bipolar technologies. Another helpful feature is its much simpler biasing circuitry.

The next section is an overview of the varactor control schemes in a standard CMOS technology. In section 3 we present the proposed differentially controlled VCO architecture and the practical considerations of the circuit design. Section 4 is devoted to the differential charge pump architecture. The whole PLL design, simulation results, phase noise estimation and test results are summarized in the remaining sections.

2 Overview of The Existing Varactor Control Schemes

In order to reduce the VCO sensitivity to the noise generated by other circuits sharing the same substrate and/or supply, it is highly desirable to have a differential VCO. By differential we mean not only to have differential outputs, which helps in rejecting common mode additive noise, but also differential control inputs. The requirement of differential control gets more important as we move towards higher integration. This principle of differential control is commonly used in both ring and relaxation type oscillators. In these oscillators the frequency is usually controlled by changing a bias current, which can easily be done differentially in an integrated environment without sacrificing the tuning range. The situation is different for LC based VCO's where a single ended control is commonly used as a DC reverse bias for the PN diode used as a varactor. Fig. 1 represents a common architecture for integrated LC based VCO's. The cross coupled differential pair Q1-Q2 represents a negative resis-

tance for both tank circuits. The varactors C1 and C2 are connected back-to-back with their cathodes biased at V_{dd}. The control voltage V_{ct} is applied at the virtual ground point and pulls the anodes below V_{dd} so as to keep the junction reverse biased at all times. Changing V_{ct} modulates the diode depletion capacitance and hence the oscillation frequency. This back to back connection eliminates the the need for decoupling capacitors and hence improves the tunability.

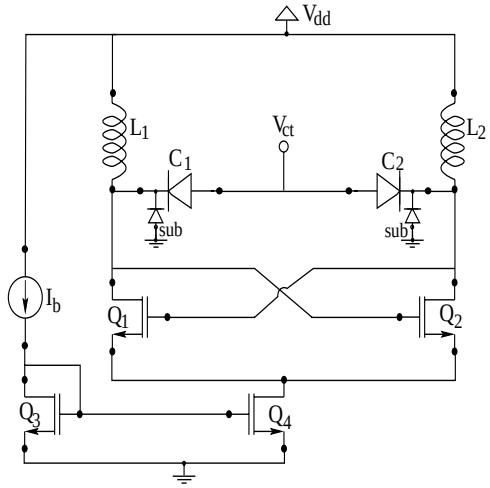

Figure 1: Classical NMOS LC based VCO

The above architecture has been successfully used for bipolar technologies [2], where the base emitter junction of an NPN is used as a varactor diode and the unused base collector junction is connected to the virtual ground. The nature of the varactor diodes available in CMOS processes causes a major drawback in this architecture. As shown in fig. 2 the varactor in a typical CMOS technology is built by diffusing a P^+ region over an N-well, which is exactly the parasitic vertical PNP transistor available in such process. The problem with this varactor structure arises from N-well to P-substrate junction diode hanging on the sensitive tank circuit point as shown in fig.1. This junction adds a huge parasitic capacitance (same order of magnitude of the useful P^+ N-well junction capacitance). This capacitance is however untunable and severely reduces the tuning range of the VCO. The other drawback comes from the fact that this capacitance is biased from V_{dd} to the substrate with the result of increasing the oscillation frequency sensitivity to supply fluctuations which defines the frequency pushing characteristics of the VCO. It is also clear that this architecture has a single ended frequency control.

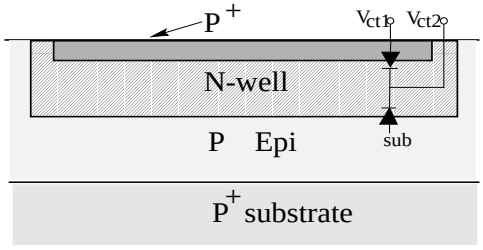

Figure 2: Varactor structure in a typical CMOS process

A straight forward modification of this architecture to alleviate the parasitic junction diode problem and facilitate a differential control for the VCO is shown in fig. 3. The DC decoupling capacitors C_{d1} and C_{d2} decouples the varactors from the circuit's DC. The varactor is then biased by the differential control inputs V_{ct1} and V_{ct2}. The AC decoupling resistors R_{ct1} and R_{ct2} are necessary to isolate the two differential RF output nodes. These resistors should be large enough to minimize their loading effect on the VCO RF output. We, however, want to keep them as low as possible to minimize their noise contribution to the varactor modulation. In addition to the differential control that could be achieved using this architecture, the polarity of the varactor diodes could be chosen as shown in the figure to avoid the parasitic diodes effect by connecting them to the virtual ground at V_{ct1}. The decoupling capacitors should be large enough to reduce their effect on the varactor capacitance seen by the tank. The main problem with this architecture is the parasitic capacitance added to the tank due to the bottom plate capacitance of these large decoupling capacitors. In a typical CMOS process this capacitance is a considerable fraction of the main capacitor and hangs in parallel with the main tank circuit reducing its tuning range. This unfortunately makes this architecture unusable for a typical process, where the achievable tuning range with control voltage from 0 to 3.0 volts is less than the frequency variations due to process tolerances.

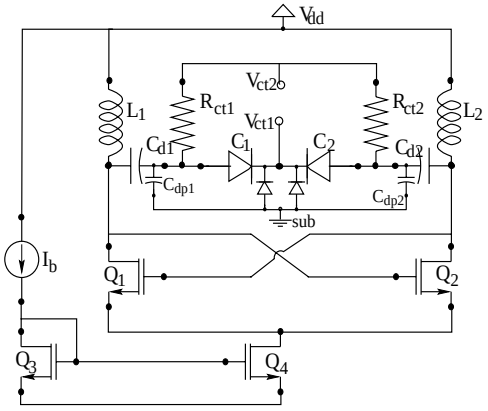

Figure 3: The use of decoupling capacitors for differential VCO varactor control

3 Differentially Controlled CMOS LC-VCO

3.1 Architecture

The circuit proposed in this section [1] combines two methods of controlling the varactor, known in literature, to achieve what we call a "semi-differential" control of the varactor. The first of these is the most commonly used varactor control scheme [8] illustrated in fig. 1. The second scheme (fig. 4) is less popular and has been used by Rofougaran *et al* [3] and modified by Razavi [4]. The idea in this second scheme is to connect the common node between the varactors to the real ground and control the other terminals by a variable voltage drop element (Q3 in the fig.) from V_{dd} to the inductors' common node.

The new circuit proposed in fig. 5 controls both terminals of the varactor. The first terminal is directly controlled by the input V_{ct1}, while the other control signal is coupled to the other varactor terminal through an operational amplifier buffering stage (A1 and Q5). If the OpAmp open loop

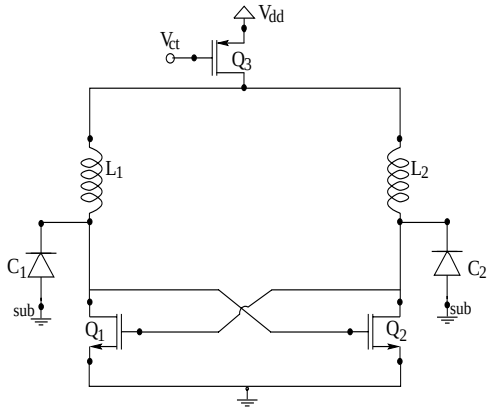

Figure 4: Using voltage drop element to control the VCO varactors [3]

gain is high enough the control signal V_{ct2} could be almost exactly transfered to the varactor terminal within the buffer loop band width. The whole VCO with its main current source Q4 acts as high impedance load (dominated by Q4 output impedance) for the the second OpAmp stage Q5. Assuming everything is ideal, any common mode signal on V_{ct1} and V_{ct2} is transfered to the varactor terminals as common mode, and hence the VCO frequency, won't change.

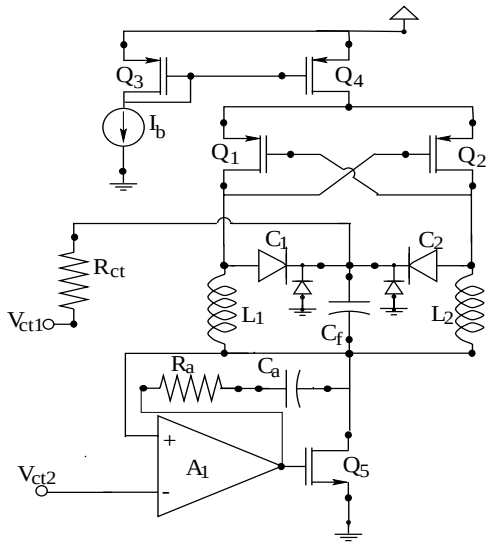

Figure 5: Proposed Differential control architecture for an LC VCO

3.2 Practical Consideration

3.2.1 Opamp design

The architecture outlined here could have been a great solution "if" an ideal operational amplifier is used. There is unfortunately no such ideal thing, and we have to consider different nonidealities and their effect on the circuit performance. The most obvious problem is the noise introduced by the differential amplifier on one of the control lines but not the other. This noise is then not common mode for the differential control inputs and will directly modulate the varactors. In order to reduce this effect the operational amplifier should be designed such that its noise contribution to the varactor modulation is much less than the expected common mode noise picked up on the control line. Reducing the BW of the buffer helps to minimize this noise contribution. The problem with this reduced BW buffer is that beyond this BW the varactor terminal will no longer follow the control voltage and we might end up having almost single ended control for noise with frequencies greater than the BW. Fortunately, the noise we are worried about is the low frequency one. This is mainly for two reasons. First, the high frequency noise is filtered, to a large extent, by the PLL loop filter. The second reason can be referred to the nature of the varactor modulation noise which, as will be discussed later, is inversely proportional to the frequency of the modulating signal. The filtering capacitor C_f will attenuate any RF frequency noise, but unfortunately we can't make it too big or it will cause instability in the buffer loop. It might be of importance here to mention that for noise with frequencies greater than the BW but still too low to be attenuated by C_f we might have a situation even worse than the single ended control situation. In this case the varactor terminal will be a high impedance point and more susceptible to noise. This noise would have been filtered by the PLL loop filter in the single ended control situation. One way to eliminate this problem is to make the OpAmp BW as big as possible so that its dominant pole will be due to C_f at the output. This is currently being investigated as future work on this circuit.

3.2.2 Why PMOS?

Unlike the decoupling capacitor architecture of fig. 3, this new proposed architecture does not solve the problem of the parasitic diodes from the varavtor N-well to the substrate. A good solution, that we propose here to solve this problem is to use PMOS transistors for the VCO core as shown in fig. 5. There are, in fact, several advantages in using this PMOS core; the first of them and the most important as explained above is that the polarity of the varactors could is changed to have the parasitic diode at the virtual ground point while maintaining the whole supply range for tuning. This and other advantages are listed below:

- Eliminate the parasitic diode problem and maintain full swing control.
- The N-well bulk of the PMOS transistors Q1 and Q2 could be connected to their source so that the drain to bulk diodes will have a constant bias, and hence a constant capacitance, as long as the drain current is constant, regardless of the control voltages. This could significantly reduce the oscillation frequency sensitivity to both ground and supply variations.
- The PMOS, being inside an N-well is less susceptible to substrate noise pickup than NMOS.
- PMOS flicker (1/f) noise is an order of magnitude better than that of an NMOS.
- The low gain of the PMOS device for the same current could be regarded as an advantage, where we can use high currents and hence have higher output power without strongly overdriving the gate.

This last point might be also regarded as a disadvantage as the circuit consumes more power before the condition of oscillation is reached. To explain the advantage of this lower

gain, we consider a high performance VCO. By high performance we mean high spectral purity which usually dictates high output voltage swing. For a certain inductor value, usually defined by the required tuning range and the parasitic capacitance, the output swing can only be increased by increasing the current. For such high bias current the VCO open loop gain could be much higher than one and some sort attenuation is usually used in the feed back network to reduce the total gain. This attenuating network is common in bipolar designs, and one might argue that it is not needed in NMOS because one could simply use a smaller size NMOS transistor and have less parasitics. This will however increase (1/f) noise. The large PMOS size could still however be regarded as the main disadvantage there, which adds extra capacitance and reduces the tuning range.

4 Differential Charge Pump with Common Mode Control

In this section we present a new charge pump common mode control architecture, suitable for use with the differential VCO proposed in section 3.

Before describing the new architecture we try to briefly explain the need for common mode control in a differential charge pump driving a differential VCO. Because of the unavoidable mismatches between the NMOS and PMOS current sources forming the charge pump, there would be a net current going to the loop filter even when the PLL is in lock. This current causes the two differential control voltages to drift independently. The loop will, however, only correct for any differential, but not common mode, signal. The common mode could then drift freely and saturate the charge pump. Another effect of the common mode drift that is specific for our differential VCO architecture, is that it should be kept around 1.5 volts or lower so that it doesn't saturate the VCO.

A common problem with different common mode control schemes is the lack of a clean reference that the common mode signal could be locked to. The noise on this reference line is directly coupled to the output. It is also desired not to have this common mode control circuit on all the time so that we don't lose the important advantage of the charge pump which should ideally turn off when the PLL is in lock.

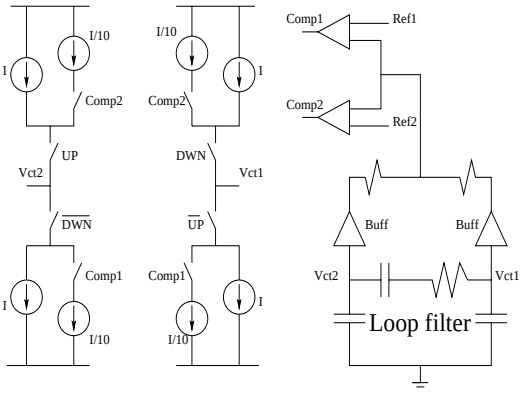

Figure 6: Proposed differential charge pump architecture

The architecture proposed in fig. 6 doesn't actually attempt to tie the common mode of the control signals to a fixed reference, it, instead forces the common mode signal between two closely spaced references. This guarantees that neither the charge pump nor the VCO gets saturated. The noise of these two references is not critical as the control circuit works in an open loop mode, and is totally off most of the time because the common mode drift is a relatively slow process.

The full operation can be explained as follows. Two simple source follower buffers are used with two summing resistors to detect the common mode value of the two control signal. This signal is then fed to a tristate comparison stage, which uses two simple comparators together with two references to generate two output signals. Both signals are zero as long as the common mode is between the two references. Once the common mode drifts beyond this range, one of the comparators will output a one signal, which is used to add an intentional offset to either the positive or the negative current sources depending on weather the common mode is to be pushed up or down. The offset (common mode control) current is switched on only when the charge pump is active. The value of the offset current is designed such that it provides enough current to push the common mode to the midway between the two references in one PLL reference frequency cycle. Care should however be taken that it doesn't push this common mode beyond the two references which might cause the common mode control loop to oscillate around the two references and never actually get between them.

5 Circuit Design and Simulation Results

Both the VCO and charge pump circuits were integrated with a simple phase frequency detector and a frequency divider in a test PLL chip. The VCO was designed for a center output frequency of 1.25GHz. According to H-spice simulation results the tuning range was about 250MHz. This tuning range was enough to achieve the desired 1.25GHz output and 25MHz tuning range around it for all processes corners, temperature and supply variations from $0-70^{\circ}$C and 2.7-3.6 volts, respectively. Using 0.5 μm CMOS process and a supply voltage of 3.0 volts the VCO core draws 3.6 mA. The differential amplifier for the buffering stage consumed 440 μA. The VCO output was capacitively coupled to a 2.1 mA simple open drain differential stage that drives a 50 Ω load for testing. Parallel to this buffering stage another source follower stage was used to drive the capacitive prescaler inputs. The stage consumed 1.0 mA. It is important to notice that the capacitive coupling of the output is necessary in this case because the DC level of the VCO output varies with the control signal.

For the differential control input the buffering stage A1 was designed with large PMOS input transistors in order to minimize its flicker noise contribution [9]. They were also biased at relatively high currents to reduce their thermal noise. The buffer closed loop BW, determined by the compensation branch (C_a and R_a), is 4 MHz within which the differential control common mode rejection is above 1,000. This BW is well beyond the PLL loop BW and should reject any common mode noise within the loop BW. This is also important to avoid degrading the PLL stability due to the extra pole. The settling time of the VCO output due to the buffer loop transients is around 100 ns, which is much faster than the loop transients . The resistance R_{ct} together with C_f acts a low pass filter for the direct control signal V_{ct1} with a BW equal to that of the other control signal, in order to slow down the common mode rejection degradation for higher frequencies.

With VCO output tuned for 1.25 GHz the third harmonic is almost -40dBc, while the second harmonic for a single ended output is -24dBc.

6 Phase Noise Estimation

The VCO phase noise output is caused by both internal and external sources. The internal phase noise is commonly estimated using Leeson's formula [5]

$$S_n(\Delta\omega) = \frac{1}{2}\frac{FkT}{C}\left[\frac{1}{4Q^2}\left(\frac{\omega_o}{\Delta\omega}\right)^2 + 1\right]\left[\frac{\omega_c}{\Delta\omega} + 1\right] \quad (1)$$

where F is the amplifier noise figure at full output, C is the oscillator output power, Q is the resonator quality factor, ω_o is the oscillation frequency, $\Delta\omega$ is the offset frequency at which the noise is to be calculated, and finally ω_c is the $1/f$ noise corner of the amplifier.

The factor $\frac{FkT}{C}$ represents the thermal noise to signal power ratio of the VCO amplifier. The quantity in the first brace represent the noise shaping due to the selective feedback circuitry, where the 1.0 accounts for the thermal noise floor away from the center frequency. The second brace accounts for the amplifier $1/f$ flicker noise. It is also important to note that the 1/2 factor at the beginning takes care of the fact that only 50% of the shaped noise power acts as phase modulation (PM) while the rest is amplitude modulation (AM) [10]. The contribution of different thermal noise sources to this relation in a typical oscillator has been also addressed[7].

The phase noise due to external sources, or the varactor modulation noise, could be described using the small phase deviation index approximation of the phase modulation theory which relates the single sideband noise modulation power, normalized to 1 Hz, to the carrier power as [6]

$$\begin{aligned} S_{n\_varactor}(\Delta\omega) &= \frac{1}{2}\Delta\phi^2_{rms} \\ \Delta\phi_{rms} &= \frac{\Delta\omega_{rms}}{\Delta\omega} \\ \Delta\omega_{rms} &= 2\pi V_{n\_var\_in\_rms} K_v co \end{aligned}$$

or

$$S_{n\_varactor}(\Delta\omega) = \frac{1}{2}\left(\frac{2\pi V_{n\_var\_in\_rms} K_{vco}}{\Delta\omega}\right)^2 \quad (2)$$

The factor $\frac{1}{2}$ is the asymptotic value of the first order Bessel function, representing the frequency components of a phase modulated (PM) signal, for small phase deviations. K_{vco} is the VCO gain defined as the output frequency change per one volt change in its control input. It should be noted that the above equation is valid only for small values of phase deviation ($\Delta\phi_{pk} \ll 1$ rad.), which should always be the case for the type of applications we are aiming at. The control circuit was designed very carefully to minimize the effect of this varactor modulation noise.

In order to estimate the output phase noise, the VCO core is simulated in an open loop condition using linear Hspice AC analysis to get the equivalent output noise voltage. This equivalent voltage is then used to calculate the value of the factor F in Leeson's formula as

$$F = \frac{V^2_{noise}}{kTR_p} \quad (3)$$

Where R_p is the equivalent parallel tank resistance at the oscillation frequency. Using a tank inductance of 4.3nH and a total capacitance of 3.77pF at the center frequency of 1.25GHz the equivalent tank Q was estimated to be 5.7 and $Rp = 189\ \Omega$. This leads to a calculated factor F of 20 and a phase noise of around -100dBc@100kHz offset frequency.

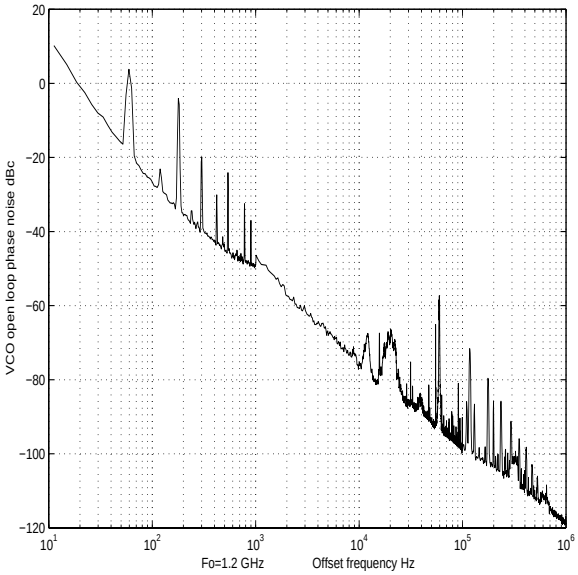

Figure 7: The measured open loop VCO phase noise at carrier frequency of 1.2GHz

To estimate the noise added by the control circuitry we also use ac analysis of the control buffer to calculate its noise contribution. The simulated thermal noise level at the varactor input was around 5.7 nV/$\sqrt{Hz}$ with (1/f) noise corner frequency of 11 kHz. For a VCO gain of 85 MHz/volt the varactor modulation noise was estimated to be -109dBc@100kHz, which means only 0.5dB degradation in the phase noise.

7 Measurement Results

Fig. 7 is a plot of the measured VCO phase noise. The values of -99dBc@100KHz and -119dBc@1.0MHz are very close to simulated ones. This confirms that the contribution of the control circuit is very small. Fig. 8 shows the differential VCO tuning range from 1.115 GHz at -0.2 volts (varactors slightly forward), to 1.440GHz at 3.0 volts. Changing the common mode of the control voltage from .2 volts to 1.7 volts has changed the output frequency by only 140 KHz. This means excellent common mode rejection of more than 2000 at DC.

To test the charge pump architecture the loop was closed with fixed division ratio of 50. The input reference was sweeped from 22.35 MHz to 29.72 MHZ to cover the full VCO range. The loop did lock correctly over the whole range which means the common mode control architecture is functioning as designed.

The current consumption is 3.6mA for the VCO core, 0.44mA for the buffer OpAmp, 1mA for the prescaler buffer, 2.1mA for the output buffer and 0.1 mA for charge pump common mode control, all at 3 volt supply. The charge pump current was designed to be 0.3mA

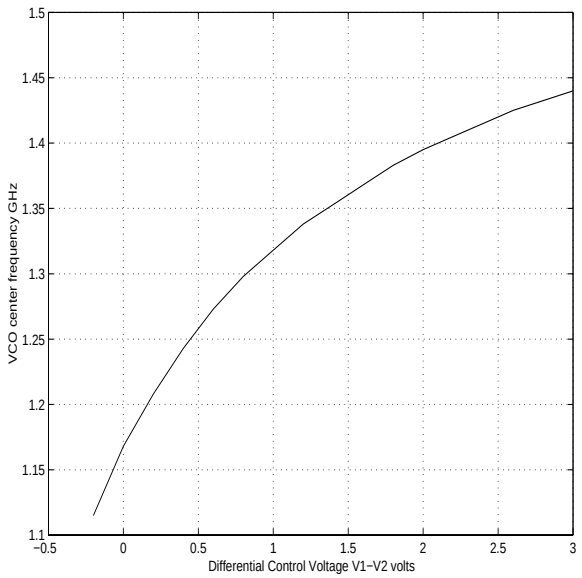

Figure 8: The measured VCO output frequency over the entire differential ($V_1 - V_2$) range

8 Conclusion

An Opamp buffer was successfully used to differentially control a CMOS LC-VCO with a very small degradation in the phase noise, and no reduction in the tuning range. The increase of the power consumption of the differential VCO over that of a single ended one is less than 10%. A simple open loop common mode control was used with a differential charge pump in a fully integrated PLL. The open loop nature of the common mode control circuit eliminates the need for a clean voltage reference and uses two crude reference instead. The differential control reduces sensitivity to supply, ground and substrate noise.

9 Acknowledgments

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