CMOS Front-End LNA-Mixer for Micropower RF Wireless Systems

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ABSTRACT

Motivated by the emerging needs for low power, low cost narrow-band wireless communication systems, the first micropower RFIC front-end has been implemented in standard CMOS technology. The front-end, an LNA combined with a down-conversion mixer, has been designed and fabricated in a HP 0.8 μm CMOS process. This mandates the use of high-Q discrete inductors to provide sufficient gain for the LNA. Employing these design methods, the front-end supply current is less than 110 μA with a 3V supply voltage for operation at 450 MHz. High-Q inductors have been manufactured using low-temperature co-fired ceramic (LTCC) technology. The front-end's gain is 25 dB with an IIP3 of -15 dBm. This is the lowest current consumption reported to date for a CMOS front-end operating at this frequency.

1. INTRODUCTION

Low power, embedded, wireless network devices are appearing in diverse narrow-band communication applications for messaging and embedded sensing and control [1,2]. These applications are characterized by requirements for efficient wireless communications at low data rate (less than 10 kbps) and short range (less than 100 m). Typical wireless nodes are equipped with sensing, location, tagging or low data rate messaging capability and are powered by compact battery cells. Short range and low data rate communication yield a significant reduction in the link budget requirements for such applications in comparison to traditional long-range wireless communication systems. However, due to the limitations of available compact battery power sources and the need for long operational life, these nodes must operate at both low peak supply current (less than 1 mA) and low average supply current (less than 100 μA). These stringent constraints, along with the requirement for low-cost CMOS implementation, motivate the development of new design methods for micropower CMOS RF transceiver components. This publication is a major step forward in micropower RF system development. The micropower RF VCO, presented previously at this conference, [3] indicated the potential for micropower CMOS RF. *However, this publication reports the complete micropower RF CMOS front end.* This successful development will provide essential capability for complete micropower transceivers.

As already demonstrated in previous work [3], a significant reduction in power dissipation of CMOS oscillators is achieved by the utilization of high-Q off-chip inductors. At a power consumption of 500 μW, the micropower VCO has a single side-band phase noise of less than –100 dBc/Hz (at 100 kHz offset frequency) with a tuning range of 10 %. While the performance is comparable with that of conventional CMOS high-power VCOs, the power dissipation has been reduced by at least a factor of 20. Continuing on the success of low power radio development, this paper reports advances in micropower CMOS LNA and mixer circuit implementations. This is the first report of a CMOS receiver front-end operating at center frequencies between 450 MHz and 1 GHz at a power as low as 330 μW.

The stringent supply energy limitation in micropower systems limits the MOS devices to operation with low bias currents. This leads to a reduction in transconductance and creates new challenges for high frequency circuit design. Steps must be taken to minimize the noise contribution of these low-gain components. The front-end reported here employs a high-selectivity LC preselector in front of an LNA to provide voltage gain and reject unwanted signals. The LNA is loaded with high-Q off-chip inductors and on-chip capacitors. The output of the LNA is capacitively coupled to a micropower CMOS double-balanced mixer on the same chip. Power dissipation is further reduced by allowing only high impedance circuit interfaces between the main RF circuit blocks. Performance meeting the requirements for embedded wireless network device applications is obtained through careful co-design of the front-end components.

The high-Q inductors are available either as low cost discrete components or embedded in low temperature co-fired ceramic (LTCC) substrate [4]. In each case, the cost of this off-chip integration is offset by the cost savings in silicon area for the

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large on-chip inductors, the reduction in required battery cost and increased system operating life. The cost and performance advantages of these off-chip inductors will be discussed in more detail later.

Based on these design principles, a micropower receiver front-end has been implemented in a standard CMOS process. For direct down conversion operation, the front-end displays a 25 dB voltage gain with 425 MHz RF and LO input signals while consuming only 110 μA. Although low power operation degrades the noise figure, the measured linearity performance compares favorably with other reported CMOS high power front-end receivers.

2. MICROPOWER CMOS LNA

The main challenge for micropower CMOS RF system development is that circuits must be optimized for operation at total power dissipation an order of magnitude less than conventional CMOS RF systems [3]. Dramatic power reduction may be obtained by developing circuits based on MOSs operating in the weak inversion region. However, design methods must be developed to mitigate the effects of low gain and high noise associated with micropower operation. By introducing high-Q inductive elements, it is demonstrated here that adequate gain and noise performances are achievable. A front-end transceiver components, LNA and mixer, are presented below.

Conventional design methods do not produce adequate gain and noise figure values for the micropower LNA at its frequency of operation [7]. Unlike conventional systems, this micropower LNA's gain does not depend heavily on the large transconductance of the input transistors. As shown in Figure 1, the LNA, incorporates a passive high-Q LC preselector at the input that provides both selectivity and a voltage gain of 8 dB. This preselector, which obtains its gain from resonance and exploits the impedance transformation between the LNA and antenna inputs, may be tunable, as has been shown possible for micropower VCO systems [2,3]. In addition, a LC network at the output of the LNA, by virtue of its high output impedance, also adds to the overall voltage gain of LNA. The combination of the input and output high-Q LC tank circuits, along with carefully chosen transistor dimensions, results in an overall voltage gain of 25 dB.

The LNA is based on a balanced cascode structure. The differential design provides immunity from common mode noise in the substrate. The cascode structure ensures adequate isolation from output to input, making the input matching network independent of the gain and output loads of LNA. The small cascode devices also assist in reducing the possibility of oscillation in the LNA. The LNA bias current is adjustable, allowing for adjustment of gain and power dissipation. By having the gate voltage sit well above the threshold level of the device, the linearity behavior of the devices are improved. Various transistor sizes were simulated to optimize the dimensions to achieve high linearity and high gain. The results indicate a trade-off between the preselector voltage gain and the LNA input transistor size. A larger device size will improve the intrinsic amplifier voltage gain. However, the resulted large input parasitic gate-source capacitance reduces the preselector gain. The LNA input transistors are chosen to be 30 μm wide. The overall gain and linearity performance of the front-end is further detailed in the measured result of Section 4.

The micropower LNA design methodology presented in this paper is applicable to both direct-conversion as well as heterodyne receiver architectures. However, unlike conventional transceiver design, which often requires 50 Ω interfaces, one of the keys to successful micropower system design is to prevent low impedance matching, as driving a 50 Ω load usually takes tremendous amounts of power. Therefore, the LNA and mixer circuits developed here will exploit high impedance circuit interfaces.

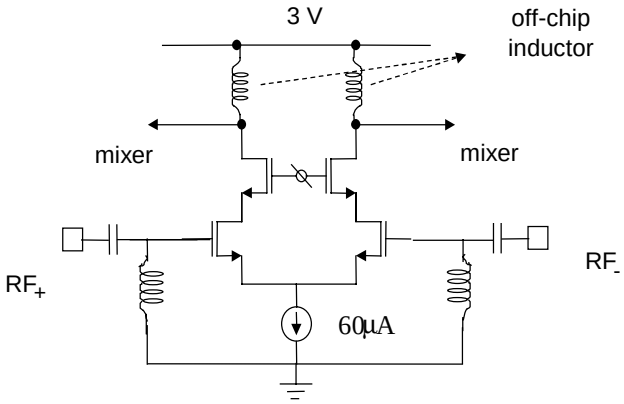


Figure 1. Circuit diagram of the LNA

Passive, high-Q inductors allow the LNA to produce adequate voltage gain with only μA current. Integrated on-chip passive inductors typically provide Q values of 3-5 at 1GHz in standard CMOS technologies [5,6]. These Q values are mainly limited by conductor resistance and eddy current loss in the silicon substrate. Off-chip inductors on low-loss substrates deliver much higher Q values. Our measurements show that inductors incorporated in ceramic substrates, such as low-temperature co-fired ceramic (LTCC), offer low-loss characteristics as well as packaging advantages. Compared with CMOS on-chip integration, the low-loss LTCC substrate, combined with low resistance conductors, provides a solution for high-Q low-power system implementation.

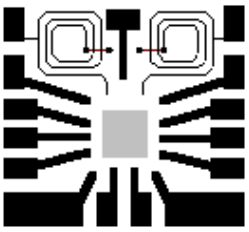


Figure 2. An example of a low temperature co-fired ceramic (LTCC) board layout.

In addition using discrete commercial chip inductors in the circuit, LNAs employing LTCC inductors are also under

development. Figure 2 shows a sample LTCC board layout for LNAs, which includes high-Q, low loss passive components, pads, and a cavity for housing multiple CMOS chip in a single substrate. With the low-loss, multi-layer capability of LTCC, the complete CMOS micropower RF front-end system can be built into a small board.

3. MICROPOWER CMOS MIXER

The implementation of the mixer circuit must balance the demands between conversion gain, linearity, noise figure, port-to-port isolation, and power dissipation. This micropower mixer design should also exploit the narrow-band nature of the intended communication systems in achieving low power operation.

Regardless of the IF used in the system, the baseband signal still has a very limited bandwidth, allowing the mixer to be used in either a direct conversion architecture (low or zero IF) or a dual conversion one (high IF). For a low frequency output, the bandwidth of the mixer output stage only needs to accommodate the low bit-rate signaling (10 kbps) required. This mixer will naturally reject the undesired high frequency output component due to its narrowband properties. For high-IF down-conversion, the unity gain frequency is expected to be far less than the IF, especially under low power operation. By tuning the mixer output to the IF with a high-Q LC tank circuit, adequate voltage gain can be obtained from this narrow band circuit without significantly increasing the power consumption. Therefore, with only minor modification, two mixer configurations are possible while sharing the same mixer design, permitting either a direct-conversion or high-IF receiver architecture.

Based on the above principles, the micropower mixer has been demonstrated for direct conversion (zero-IF) operation. The double-balanced Gilbert cell circuit, shown in Figure 3, is chosen for its fully differential structure and superior LO-IF isolation. This mixer alone draws only 22 μA at 3 V supply bias and has an output bandwidth greater than 100 kHz, which is sufficient for the target applications. Measurement of two-tone, third order intermodulation distortion yielded a value of –3 dBm for IIP_3 and the 1-dB gain compression point was measured to be –12dBm. Voltage conversion gain for the mixer was 12 dB for a 100 kHz output signal. It should be noted that the measure of power corresponds to power into an effective 50 Ω load. Actual circuit implementation and testing involves only high impedance loads to permit low power operation. By adding a high-Q LC tank circuit at the mixer output, the same circuit is able to perform high-IF down-conversion. Note that the high-IF mixer output is already band limited, thus, relaxing requirements on subsequent filtering.

As with all CMOS direct conversion mixers, 1/f noise dominates low frequency noise. However, due to the specific communication characteristics (short range, low bit-rate), combined with the introduction of large area input transistors in the mixer and sufficient gain from the LNA stage, the impact of mixer noise on the overall receiver is minimized. In considering linearity, CMOS mixers generally display better linearity performance than BJT mixers. This is due to the fact that MOST drain current depends quadratically on gate-source voltage, to a first-order approximation, while bipolar current depends exponentially on the base-emitter voltage. It is thus expected that the micropower mixer operating in weak inversion will show increased intermodulation distortion compared to strong inversion CMOS mixer circuits. However, it is demonstrated in this work that by proper sizing of the transistors, the effect of power reduction on linearity is minimized.

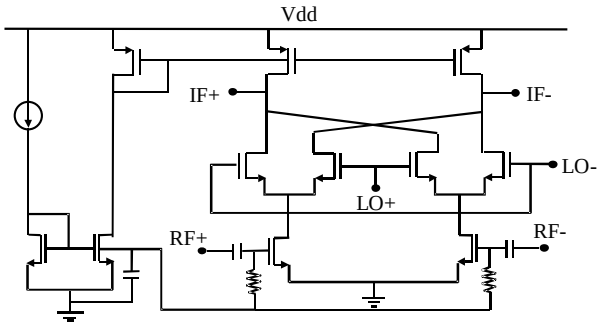


Figure 3. Mixer circuit diagram

4. FRONT-END MEASUREMENT AND RESULTS

The complete front-end combination of LNA and mixer consumes only 110 μA from a 3 V power supply. The front-end, with an input signal at 450 MHz, has 25 dB of differential gain, a noise figure of 19.5dB, input 1-dB compression of –25 dBm, and IIP3 of –15 dBm (at 25 kHz mixer output tone). These results meet the specifications for low power, short range communication for a large class of embedded wireless sensor applications [2]. Noise figure, dominated by 1/f noise contribution from the CMOS mixer, may be reduced for higher output tone frequencies. Figure 4 shows operation of the complete micropower front-end. The chip photo of the front-end is shown in Figure 5.

5. LOW POWER OFF-CHIP INTEGRATION

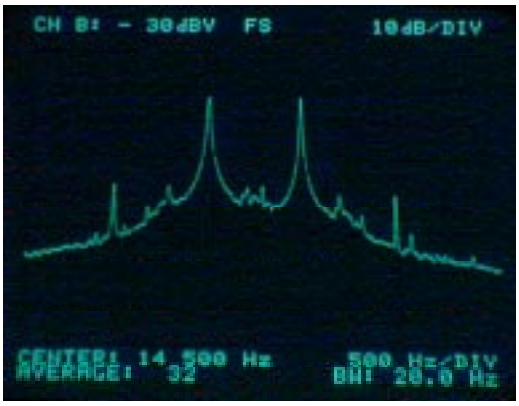
The decision of whether to use integrated on-chip passive components or discrete off-chip ones plays an important role in the transceiver implementation. For low power design, the chosen method must be able to recover performance degradation from low power operation. The results above show that the proper choice for power and performance is off-chip integration. Off-chip integration may first appear to present a cost disadvantage over on-chip integration. However, it is important to discuss the potential cost advantages of off-chip component integration.

On-chip passive inductors often suffer from substrate eddy current losses, reduced self-resonant frequency, and the possible requirements for non-standard wafer processing. (For example, post-wafer etching step.) For high power application, broadband radio modems, these low-Q circuits are compatible (or are required) for broad band fast hopping, and high process gain systems. In contrast, for narrowband embedded radio modems, the design choice should be optimized for low bit rate and should exploit high-Q circuits.

The cost associated with off-chip component integration in LTCC is offset by several issues: 1) Removing the passive components

from the lossy silicon substrate drastically reduces power requirements to obtain specified performance. Therefore the high system cost associated with batteries and their prohibitive replacement cost is reduced. 2) Removing large area passive components from the chip onto the low real estate cost substrate reduces the high cost associated with the large silicon area required for the large inductors. 3) Eliminating the requirements for non-standard CMOS technology modification required for inductors reduces development time. Finally, all RF CMOS integration methods will rely on packaging of the complete die or chipset. For packaging that relies on multichip modules, ceramic substrates, chip-on-board, and other methods, the low loss inductors reported here may be integrated with package. Thus, the incremental cost for adding low loss RF passives may be minimized.

The high-Q circuits reported here have been implemented successfully with off-chip components (either low cost discrete components or integrated into low temperature co-fired ceramic substrates). However, one must be careful in minimizing the parasitic loss due to off-chip integration. A common source of parasitic loss is the lossy substrate seen by the bond pads. The use of bond pads carrying a ground shield between pad and substrate can isolate the pads from the lossy substrate, thus, improving noise and power performance.



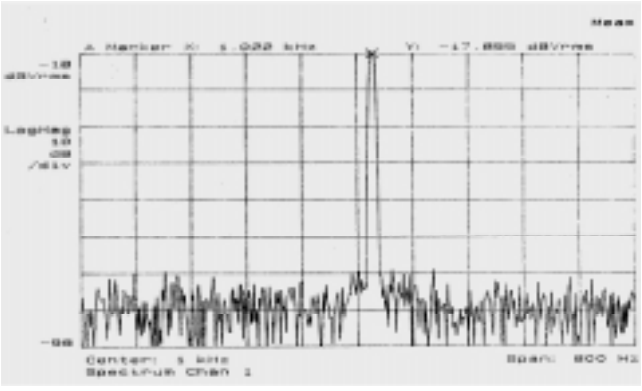


Figure 4. (a) Measurements of two-tone third order intermodulation distortion for the front-end. The front-end IIP_3 intercept is at –15 dB. (b) Example output spectrum showing the micropower front-end output operating as a direct conversion system. Here the input frequency is 450.001 MHz and the local oscillator frequency is 450.000 MHz, yielding the 1kHz output tone.

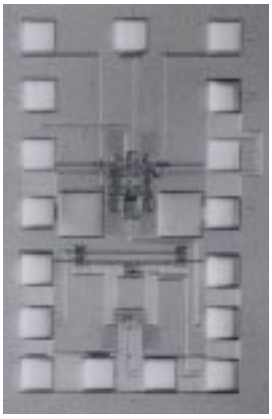


Figure 5. The front-end chip photo

6. CONCLUSION

A micopower front-end RFIC, comprising a low-noise amplifier and down-conversion mixer, has been designed and fabricated in 0.8µm CMOS. Performance at this micropower level meets the requirements for narrowband, embedded wireless communicators. The front-end performance is enabled by design methods that depend on high-Q inductive components. These results will now enable implementation of a complete front end integrated with the baseband portions of a direct-conversion receiver, all sharing a common CMOS substrate.

In summary, with the successful operation of the micropower CMOS LNA and mixer reported in this paper and the previous demonstration of CMOS VCOS [3], the primary components for the embedded radio have been implemented in low cost CMOS technology.

7. ACKNOWLEDGMENTS

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