

# Realizable Reduction for RC Interconnect Circuits

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## Abstract

*Interconnect reduction is an important step in the design and analysis of complex interconnects found in present-day integrated circuits. This paper presents techniques for obtaining realizable and accurate reduced models for two-port and multi-port RC circuits. The proposed method is also particularly suitable for interconnect reduction for nonlinear circuit simulation and for interconnect post-processing in a parasitic extractor. The method has two limitations. First, it only considers the first few moments of the transfer function; however, that is accurate enough for RC circuits. Second, the amount of interconnect reduction is topology dependent. Although, most on-chip interconnect topologies are well suited for the method proposed. Accuracy and efficiency of the proposed method is demonstrated for various realistic examples.*

## 1. Introduction

Interconnect effects are critically important in the design and verification of integrated circuits. On-chip interconnects are typically modeled by linear resistive (R) and capacitive (C) elements. For global nets (i.e., nets connecting one macro to another macro) the interconnect delay can typically be much greater than the logic delay. Even among nets within a macro, the interconnect delay can constitute a significant portion of the path delay (i.e., typically up to 25%).

Model reduction takes an original linear circuit and reduces it to a much smaller linear representation while maintaining much of the circuit performance. Model reduction has been an area of considerable research over the last several years, with a lot of the work originating from Asymptotic Waveform Evaluation (AWE) [1]. AWE computes the moments of the original circuit and then matches these moments to a reduced-order transfer function using Pade approximation. Along with the moment matching techniques, AWE, and later RICE[4], proposed an efficient way of computing the circuit moments by repeated DC solutions. The repeated DC solutions to compute moments causes the accuracy of the moments to decrease as the number of moments increase. Several techniques, notably using Krylov-subspace methods [3][6][7][8], were developed to increase the accuracy of the model reduction procedure. Krylov-subspace methods can match a much higher number of implicit moments yielding to much higher accuracy. These techniques are also more suitable for analyzing the frequency response of linearized analog circuits. Block Krylov-subspace methods were developed to handle multi-port circuits, however these methods typically work well only when the number of ports is less than ten. Krylov-subspace methods match the original circuit to a set of state equations that describe the reduced circuit. However, the reduced-order state equations may not be passive or realizable. Techniques in [14] and [6] extend the Krylov-subspace methods to guarantee passivity of the reduced-order state equations. However, these methods do not guar-

antee the realizability of the reduced circuit equations. Realizability of the reduced-order models has been shown for single-port circuits[13][15]. Uniform transmission lines can be matched to reduced-order non-uniform lumped segments by numerical least-squares techniques[17]. Techniques for determining reduced models for line structures via Gaussian Quadrature through circuit-element distribution moments are presented in [16].

Realizable model reduction is particularly useful in interconnect analysis. In a typical design methodology, various circuit analysis and verification procedures (e.g., static timing, dynamic simulation, noise analysis, circuit checking, power analysis, etc.) are performed on the extracted parasitic data. If the model reduction of the parasitic data is not realizable, it produces reduced transfer functions or reduced state equations and not reduced RC circuits. Hence, all downstream circuit simulators and associated programs have to be modified to handle reduced-order equations. Realizable reduced models are even more useful when both linear and nonlinear parts of the circuit have to be analyzed together. Furthermore, several circuit analysis programs (like circuit checking) only work if the input is in form of an RC circuit.

Apart from realizability, another significant problem in interconnect analysis is the large number of ports. For example, RC circuits originating from clock and power distribution networks may have hundreds of ports. For on-chip interconnects, addressing the need for an increase in number of ports is often more important than increasing the order of the approximation. On-chip interconnects do not require a large number of moments to produce accurate results. However, they often do have a large number of ports. Model reduction of these circuits will yield a dense reduced-order model which can be prohibitively expensive to analyze in downstream circuit analysis tools. The matrix factorization of a dense matrix is order  $O(n^3)$ , whereas the matrix factorization of a sparse matrix is order  $O(n^{1.5})$ . For the case of circuits with a large number of ports, the simulation with reduction may often take longer than simulation without reduction.

This paper presents realizable model reduction and linear circuit partitioning techniques to address the problems discussed in the previous two paragraphs. A multi-port circuit is first partitioned into a set of two-port circuits. This partitioning maintains the spatial sparsity of the original circuit. Each two-port circuit is then reduced to an equivalent and realizable RC circuit. Instead of assuming a transfer function or state equations as the model for the reduced system, a representative RC circuit is assumed as the model for the reduced system. The model reduction procedure consists of computing R and C element values for the assumed reduced-order circuit. Closed-form expressions are derived to compute the element values. The realizability and passivity of the reduction procedure is proven. Interconnect reductions of each two-port circuit are reconnected to

yield the final reduced circuit. This procedure works exceeding well for most on-chip interconnects. The procedure presented in this paper does not handle coupling capacitors.

Moments of the transfer function need to be computed for each two-port network. The moments can be computed by setting appropriate excitation and by performing matrix factorization[1]. The moments can also be computed by a linear-time path tracing technique, which is more efficient for large original circuits.

The paper is organized as follows. Section 2 presents the realizable model reduction procedure for two-port circuits. Circuit partitioning into a set of two-port circuits is described in Section 3. Results for representative industrial circuits are presented in Section 4, followed by Conclusions and Future Work.

## 2. Reduction Procedure

The behavior of any two-port circuit can be completely described by its transfer function matrix,  $Y(s)$ . Let  $I_1$  be the current into port 1,  $V_1$  be the voltage across port 1,  $I_2$  be the current into port 2, and  $V_2$  be the voltage across port 2. The transfer function can be written as:

$$\begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix} = \begin{bmatrix} Y_{11}(s) & Y_{12}(s) \\ Y_{21}(s) & Y_{22}(s) \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} \quad (1)$$

Traditional reduction procedures model the exact transfer function,  $Y(s)$ , with an approximate transfer function,  $\hat{Y}(s)$ . The computation of moments (explicit or implicit) of the original circuit is the first step in the reduction procedure. These moments are then matched to an assumed model to get the reduced circuit equations. The reduced model is usually another set of state equations or another transfer function. Hence, it is difficult to convert these reduced circuit equations to a realizable circuit. For realizable reduction, it is better to assume another smaller RC circuit as the reduced model. The proposed reduction procedure consists of computing the numerical values of the elements in the assumed RC circuit.

The choice of the reduced RC circuit is an important part of the realizable reduction procedure. The reduced RC circuit should share the same properties as the original RC circuit. For the case of on-chip interconnects, the following assumptions can be made for the original RC circuit:

- The original multi-port circuit has been partitioned into set of connected two-port RC circuits.
- Each two-port RC circuit has no DC path to ground.
- Each two-port RC circuit has a DC path from one port to its other port.

Most on-chip interconnects exhibit the above mentioned properties and partition nicely into set of two-port circuits. Given this set of assumptions for the original circuit, the circuit shown in Figure 1 is chosen as the reduced circuit. Realizable reduction is possible if one can:

- Compute the values of circuit elements ( $R_1, R_2, R_m, C_1, C_2$ ) from the moments of the original circuit.
- Demonstrate that all circuit element have positive values, i.e.,  $R_1 > 0, R_2 > 0, R_m > 0, C_1 > 0$  and  $C_2 > 0$ .

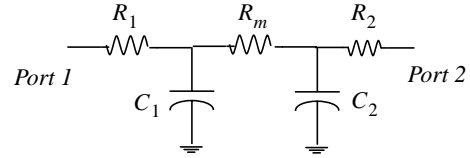


Figure 1 Reduced RC circuit model.

### 2.1. Computing the RC values for the Reduced Model

The transfer function of the original circuit can be expanded into its moments

$$Y(s) = \begin{bmatrix} (y_{11})_0 & (y_{12})_0 \\ (y_{21})_0 & (y_{22})_0 \end{bmatrix} + \begin{bmatrix} (y_{11})_1 & (y_{12})_1 \\ (y_{21})_1 & (y_{22})_1 \end{bmatrix} s + \dots \quad (2)$$

The first two expansion terms of the transfer function are used to compute the element values of the reduced circuit. The first two expansion terms contain eight moments. However, the following relationships among these eight moments are always true:

- $(y_{11})_0 = (y_{22})_0 = -(y_{12})_0 = -(y_{21})_0 > 0$
- $(y_{12})_1 = (y_{21})_1$
- $(y_{11})_1 > 0, (y_{12})_1 > 0, (y_{22})_1 > 0$
- $(y_{11})_1(y_{22})_1 - (y_{12})_1^2 > 0$

Given these relationships among the first eight moments, there are only four truly independent moments in Equation (2). The first independent moment is  $(y_{11})_0$  from the zero-order term, and it is simply the inverse of the effective resistance between the two ports with all capacitors open-circuited. Three additional independent moments are  $(y_{11})_1, (y_{22})_1,$  and  $(y_{12})_1$  from the first-order term. These three first-order moments each have the dimension of capacitance, and they are each equal to weighted sums of capacitances in the original two-port circuit. Define a dimensionless variable  $x_k$  at every node  $k$  in the original two-port RC circuit as follows:  $x_k$  is the resultant voltage when a unit voltage source is applied at port 2 with port 1 grounded and all capacitors open-circuited. Thus,  $x_k = 0$  at port 1,  $x_k = 1$  at port 2, and  $x_k$  equals some intermediate value at each internal node. The moments  $(y_{11})_1, (y_{22})_1,$  and  $(y_{12})_1$  are each equal to weighted sums of all capacitances in the original two-port RC circuit, where the weighting factors are given respectively by  $(1-x_k)^2, x_k^2,$  and  $x_k(1-x_k)$ . The total capacitance of the original two-port RC circuit is equal to  $(y_{11})_1 + 2(y_{12})_1 + (y_{22})_1$ . The Elmore delay from port 1 to port 2 is equal to  $[(y_{12})_1 + (y_{22})_1]/(y_{11})_0$ , and the Elmore delay from port 2 to port 1 is equal to  $[(y_{12})_1 + (y_{11})_1]/(y_{11})_0$ .

The assumed reduced-order circuit in Figure 1 has five elements (three resistors and two capacitors). The circuit elements are rewritten in terms of four independent variables. A single dimensionless parameter  $k$  is introduced that relates the values of the two capacitors. Alternatively, the capacitor values are written as

$$C_1 = (1-k)C \text{ and } C_2 = (1+k)C. \quad (3)$$

For the reduced circuit to be passively realizable, the following conditions must be true:

- $R_1 > 0, R_m > 0, R_2 > 0$

- $C > 0$
- $-1 < k < 1$

The parameter  $k$  may be viewed as a “realizability parameter” since only a range of values for this parameter will yield a realizable circuit. The parameter  $k$  is not an independent variable. It is considered to be a fixed value during moment matching, so that the number of truly independent circuit variables and the number of unique moments are both equal to four. Later, it will be shown how a value for  $k$  can always be chosen ahead of time to guarantee realizability and passivity of the reduced circuit.

The four independent moments of the original circuit from Equation (2) are symbolically matched to the corresponding moments of the reduced circuit in Figure 1. This set of equations can then be symbolically inverted to solve for  $R_1$ ,  $R_2$ ,  $R_m$  and  $C$  in terms of  $(y_{11})_0$ ,  $(y_{11})_1$ ,  $(y_{12})_1$ ,  $(y_{22})_1$ , and the fixed parameter  $k$ . The following expressions are obtained for  $R_1$ ,  $R_2$ ,  $R_m$  and  $C$ :

$$C = \frac{1}{2}[(y_{11})_1 + 2(y_{12})_1 + (y_{22})_1]$$

$$R_m = \frac{2 \sqrt{\frac{D}{1-k^2}}}{(y_{11})_0[(y_{11})_1 + 2(y_{12})_1 + (y_{22})_1]}$$

$$R_1 = \frac{(y_{12})_1 + (y_{22})_1 - \sqrt{D} \sqrt{\frac{1+k}{1-k}}}{(y_{11})_0[(y_{11})_1 + 2(y_{12})_1 + (y_{22})_1]}$$

$$R_2 = \frac{(y_{12})_1 + (y_{11})_1 - \sqrt{D} \sqrt{\frac{1-k}{1+k}}}{(y_{11})_0[(y_{11})_1 + 2(y_{12})_1 + (y_{22})_1]}$$

where  $D = (y_{11})_1(y_{22})_1 - (y_{12})_1^2 > 0$ .

The next step is to demonstrate how to compute a value of  $k$  which guarantees realizability. By examining the numerators of expressions for  $R_1$  and  $R_2$ , two boundary values for parameter  $k$  can be computed:

$$k_1 = \frac{((y_{12})_1 + (y_{22})_1)^2 - D}{((y_{12})_1 + (y_{22})_1)^2 + D} \quad (5)$$

$$k_2 = \frac{D - ((y_{12})_1 + (y_{11})_1)^2}{((y_{12})_1 + (y_{11})_1)^2 + D} \quad (6)$$

When  $k = k_1$ ,  $R_1$  is zero. When  $k = k_2$ ,  $R_2$  is zero. Any choice of  $k$  in the range  $k_2 < k < k_1$  yields a passively realizable reduced-order circuit model, since it can be shown that the relationship  $-1 < k_2 < k_1 < 1$  always holds. In the reduction procedure, we choose the average value:

$$k_r = \frac{k_1 + k_2}{2} \quad (7)$$

Or, expressed in terms of the original circuit moments:

$$k_r = \frac{[(y_{22})_1 - (y_{11})_1][(y_{11})_1 + 2(y_{12})_1 + (y_{22})_1]}{[(y_{12})_1 + (y_{22})_1]^2 + D} \cdot \frac{[(y_{12})_1 + (y_{11})_1]^2 + D}{[(y_{12})_1 + (y_{22})_1]^2 + D} \quad (8)$$

### 3. Linear Partitioning and Spatial Latency

Linear circuit partitioning is essential during model reduction. A general multi-port circuit is partitioned into a set of two-port circuits. Partitioning into a set of two-port circuits maintains the spatial latency of the original circuit. If circuit partitioning is not performed, traditional model reduction will yield a dense reduced circuit. Once the original circuit has been partitioned into two-port segments, the model reduction technique described in Section 2 is applied to each individual two-port segment. Often, each individual two-port segment in the partition may correspond to a line structure in the original multi-port circuit, but this is certainly not a requirement. The model reduction technique described in Section 2 works equally well for a two-port segment that is not a line (e.g., it may contain loops). The final reduced circuit is obtained by recombining the individual reduced circuits.

It should be noted that interconnect partitioning schemes can also be used in conjunction with previous model reduction procedures. However, the resultant reduced circuit may not be realizable.

### 4. Results

The efficiency and accuracy of the reduction procedure is illustrated through various industrial examples.

| Circuit | Number of Nodes | % Reduction | Accuracy (Percentage Error) |                 |
|---------|-----------------|-------------|-----------------------------|-----------------|
|         |                 |             | Delay (%)                   | Output Slew (%) |
| ckt1    | 6               | 33.3%       | -0.45%                      | 1.62%           |
| ckt2    | 10              | 60.0%       | -0.80%                      | 3.65%           |
| ckt3    | 32              | 76.92%      | -0.17%                      | 0.71%           |
| ckt4    | 65              | 81.13%      | -0.03%                      | 0.23%           |
| ckt5    | 152             | 95.52%      | -0.19%                      | 0.94%           |
| ckt6    | 250             | 94.52%      | -0.14%                      | 0.70%           |
| ckt7    | 502             | 96.38%      | -0.60%                      | 0.21%           |
| ckt8    | 774             | 98.25%      | -0.28%                      | 0.50%           |
| ckt9    | 1681            | 99.50%      | -0.54%                      | 1.87%           |
| ckt10   | 5924            | 99.74%      | -0.23%                      | 0.73%           |
| ckt11   | 10211           | 99.85%      | 0.09%                       | 1.17%           |

Table 1 Reduction percentage and timing accuracy for the proposed method.

Table 1 shows the amount of reduction and the accuracy of the model reduction procedure. Circuits denoted by ckt5, ckt8, ckt9, and ckt11 also have loops. The accuracy is defined as a percentage error in the circuit waveforms between the circuit with no reduction and the circuit with reduction. The accuracy data shown in the table are worst-case errors for the set of all primary inputs and primary outputs for a given circuit. As seen from Table 1, the proposed method provides high reduction percentage (from 33.3% to 99.85%) with very high accuracy (with the worst case delay error being -0.80%, and worst case slew error being 3.65%). As expected, the model reduction procedure works better for larger circuits.

Table 2 shows the efficiency of the model reduction procedure as measured in CPU run time. The table compares the total simulation run time of the circuit with no reduction with the run time of the circuit with reduction. Simulations of both the original circuit and the reduced circuit are performed by Backward Euler numerical integration with tight local truncation error control. The simulation time for the reduced circuit also includes the moment computation time and the reduction time. As seen from the table, significant speedup is obtained. The simulation time for the reduced circuit is shown for two different cases. In the first case, the moments of the original circuit are computed through matrix (LU) factorization and forward and backward substitution (FBS). In the second case, the moments of the original circuit are computed through a linear-time path tracing method.

| Circuit | Number of Nodes | Simulation Time (No Reduction) (in seconds) | Simulation Time (with Reduction) (in seconds) |              |
|---------|-----------------|---|---|--------------|
|         |                 |   | Matrix Method                                 | Path Tracing |
| ckt1    | 6               | 0.01  | 0.01  | 0.01         |
| ckt2    | 10              | 0.01  | 0.01  | 0.01         |
| ckt3    | 32              | 0.03  | 0.01  | 0.01         |
| ckt4    | 65              | 0.07  | 0.02  | 0.02         |
| ckt5    | 152             | 0.16  | 0.03  | 0.03         |
| ckt6    | 250             | 0.38  | 0.04  | 0.04         |
| ckt7    | 502             | 0.75  | 0.04  | 0.04         |
| ckt8    | 774             | 1.59  | 0.06  | 0.05         |
| ckt9    | 1681            | 4.48  | 0.10  | 0.05         |
| ckt10   | 5924            | 11.16                                       | 0.22  | 0.07         |
| ckt11   | 10211           | 23.09                                       | 0.54  | 0.11         |

Table 2 Efficiency of the model reduction procedure.

## 5. Conclusions and Future Work

Realizable interconnect reduction techniques for on-chip RC interconnects have been presented in this paper. The original circuit is first partitioned into set of two-port circuits to maintain the spatial sparsity of the reduced model. Each two-port circuit is matched to a reduced RC circuit, instead of reduced state equations as in previous techniques. Efficient closed-form expressions are derived for computation of the element values of the reduced RC circuit. Efficiency and accuracy of the reduction technique has been shown for various industrial circuits. Future work includes modifying the proposed reduction procedure to handle interconnect circuits which contain coupling capacitors.

## 6. References

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