Low Power Techniques for Digital GaAs VLSI

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Abstract

This paper presents a survey of low-power digital Gallium Arsenide logic applicable to high performance VLSI circuits and systems and proposes new design concepts in methodology and architecture based on implementation of Pseudo-Dynamic Latched Logic in order to achieve reasonable power-delay-area tradeoff. The approach is highly suitable for self-timed systems where the complexities of clock skew are avoided and power saving is achieved through pipelined architectures. The emergence of low-power Complementary HIGFET (C–HIGFET) technology enables the realisation of new high performance low-power architectures. The viability of neu-GaAs (νGaAs) as applied to C–HIGFET is discussed and the concept of 'soft' hardware referred as 'flexware' is introduced as a new design paradigm for GaAs.

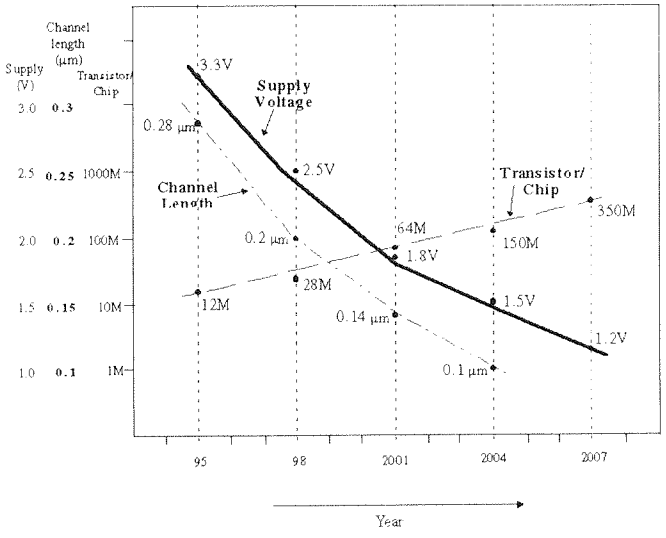

Figure 1. Integration complexity road map for deep submicron silicon technology.

1. Introduction

Over the past several years, CMOS technology has become the dominant fabrication process for cost effective VLSI circuits and systems. Therefore much of the efforts in recent years directed towards enhancement of performance is generally related to optimisation of speed, chip area, power dissipation in particular for low voltage applications, and testability. Silicon-on-Insulator (SOI) CMOS has shown much promise because of the reduced parasitic capacitance and improved transistor characteristics for low-power and low-voltage applications. Figure 1 illustrates the scaling process and the expected outcome for digital silicon technology by the way of a complexity road map [12]. Thus, from the road map it is evident that there has been a systematic approach by the silicon IC industry not only to improve the fabrication process but also to use scaling as a main step for improving the figure of merit for the silicon-based technology. However, a number of complex problems are to be encountered as part of such developments. These include non compliance of threshold voltage behaviour with scaling and more seriously, the mismatch of gate oxide at 0.1 micron and beyond, where the oxide will have to be replaced with new materials. This poses a major challenge, since conventional oxide and its unique passivating properties have been responsible for the success of the silicon MOS technology as we know it today [10].

In order to meet the ever-increasing performance requirements, some parallel technological changes have also taken place in the area of Gallium Arsenide (GaAs). GaAs channels have significantly higher gain for the same transistor capacitance than silicon channels. This means GaAs transistors dissipate about 4 to 5 times less power than equi-

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valent CMOS SOI gate being clocked at the same rate. Gallium Arsenide technology is the second most used compound, after silicon in communication and related industries. New investments and efforts will not alter this order of preference. However, there are a number of specialised niches such as new generation of personal interactive multimedia mobile communications systems [2] where GaAs can show its capability. Advantages of GaAs over silicon include important optoelectrical properties, higher temperature tolerance and higher radiation hardness which make the technology highly suitable for applications such as the future nanosatellite technology.

The new performance challenge requires new innovations in circuit techniques as well as new approach to architectures that are matched to the technology. The first part of this paper deals with characteristics of MESFET based circuits for low power high performance applications. The second part looks at the Complementary HIGFET (C–HIGFET) and the related performance and design methodology, as well as new possibilities of νGaAs as the foundation for a new paradigm of '*soft*' hardware based circuits.

2. Low Power MESFET Logic

MESFET technology is composed of Enhancement and Depletion (E/D) transistors. The main difference with the CMOS transistor is the presence of a Schottky barrier at the gate of the transistor. This imposes a restriction in the logic swing of the basic logic gate and hence in its noise margin [13]. Most GaAs designs are restricted to static logic, which suffer from high power dissipation because, unlike CMOS, in static GaAs gates, depending on the state of the output, there can be a continuous current flow from the power supply to ground. Recently introduced Pseudo Dynamic Latched Logic (PDLL) [6], as illustrated in Figure 2, has shown a good compromise for high speed and low power consumption for synchronous and asynchronous systems.

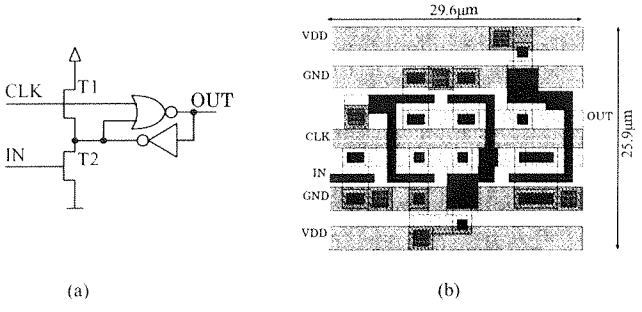

Figure 2. (a) PDLL latch schematic, (b) Layout.

A number of PDLL circuits have been designed and fabricated using a 0.6 μm E/D MESFET technology, ranging from shift registers, barrel shifters, PLAs and Carry Lookahead Adders (CLA) to Read Only Memories (ROM). All of them have exhibited very low power dissipation at high clocking speeds as shown in Table 1.

Table 1. PDLL circuits performances

Circuit	Frequency	Power Diss.
4-b Barrel Shifter	0.5 GHz	2.2 mW
$4 \times 8 \times 8$ PLA	0.5 GHz	10 mW
4-b CLA Adder	0.8 GHz	2.8 mW
1-Kb ROM	0.5 GHz	24 mW

The PDLL structure can be modified by removing the precharge transistor T_1 shown in Figure 2 resulting in Latched Coupled FET Logic (LCFL) [11]. The logic provides for slightly lower power dissipation at the expense of reducing the amount of logic that can be implemented per stage. LCFL is a 'quiet logic' which means perturbation to the power distribution buses can be kept to a minimum during switching.

One of the most complex tasks when designing high speed synchronous systems is the clock distribution and minimization of clock skew in the clock delivery network. The synchronizing clock signal affects nearly all parts of the system. The difference in arrival times of fanned-out clock signals (clock skew) affects the behaviour of the system. This difficulty is enhanced when two phases are required as it is the case for PDLL/LCFL based circuits. Moreover, the clock distribution system can dissipate a considerable amount of power, reaching up to 40% of the total power dissipation of the system. Self-timed systems solve the clock skew problem at the expense of increased circuit complexity. The GaAs Muller-C element is the core building block used in the two-phase and four-phase handshake protocols for asynchronous architectures. As an example, the basic structure for a self-timed shift register that has been designed using a 0.6 μm E/D MESFET process as shown in Figure 3.

The handshake path, when compared to a standard four-phase handshake protocol, is such that a particular LCFL logic cell is not permitted to enter into the *reset* state until the following cell completes its evaluation. Furthermore, it cannot perform the next evaluation until the cell following it enters the *reset* state. This handshake protocol operation removes the need for separate latches between logic stages.

3. Complementary HIGFET Technology

In the long term, emergence of new GaAs technologies provide further reduction in static power dissipation,

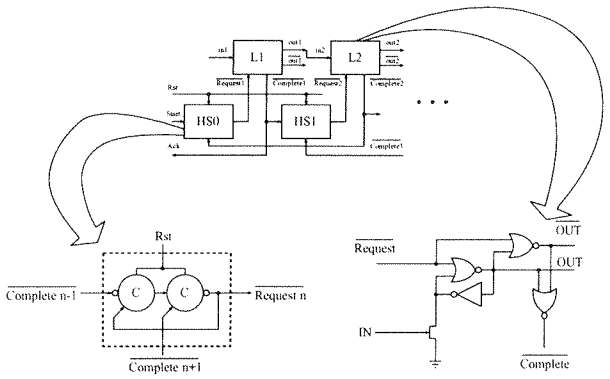

Figure 3. Self-timed LCFL GaAs shift register.

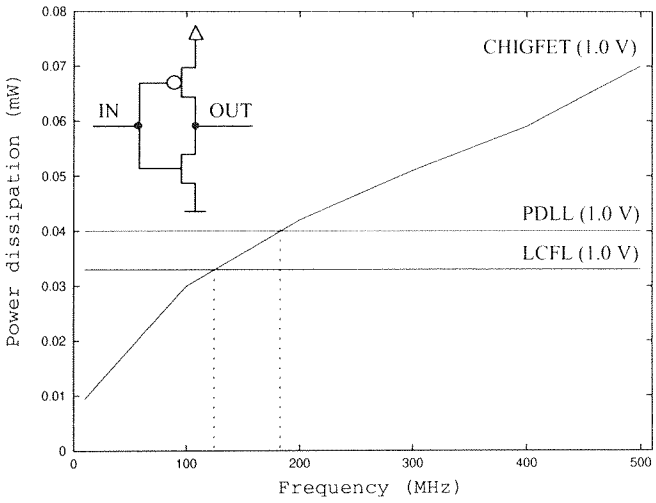

Figure 4. Power Vs. frequency estimation for C–HIGFET, PDLL and LCFL.

mainly by using Heterostructure Insulated Gate FETs (HIGFETs) [7], anisotype FETs [8] and the recently announced MOS-GaAs [4] using a mixture of gallium oxide and gadolinium oxide $Ga_2O_3(Gd_2O_3)$. However, in the short term, complementary GaAs based on HIGFET transistors appears to be the most likely option in terms of low power performance. The flexibility provided by this technology in terms of circuit design options, together with the ability of adjusting speed and power characteristics by varying power supply from 0.9 to 1.5 V, permit the designer to construct optimum architectures. Thus, full-complementary logic is used when low power dissipation is the goal, demonstrating speed-power performance as low as 0.01 μW/MHz/gate at 0.9 V and 0.1 μW/MHz/gate at 1.2 V for circuits such as SRAMs, multipliers and microprocessor cores [5]. Design for speed can be accomplished by mixing silicon ECL like source-coupled logic (SCFL) with the forementioned full-complementary logic, showing 0.4 μW/MHz/gate for a signal processor circuit with SCFL and complementary blocks operating at -4 V and -1.2 V respectively. Further reduction in power supply (from -4 V to -2.5 V) permits a figure of merit of just 0.16 μW/MHz/gate while maintaining the same frequency of operation [1].

We have performed simulations for full complementary HIGFET (C–HIGFET) gates based on a composite parameter set derived from a number of complementary GaAs processes. Figure 4 shows power dissipation versus frequency for 0.5 μm C–HIGFET and a scaled version of 0.4 μm MESFET technology for PDLL/LCFL.

It is apparent from the power vs. frequency characteristic of Figure 4 that for low frequencies (from DC to around 125 MHz), C–HIGFET provides a good option for battery operated systems. PDLL and LCFL show little variation with frequency due to their small dynamic power dissipation component, and hence, are highly suitable for frequencies above 200 MHz. Furthermore, as long as the number of devices continue to increase, the use of automated tools become indispensable in order to reduce time-to-market. In this scenario, a new design methodology based upon Ring Notation [9] has shown to be an effective approach that takes into consideration the organisational aspects of Power and Ground lines in relation to high-speed signal paths. Ring Notation also creates new possibilities for automated layout of such circuits and provides the designer with a topological information permitting early detection of asymmetries and path imbalances in the physical design. Translation from Ring Notation to symbolic and hence to mask is rather straight forward as it is illustrated in Figure 5 for the case of a C-HIGFET NOR gate.

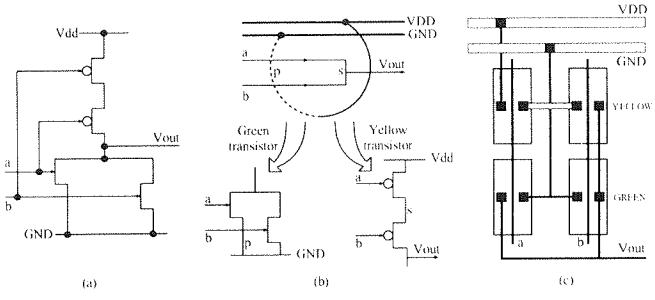

Figure 5. C–HIGFET NOR gate (a) schematic, (b) Ring diagram, (c) symbolic layout.

4. Neu-GaAs (νGaAs)

The neu-GaAs transistor was first investigated in [3] and was inspired by the neu-MOS (νMOS) transistor, recently discovered by Shibata and Ohmi [14] in 1991, which uses capacitively coupled inputs onto a floating gate. The resulting output is simply a weighted sum of the inputs, due to the capacitive input network, followed by a thresholding operation. The behaviour of the transistor resembles that of a biological neuron where the turn-on of the transistor is parallelled by the firing of a neuron. νMOS or νGaAs circuits operate with mixed mode analog/digital functions and can perform Boolean logical operations that are dynamically reconfigurable. This means the notion of 'soft' hardware, referred as 'flexware', becomes a new design possibility for reconfigurable architectures. The use of ν-circuits greatly increases functionality/area while still maintaining low cost via the use of standard fabrication.

The νMOS concept has enabled the design of conventional digital and analog circuits, in standard CMOS, with a factor of 5-10 decrease in gate count. Furthermore, νMOS/νGaAs circuit characteristics are insensitive to transistor parameter variations but instead rely on coupling capacitor *ratios*. Due to the greater functionality per unit area available in νGaAs, interconnect lengths are also greatly reduced as a by-product of this methodology. Hence, νGaAs is very promising as a low power technology which is attractive for smart sensors in mobile applications.

Preliminary results demonstrate functional νGaAs 3-bit A/D converters with a factor of 4 reduction in gate count and power dissipation reduction over a factor of 50 over conventional complementary GaAs layouts.

5. Conclusions

Gallium Arsenide has continued to remain as a definite contender for low power/high speed architectures due to its superior power–speed performance. In this paper, PDLL/LCFL class of logic based upon the combination of the strength afforded by static and dynamic logic families is presented. The logic is capable of operating in the 500 MHz to 1 GHz range at low power and low supply voltage. Extension of the PDLL/LCFL logic structure permits their application in self-timed systems basically to overcome the clock distribution complexity. Emergence of technologies such as complementary HIGFET promise new possibilities for low power/high speed portable equipment such as mobile interactive multimedia communicators.

6. Acknowledgements

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