A Novel Low Power Low Phase-Noise PLL Architecture for Wireless Transceivers

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Abstract

A sample-and-hold stage placed in the feedback path of a PLL frequency synthesizer reduces the division ratio, and hence the phase-detector phase-noise, without the need of multiple loops. When used in conjunction with a DDS, this architecture simplifies the DDS design leading to a low-power architecture. Furthermore, this architecture allows for a large loop bandwidth thus suppressing the VCO phase-noise. The advantages of this architecture are highlighted and system- and circuit-level simulations presented.

1. Introduction

The frequency synthesizer is one of the most critical blocks in a wireless transceiver. On one hand its performance directly affects the transceiver's noise figure, image rejection and spurious emission, and on the other hand, the VCO is very sensitive to interference, especially in systems that transmit a high power such as the narrowband-PCS network of Mobitex (2W).

In a classical PLL-based frequency synthesizer for a wireless transceiver, the reference frequency to the PLL is equal to the channel spacing. This often leads to a large division ratio causing the close-in phase-noise to be dominated by the noise from the phase detector. Thus the loop bandwidth must be reduced to attenuate this noise in the range of interest.

The bandwidth must also be small for adequate spurious suppression. Whether a classical or a fractional-N PLL is used, a spurious signal appears at a frequency equal to the channel spacing. The bandwidth in both architectures is usually one decade below the channel spacing in order to sufficiently attenuate the spurs.

Since the PLL has a small bandwidth, the loop does not attenuate the VCO phase-noise in the range of interest. Thus the stringent phase-noise requirements can be met only by resorting to an off-chip high-Q oscillator. This results in higher power consumption, large size and more importantly, greater interference problems.

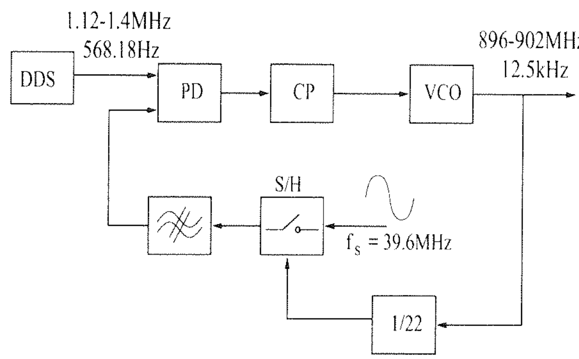

Figure 1. Proposed PLL architecture.

One technique to solve these problems is to use a digital frequency synthesizer (DDS) to drive a PLL [2]. By operating the DDS at a high frequency, the division ratio is reduced and hence the contribution of the PD to the phase-noise. Also, the spurious signals will be located at the high frequency of the DDS output. Thus, the bandwidth can be increased in order to inhibit the phase-noise of the VCO, while maintaining good spurious rejection. The problem with this architecture is that the high frequency of operation of the DDS results in higher power consumption and greater difficulty in designing the DAC at the DDS output. Another problem with this architecture is the large resolution needed in the DDS. Regardless of the division ratio used, the resolution of the DDS will be determined by the ratio of the output frequency to the channel spacing. For Mobitex, the channel spacing is 12.5kHz and an 18-bit DDS would be necessary.

In this paper we propose a novel architecture that

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reduces the division ratio while using a low-frequency, low-resolution (and thus low-power) DDS [1]. In addition, the bandwidth of the architecture is relatively large allowing for the integration of the VCO, and significantly reducing interference problems.

2. PLL architecture

The proposed architecture is shown in Fig. 2. The specific frequency bands selected where designed for Mobitex, which has a transmission band of 896-902MHz with a channel spacing of 12.5kHz. The phase-noise requirement is -95dBc/Hz at 10kHz offset.

The VCO output is divided down to an intermediate frequency using a simple, low-power fixed-modulus counter. The output of the divider then samples a fixed-frequency sinusoidal signal f_s, and the beat frequency is filtered by a low-order LPF. By placing the sampling mixer after the frequency divider, the reference signal needed (f_s) is of a low frequency and thus could be derived from a crystal oscillator. This alleviates the need of an extra PLL/VCO or mixers like the double-loop PLL architecture [3].

The significant advantage of this architecture is the reduction of the division ratio while maintaining a low operating frequency for the DDS. The division ratio in Fig. 1 is only 22 versus 644 if the sampling mixer was not used. This provides more than 29dBc attenuation of the phase-noise from the phase-detector and DDS signal. This will also influence the number of bits needed for the DAC of the DDS, since the quantization noise of the DAC translates into phase-noise [2]. This significantly reduces the DAC power consumption.

Another important advantage of this architecture is the DDS size and power consumption. The VCO output is converted down to the 1.4MHz range with a division ratio of only 22. Thus the DDS will have to provide a resolution of 568.18Hz with a clock of approximately 3.5MHz. Hence only 13 bits of resolution will be sufficient versus 18 bits if no mixing was employed. This leads to a significant reduction in the DDS size and power consumption. In addition to reducing the division ratio, this architecture has a relatively high reference frequency (1-1.4MHz as opposed to 12.5kHz in a classical PLL). This allows for a large bandwidth while maintaining low spurious. A bandwidth of 100kHz will still be one decade less than the spurious frequency while providing nearly 40dBc attenuation of the VCO phase-noise at 10kHz [4]. This makes the use of on-chip VCOs, which usually have low quality factors, possible and thus greatly reduces the interference problems as well as avoiding the extra buffers needed to drive external 50-Ohm terminations. The large bandwidth is also beneficial in that it provides a fast switching time.

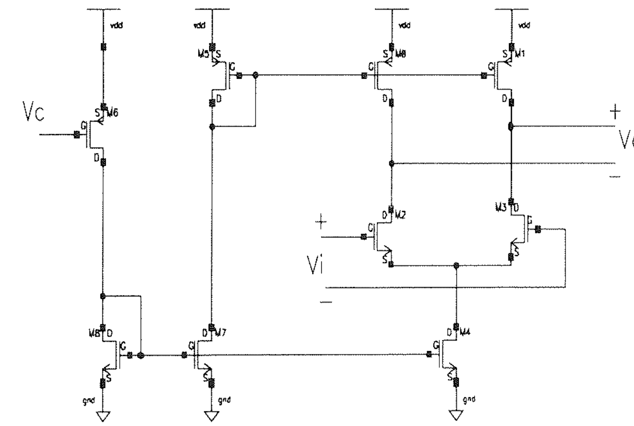

Figure 2. Ring VCO stage.

3. Circuit Design

The proposed architecture, apart from the DDS, was implemented in $0.35\mu m$ CMOS technology. The VCO used was a three stage ring oscillator shown in Fig. 2. Both the tail bias current and the load current sources are a function of the control voltage. This yields an amplitude that is fairly constant over frequency. The center frequency was 1GHz, the gain approximately 80MHz/V and the power consumption 2.8mA. The sampler and filter combination are shown in Fig. 3. A passive sampler architecture consisting of capacitors and switches was used. This architecture consumes very little power and is adequate for our application. Since the sampled signal has a relatively low frequency (less than 100MHz), the capacitor, C, can

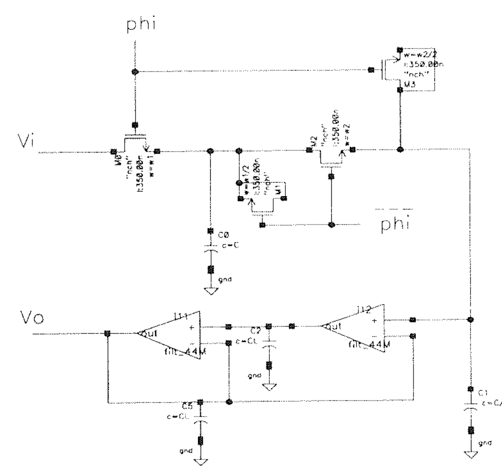

Figure 3. Sampler/filter circuit diagram.

be made large while maintaining an adequate tracking bandwidth. This results in low clock feedthrough and charge injection. To reduce these effect further, dummy switches were also added.

The filter is realized by simply cascading two opamps. The finite gain-bandwidth product, ω_t, of each opamp results in a first-order filtering action, with the BW_{3dB} determined by the load capacitance. If the gain of the opamp is A, then the filter transfer function is

$$\frac{v_o}{v_i} = \frac{1}{1 + 1/A + 1/A^2} \tag{1}$$

For an opamp with a single dominant pole,

$$A = \frac{1}{1/A_o + s/\omega_t}. \tag{2}$$

Assuming $A_o >> 1$,

$$\frac{v_o}{v_i} = \frac{1}{1 + s/\omega_t + (s/\omega_t)^2}. \tag{3}$$

Note that due to the fashion the opamps are connected, the Q of the transfer function is equal to 1 as opposed to 0.5 in the case of a cascaded RC sections. Fig. 4 shows the outputs of the sampler and filter for a 40MHz sinusoide sampled at 38MHz. The filter consumes 570μA from a 3.3V supply.

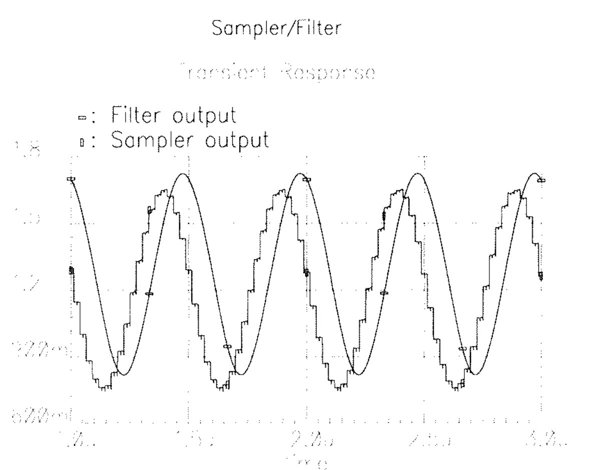

Figure 4. Output of sampler and filter.

4. Simulations

The system of Fig. 1 was simulated using Simulink from Matlab. The loop bandwidth was set to 67.5kHz and the damping factor 0.707. The transient response of the loop, for a 6MHz frequency step, is shown in Fig.

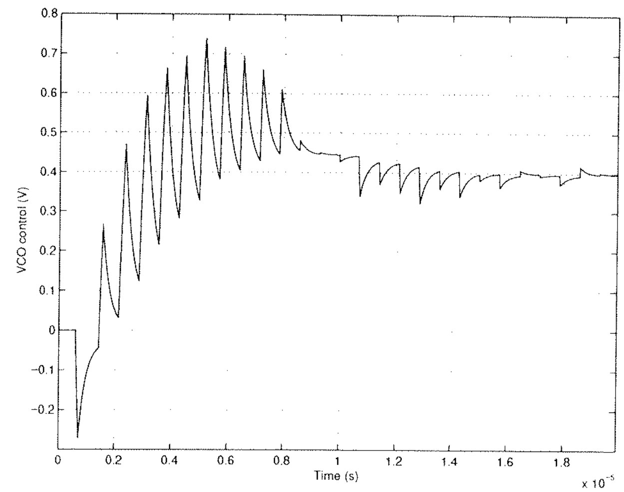

Figure 5. Matlab simulations of the VCO input for a 6MHz frequency step.

5. As shown, the response follows that of a second-order system with the expected natural frequency.

The spectrum of the VCO output is shown in Fig. 6. In this case, a simple 1-st order LPF was used after the sampling mixer to reject the harmonics. As shown, the spurs are approximately -55dBc down. These spurs could be further reduced by using a higher-order LPF, or by reducing the loop bandwidth.

The suppression of the VCO phase noise was also simulated. For a bandwidth of 67.5KHz, it is necessary to use an excessively large number of points for FFT in order to get a sufficient resolution. Thus the loop parameters where changed in order to increase the loop bandwidth. The VCO output was 899MHz and sampled at 80MHz. The reference to the phase-detector was 9.9MHz and the bandwidth was set to 2MHz. In order to simulate the VCO phase-noise, three equal tones were injected in the VCO phase at 0.8MHz, 2MHz and 7.83MHz. Fig. 7 shows the VCO output when configured in the loop. As shown the tone within the loop bandwidth was attenuated by approximately 18dB, while the one outside the bandwidth was not attenuated. The tone at 2MHz increased by approximately 3dB. This is attributed to the peaking of the transfer function around the bandwidth.

Hspice post-layout simulations were conducted on the complete circuit design. The loop natural frequency was set to 285kHz, and the reference input to the phase detector was at 3MHz. The transient response of the charge-pump output, for a 32MHz frequency step, is shown in Fig. 8. The complete circuit consumes 8.6mA from a 3.3V supply.

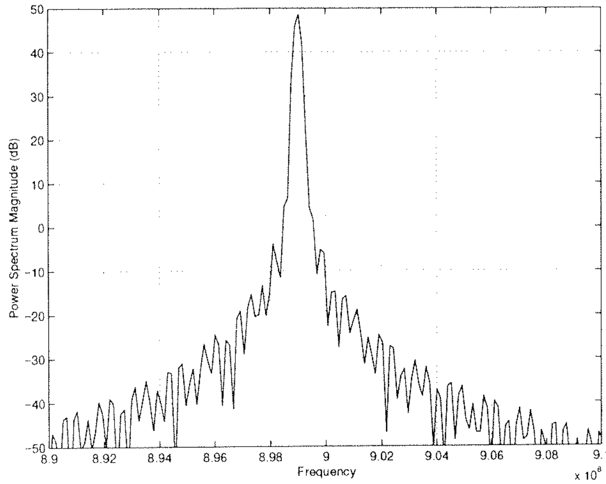

Figure 6. VCO output spectrum.

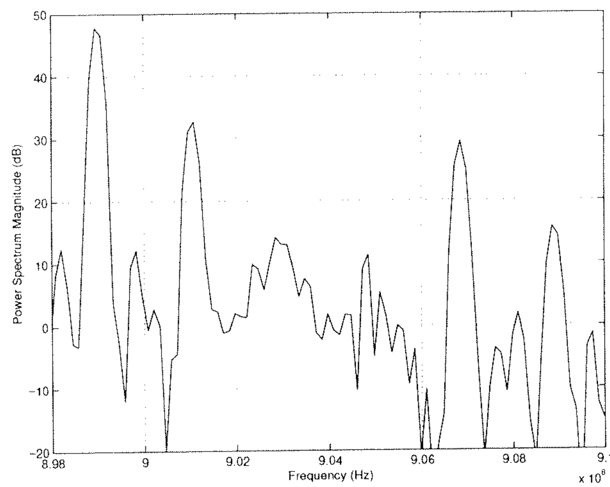

Figure 7. Loop suppression of the VCO noise.

5. Conclusion

A novel PLL architecture in which the divided VCO output samples a fixed-frequency signal was proposed. This architecture greatly reduces the division ratio, thus attenuating the phase-noise due to the phase detector and input reference, without the use of extra loop or mixers. Also, if a DDS is used to provide the reference, it will have a significantly fewer number of bits. In addition, the reference frequency to the PLL is relatively high allowing for a large loop BW and thus lower VCO phase-noise contribution. The architecture was designed in a $0.35\mu m$ CMOS process and consumes only 8.6mA from a 3.3V supply.

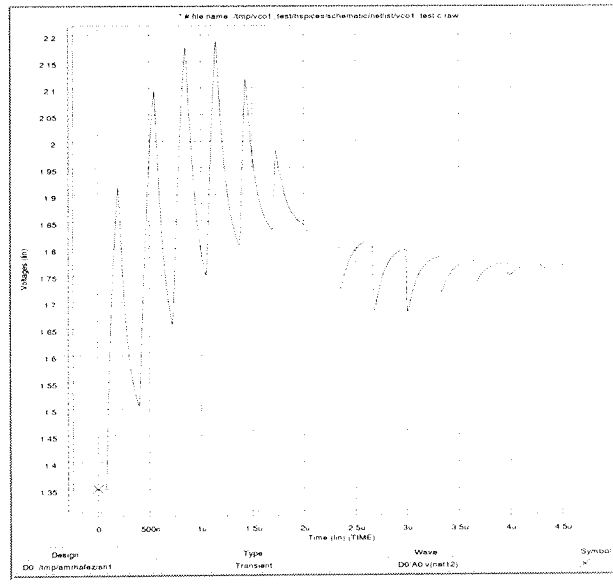

Figure 8. Hspice simulation of the VCO control for a 32MHz frequency step.

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