VHDL Design of a Test Processor Based on Mixed-Mode Test Generation

Md.Altaf-Ul-Amin and Zahari Mohamed Darus
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia

Abstract

This paper presents the VHDL design of a prototype test processor, which can be used for functional testing of digital ICs. The design of the test processor supports itself to be controlled by a microcomputer. The processor can generate mixed-mode (pseudo-random followed by deterministic) test vectors and can apply them to circuit under test (CUT). The test processor also receives the output responses of the CUT and compresses them to a signature. The signature is then sent to the computer for comparison. The test processor supports the testing of combinational as well as sequential circuits (with scan-path).

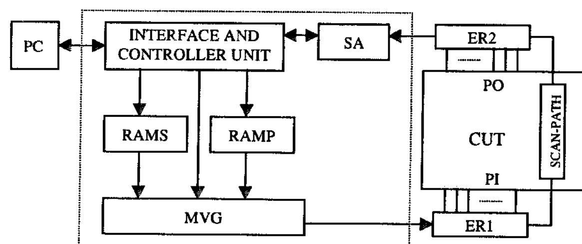
1. Introduction

In functional testing, the functionality of an IC is verified by applying test vectors at its inputs and by observing its output responses. Test vectors can be primarily classified into four types: *exhaustive, deterministic, pseudo-random and mixed-mode.* Whatever be the type of test vectors, for actual testing of an IC, it requires to either store them in memories or to generate them by some hardware (usually LFSR) before applying them to the CUT. For efficient testing of an IC, it is necessary to select the proper type of test vectors and at the same time the proper technique for their hardware generation and/or application to CUT. Factors, such as storage data volume, test application time, hardware area, hardware complexity, fault coverage, programmability etc. are considered for hardware generation of test vectors. In the present work, mixed-mode test vectors are generated based on multiple polynomial multiple seed linear feedback shift register (MPMSLFSR) scheme.

Mixed-mode test vectors consist of pseudo-random and deterministic test vectors. In mixed-mode testing, pseudo-random test vectors are first generated to cover large percentage of easily testable faults and deterministic test vectors are then generated to target random pattern resistant faults. To generate a specific deterministic test vector based on MPMSLFSR scheme, using an n-bit LFSR, a primitive polynomial of degree n is first selected. Then an appropriate n-bit seed is calculated. If no seed is found then another polynomial is considered and so on. It has been mathematically derived that the probability of not finding a seed to generate a test vector with n specified bits in an n-stage LFSR with 16 polynomials is less than 10^{-6} [1].

2. Architecture of the test processor

The functional block diagram of the test processor is shown in Figure 1. The mixed-mode vector generator (MVG) is a 32-bit LFSR. The LFSR can be loaded with 16 polynomials and 32 seeds one by one with one seed and one polynomial at a time. The first seed and the first polynomial are supposed to be used to generate pseudo-random vectors. All 16 polynomials can be used to generate deterministic vectors. The seeds are arranged in groups for specific polynomials and an "extra-bit" is added to each seed to indicate whether the feedback polynomial has to be changed while the next seed will be loaded to the vector generator. The signature analyzer (SA) is also a 32-bit LFSR with feedback polynomial $x^{32}+x^{28}+x^{27}+x+1$, which is a primitive polynomial of



RAMS: Seed storage RAM
RAMP: Polynomial storage RAM
MVG: Mixed-mode vector generator
SA: Signature Analyzer
ER1 & ER2: External registers
PI & PO: Primary inputs and outputs of the CUT

Figure 1: Functional block diagram of the test processor with a CUT

0-7695-0104-4/99 $10.00 © 1999 IEEE

degree 32. This is a serial input internal EOR type signature analyzer. The RAM blocks (RAMS and RAMP) are used to store seeds and polynomials. The interface and controller unit mainly consists of several state machines and a 40-bit long instruction register (IR). The IR contains information about the test-length for pseudo-random testing (19-bit), test length for deterministic testing (5-bit), the number of primary inputs plus scan-path registers of the CUT (8-bit) and the number of primary outputs plus scan-path registers of the CUT (8-bit). Two external registers ER1 and ER2 are to apply the test vectors to the primary inputs of the CUT and to capture the responses from the primary outputs of the CUT. The number of LFSR stages for MVG and SA, the number of stored seeds and the length of IR have been arbitrarily assumed for this prototype design and can be varied easily if required.

4. Operation of the test processor

Prior to testing a CUT the seeds and polynomials are written in the RAM blocks and the IR is loaded with necessary data as mentioned in previous section. Then the first seed and the first polynomial are loaded to MVG. The MVG starts to produce serially the bits of the first test vector which are shifted into ER1 and the scan-path. After shifting bits equal to the number of primary inputs plus scan-path registers, the vector is then applied to the CUT. In the next clock cycle the responses are loaded to the scan register and ER2. The responses are then serially shifted into the SA. Subsequently, the vector generator starts to generate the next vector and the process continues until the number of applied test vectors equals the number of predefined test-length for pseudo-random testing. Then the deterministic test vectors are generated by changing the seeds and the polynomials (if necessary). At the end, the content of the SA is sent to the computer to compare with that of a fault-free CUT. The test processor also generates the necessary control signals to enable and disable the external registers at appropriate moments.

5. Design methodology

The test processor has been designed using VHDL. VHDL supports both behavioral and structural modeling. Digital circuit models using VHDL need not to be exclusively behavioral or structural. Circuit designs that contain both behavioral and structural modeling are referred to mixed-mode modeling. A mixed-mode modeling technique has been used to design the test processor. The performance of the test processor has been verified using Mentor Graphics QuickHDL simulation tool. Later, the design has been synthesized and optimized using AutoLogicII from Mentor Graphics. AutoLogicII has also been used to generate the schematic of the design. Figure 2 shows the top page of the schematic of the test processor. FPGA implementation of the test processor is currently in process.

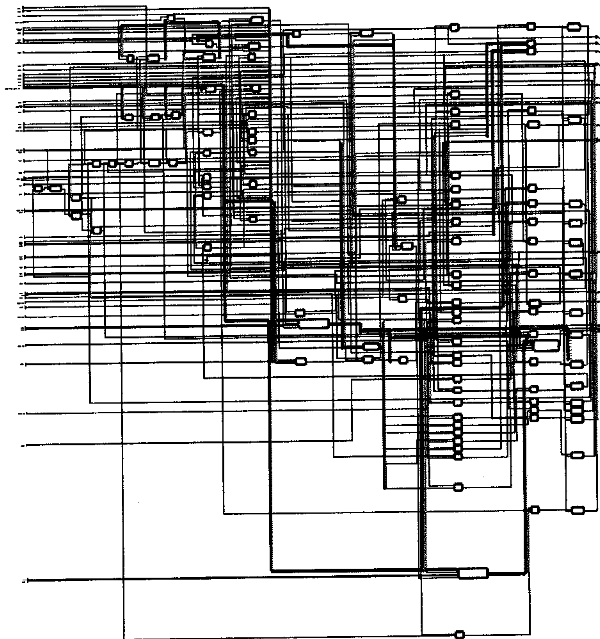


Figure 2. Top page of the Schematic of the test processor generated by AutoLogicII

5. Conclusions

A test processor has been designed using VHDL based on a well-known test generation technique. The test processor can be used to develop an external IC tester of reliable performance that supports the testing of combinational as well as sequential circuits (with scan-path).

Acknowledgements

The work presented here is supported by the Ministry of Science, Technology and the Environment of Malaysia under the Intensification of Research in Priority Areas (IRPA) grant (IRPA 04-02-02-0011).

Reference

[1] Hellebrand S., Rajski J., Tarnick S., Venkataraman S. & Courtois B. "Built-in test for circuits with scan based on reseeding of multiple-polynomial linear feedback shift registers". *IEEE Transactions on Computers*. Vol. 44, No. 2, pp. 223-233, February 1995.