A Novel High-Speed Flip-Flop Circuit Using RTDs and HEMTs

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Abstract

An RTD (resonant tunneling diode)-based flip-flop circuit with a new configuration is proposed. The circuit features an SCFL interface for both input and output, and achieves high-speed operation with a simplified configuration. The circuit consists of only two RTDs and three HEMTs, and works as a delayed flip-flop (D-FF) with return-to-zero (RZ) mode output. 50 Gbit/s operation is confirmed by SPICE simulation for the SCFL-interfaced D-FF with the proposed configuration. A static binary frequency divider (T-FF) is also designed based on the same concept. It is fabricated by InP-based RTD/HEMT integration technology, and its proper operation of up to 15 GHz is confirmed experimentally.

1. Introduction

The RTD-based circuit with MOBILEs (monostable-bistable transition logic elements) [1] is an effective means of providing high-speed logic circuits. So far, we have developed an RTD-based D-FF (35 Gbit/s), a T-FF (34 GHz) and a multiple-valued quantizer (10 Gbit/s), and showed the potential of MOBILE technology for various high-speed logic circuit applications [2-4]. However, while the MOBILE itself has been shown to be an ultra-high-speed device, there is still the problem of how to fabricate its interface without sacrificing its high-speed operation and simple configuration. In other words, in implementing an RTD-based circuit with MOBILE technology into conventional circuits, the issue is how to ensure the interface match between them.

In the two flip-flop circuits mentioned above, the clock signals are directly applied from an external signal source. In the multiple-valued quantizer [4], the HEMT, which works as a clock buffer, is serially connected with a pair of RTDs in the MOBILE, but the feasibility of this type of clock buffer is not clear for high-speed operation. We also demonstrated that the RTD-based MOBILE can drive the SCFL-type output buffer at high speed and the SCFL-interfaced output level is obtained [5]. But the input interface of the above-mentioned circuits has not matched with that of conventional circuits. This is because of the difficulties in designing an appropriate clock buffer that can drive the MOBILE at high speed.

In this study, we propose an RTD-based flip-flop circuit that features an SCFL interface for both input and output. Its performance is estimated by SPICE simulation, and 50 Gbit/s operation is obtained for a D-FF circuit whose configuration is based on the proposed concept. A static binary frequency divider is also designed with the same scheme, and proper operation of up to 15 GHz is confirmed experimentally.

2. Circuit design

For the proper operation of the MOBILE, large current (several mA) that is equal to the peak current (I_P) of the RTD is required (Fig. 1). One way to drive the MOBILE while satisfying the interface match is to supply the output of conventional circuits, for example, SCFL-type circuits. In this case, the MOBILE must be taken into account as the load resistor for the SCFL-type circuit, because the current flowing into the MOBILE is not negligible. As a result, the SCFL-type circuit must have sufficient current drivability to ensure high-speed operation with this scheme. However, such circuit design is not practical in terms of power dissipation. To solve the problem of how to drive the MOBILE while ensuring the interface match, without spoiling the feature of the MOBILE, or high-speed operation, a novel RTD-based flip-flop circuit is proposed.

2.1. RTD-based flip-flop with SCFL interface

The configuration of the proposed circuit is shown in Fig. 2. The circuit consists of two HEMTs, in addition to the MOBILE. One (Tr1) is for the clock input, and the other (Tr2) is for the current source. This configuration is similar to that of the source follower (SF) circuit. Thus, its interface can easily match those of the SCFL or SF circuits, which are widely used in FET-based digital ICs. The key point of the proposed circuit is that the clock buffer, which works as the MOBILE driver, is unified

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with the MOBILE itself. Therefore, the proposed circuit is regarded as a new type of the MOBILE, which features the SCFL interface.

Before we proceed to the operating principle of the proposed circuit, we explain that of the MOBILE in reference to Fig. 1. When the driving voltage, V_{drv} is smaller than $2V_P$ (V_P: the peak voltage of the RTD), the MOBILE is in a "monostable" state, and V_{OUT}, the output of the MOBILE, is 'low'. When V_{drv} is larger than $2V_P$, the MOBILE is in a "bistable" state, and whether V_{OUT} is to be 'low' (V_L) or 'high' (V_H) is determined by the relationship between the peak currents of two RTDs at the rising edge of V_{drv} (the edge triggered function). For example, when the peak current of RTD1 (I_{P1}) is larger than that of RTD2 (I_{P2}), RTD2 switches from the peak to the valley. Thus, V_{OUT} is 'low'. On the other hand, when I_{P2} is larger than I_{P1}, RTD1 switches from the peak to the valley. Thus, V_{OUT} is 'high'. Once the output is determined, it does not change while V_{drv} is 'high' ($> 2V_P$), even if the relationship of the peak currents changes (the latching property).

Now, the operating principle of the proposed circuit is explained. Note that the voltage difference, $|0 - V_M|$ corresponds to V_{drv} in the MOBILE in Fig. 1. For ease of explanation, we assume three conditions:

(i) The drain-source current of Tr2 (I_{SRC}) is set a little larger than I_P of the RTDs in the MOBILE,

(ii) V_{MCS}-V_{MSS} is set less than $2V_P$, and Tr1 and Tr2 have the same gate width.

(iii) I_{ds} is the product of the constant (voltage-independent) transconductance by ($V_{gs} - V_{th}$).

Here, V_{gs} and V_{th} are the gate-source voltage and threshold voltage of the HEMTs, respectively. Condition (i) ensures enough current ($\sim I_P$) is supplied to the MOBILE for switching the RTD, and condition (ii) guarantees that the MOBILE is in the "monostable" state when V_{CLK} has a certain value. The drain-source current of Tr1 (I_{CLK}) always satisfies the relationship $I_{CLK} + I_M = I_{SRC}$. Here, I_M (which is the function of V_M) is the current flowing in the MOBILE, and is larger than 0. Then, V_M always satisfies the relationship

$$V_{CLK} - V_M < V_{MCS} - V_{MSS}. \quad (1)$$

From Eq. (1) and condition (ii), when $V_{CLK} = 0$ V, the MOBILE is in the "monostable" state because $|0 - V_M| < 2V_P$. V_M decreases with a decrease of V_{CLK}, and $V_{CLK} - V_M$ also decreases at the same time, because I_M (V_M) increases with an increase of $|0 - V_M|$. Then, $V_{CLK} - V_M$ is minimized at $V_M = -2V_P$, because I_M takes the maximum value ($\sim I_P$) at that time. Therefore, I_M decreases with a further decrease of V_{CLK}. Thus,

$$I_{CLK}(V_{CLK} - V_M) > I_{CLK}(V_T - (-2V_P)). \quad (2)$$

Here, V_T is defined as V_{CLK} at $V_M = -2V_P$. From Eq. (2) and the condition $V_{CLK} < V_T$, the relationship $V_M < -2V_P$ is obtained. Thus, when $V_{CLK} < V_T$, the MOBILE is in the "bistable" state. Consequently, the monostable-bistable transition occurs in the MOBILE, and the proposed SCFL-interfaced circuit shows proper operation as the MOBILE-type circuit.

2.2. Static Binary Frequency Divider

We also designed a static binary frequency divider (T-FF) (Fig. 3). The T-FF consists of a clock buffer and an output buffer in addition to a core circuit made with two sub-circuits (SC1 and SC2). The clock buffer and output buffer are designed by SCFL technology, and the configuration of the core circuit is based on the proposed RTD-based flip-flop with the SCFL interface.

The operating principle of the two sub-circuits is the same as that of the flip-flop circuit described in the previous section. The output from SC1 is the complementary signal of the input. On the contrary, SC2 outputs the true signal of the input. In other words, SC1 works as a clocked inverter and SC2 as a clocked buffer. Thus, when the clock signal and its complementary signal are applied to the two sub-circuits, the core circuit works as a frequency divider. The operating principle of the core circuit is described in more detail elsewhere [3].

The designed T-FF contains a clock buffer that generates the complementary set of the clock signal. In our previous work [3], the circuit requires a two-phase clock from an external signal source, because the clock buffer had not been built in. Such a circuit configuration is not useful for practical application. However, in this study, the circuit does not require a two-phase clock because the clock buffer is integrated. The proposed circuit configuration featuring the SCFL interface enabled the integration of the conventional circuit and the RTD-based circuit.

3. Results

3.1. Circuit Simulation of D-FF

Figure 4 shows the configuration of the simulated circuit, which works as a D-FF circuit with RZ-mode output signal. The simulated circuit has an output buffer consisting of the SF and SCFL circuits. Thus, in addition to the input interface, the output interface matches the SCFL interface.

The circuit performance was investigated by SPICE simulation. The device model used in the simulation is as follows. The RTD was treated as a parallel circuit of the voltage-controlled current source (Grtd) and a capacitor (Crtd) with the voltage dependence. Schulman's model was used for the Grtd [6], and the experimental data were used for the Crtd. Here, the peak structure in the capacitance-voltage characteristics was not taken into account [7, 8]. The model of the HEMT is based on Curtice model.

The RTDs have V_P of 0.30 V, a peak current density

(j_p) of 9.4 X 10^4 A/cm^2, a peak-to-valley current ratio (P/V) of 5.5 and Crtd (V = 0) of 5.0 fF/μm^2, and the HEMTs have a gate length (L_g) of 0.1 μm, V_{th} of -0.40 V, and a transconductance (g_m) of 1.0 S/mm. The emitter areas of the upper and lower RTD in the MOBILE were 7.0 and 6.6 μm^2, respectively. The gate width of the HEMTs was 20 μm, except for that in the MOBILE, which was 10 μm.

The pseudo-random bit stream was used for the data signal in the simulation. 50 Gbit/s operation was obtained with a clear eye-pattern (Fig. 5). V_{MSS} and V_{SS} were -1.8 and -2.5 V, respectively. The estimated power dissipation is about 65 mW. The amplitudes of the clock signal and the data signal are 700 and 400 mV, respectively. The output voltage swing is about 420 mV. As the output voltage swing is larger than the amplitude of the input data, the proposed circuit has enough drivability along with high-speed operation.

3.2. Fabrication and Measurement of T-FF

The static binary frequency divider was fabricated by integrating InGaAs/AlAs/InAs RTDs and InAlAs/InGaAs HEMTs [9, 10]. Figure 6 is a microphotograph of the fabricated circuit. The RTDs have V_P of 0.37 V, j_p of 6.8 X 10^4 A/cm^2, and P/V of 10.5. The HEMTs have L_g of 0.1 μm, V_{th} of -0.35 V, and g_m of 950 mS/mm. Proper operation was confirmed up to 15 GHz for the fabricated circuit (Fig. 7). This means that the operating principle of the proposed circuit is correct.

The obtained toggle frequency of the circuit is not so high compared with that of our previous work (34 GHz, [3]) and the conventional SCFL-type T-FF (40.4 GHz, [11]). This is because the circuit configuration is not optimized due to the absence of level-shift diodes. Moreover, there is a relatively small output swing (120 mV) due to the input/output level mismatch between the source follower circuit and the SCFL inverter in the output buffer. This problem will also be overcome with the integration of level-shift diode with RTDs and HEMTs [11].

4. Summary

We proposed a novel RTD-based circuit for the implementation of RTDs in conventional digital ICs. A simulation and experiment showed that the proposed circuit achieves high-speed operation with a simplified configuration along with the SCFL interface. The presented results show that the proposed circuit technology is a promising way to provide ultrahigh-speed logic circuits.

Higher operating speed and larger output amplitude will be possible by the integration of level-shift diodes with RTDs and HEMTs.

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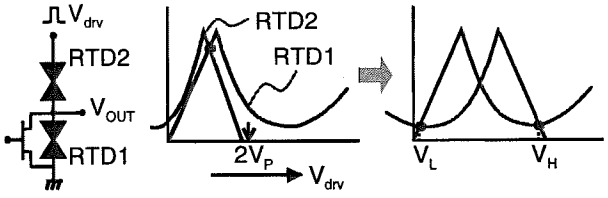

Figure 1. Configuration and operating principle of a MOBILE

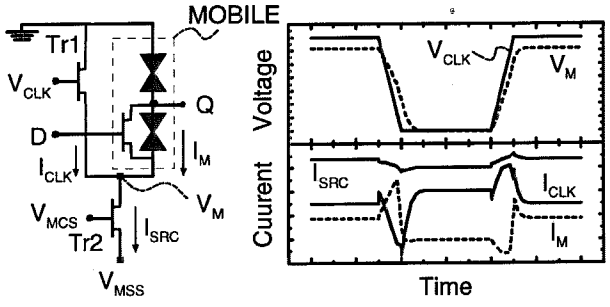

Figure 2. RTD-based flip-flop with SCFL interface

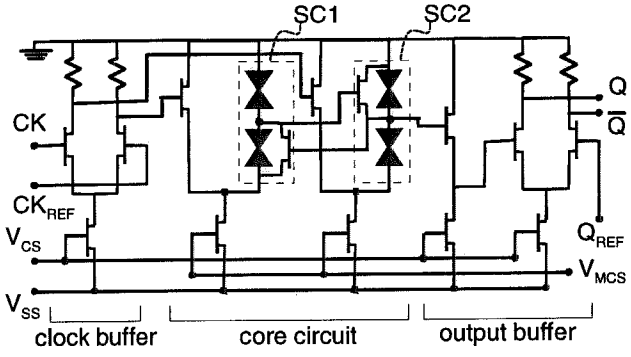

Figure 3. Static binary frequency divider

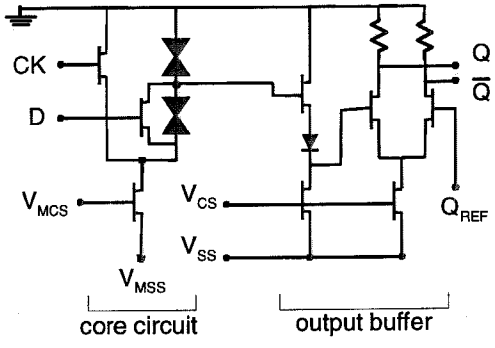

Figure 4. D-FF circuit with RZ output

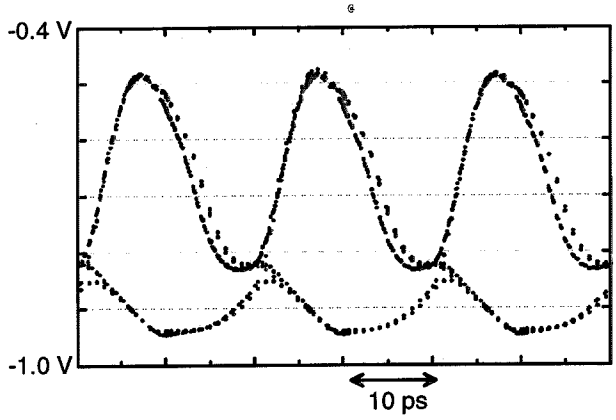

Figure 5. Waveform of D-FF at 50 Gbit/s

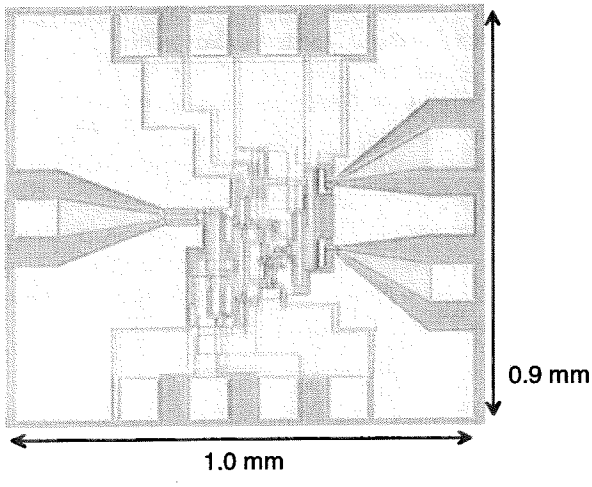

Figure 6. Microphotograph of fabricated T-FF

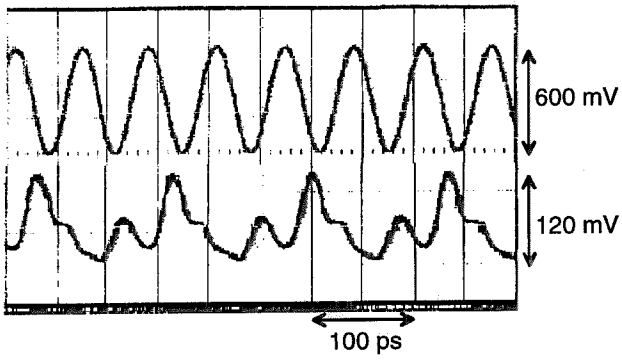

Figure 7. Waveform of T-FF at 15 GHz
upper: clock input, lower: output signal