The Development of Analog SPICE Behavioral Model Based on IBIS Model

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Abstract

This paper presents an approach for building an analog SPICE behavioral model based on the information provided by IBIS model. Such analog SPICE behavioral model can describe both static and dynamic characteristics of I/O buffers. The method to extract dynamic information from IBIS switching waveform VT tables is discussed in detail. Two types of models can be generated depending on the availability of the waveform tables with different load conditions in IBIS data. The influence of waveform table load condition on the validity of the analog SPICE behavioral model is also investigated.

1. Introduction

Due to increasing integration density and high-speed digital circuits, the correct design specially needs simulation support for signal integrity (SI) analysis. Such simulation requires electrical models to describe the IC drivers and receivers [1]. In order to satisfy the need for analyzing SI of high-performance systems with a large amount of nets, IBIS model is evolved [2].

IBIS is an emerging standard for electronic behavioral specifications of digital integrated circuit input/output analog characteristics. IBIS model provides many advantages over previous I/O buffer models. It can protect proprietary information about both the buffer design and the underlying fabrication process, run much faster than any corresponding structural model, and at the same time, no accuracy is sacrificed. Thus, IBIS model has become widely accepted among EDA vendors, semiconductor vendors and system designers, and it is becoming an international standard.

Currently, the SPICE-based EDA simulation tools are not IBIS-supported. As IBIS is becoming one main available model source to model the I/O buffers, and SPICE is a widely used simulation tool to analyze electronic interconnections on chips, boards and system level, it is meaningful to develop an approach to make IBIS information used into SPICE.

This paper presents an approach to build an analog SPICE behavioral model based on IBIS data that can be used by SPICE directly. The analog SPICE behavioral model can describe both the static and dynamic characteristics of I/O buffers. The dynamic information relevant to switching transient behavior is the VT tables available in IBIS version 2.1 format or higher. Not much has been published on exactly how these VT tables can be used to extract the large signal transient model to the best of our knowledge, even though some EDA tools with IBIS support claim to possess such capability. The systematic procedure to solve this problem is discussed in detail. Paper [3] presents one method based on one pair of switching VT tables to extract the transient behavioral model, but an arbitrary assumed assumption limits its validity. In this paper, a more accurate model based on two pairs of switching VT tables is presented.

2. Analog SPICE behavioral model building methodology

2.1. Building principle

IBIS behavioral model presentation of an output buffer is shown in Fig 1. There are five basic elements that must be included for IBIS modeling of an output buffer : pullup transistor, pulldown transistor, power

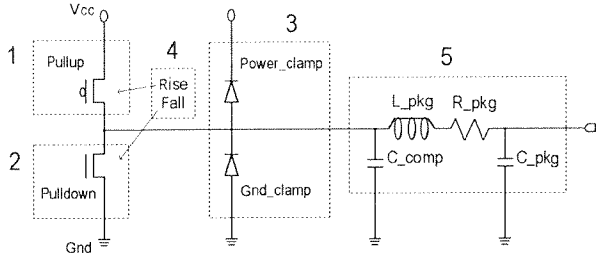

Fig 1. IBIS representation of an output buffer

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clamping diode and ground clamping diode, ramp time and pad and package parasitics. In the static domain, current versus voltage (DC IV) tables are used to characterize each of the output transistors and each of the clamping diodes. Lumped RLC combinations are used to characterize package information. Values for rising and falling ramp time are used to describe dynamic behavior of the output stage. Optionally in the advanced IBIS version, higher precision is achieved by switching waveform VT tables. Voltage versus time (VT) tables represent the transient behavior under the condition of a specific test fixture.

The building of analog SPICE behavioral model needs to find a valid SPICE representation of IBIS model by using SPICE allowed elements. The information of DC IV tables can be represented by voltage controlled current source (VCCS) in SPICE expressed in piecewise linear function. The information of pad and package parasitic can be used by SPICE directly. So all these static characteristics of I/O buffer described by IBIS model can be translated into SPICE without much trouble. Thus, the main problem left is how to generate a large signal model suitable for transient simulation based on IBIS information.

In IBIS specification, the rising and falling waveform VT tables are measured under the load condition without the package parasitic by connecting a resistance R_fix and an external V_fix directly to the output pad of the die

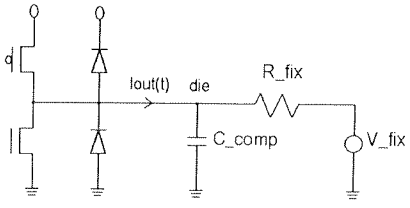


Fig 2. IBIS switching waveform VT tables measurement circuit

as shown in Fig 2. The voltage at the die as a function of time is measured and tabulated as the VT table. Several pairs of these tables may be available in an IBIS model. Typically, the measurement load conditions for switching VT tables are:

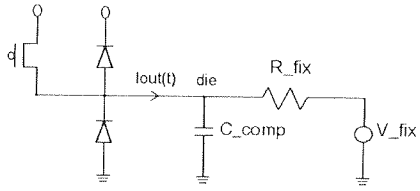
for one pair of switching VT tables

rising edge:	R_fix=50Ω	V_fix= Gnd
falling edge:	R_fix=50Ω	V_fix= Vcc

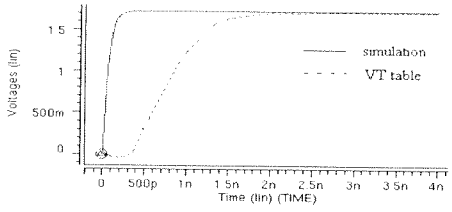
for two pairs of switching VT tables

rising edge:	R_fix=50Ω	V_fix= Gnd
	R_fix=50Ω	V_fix= Vcc
falling edge:	R_fix=50Ω	V_fix= Gnd
	R_fix=50Ω	V_fix= Vcc

It must be cautioned that the IV tables of an IBIS model are purely based on DC condition and should not be used for transient simulation. This can be verified from the simulation results. For example, for the rising case, the circuit topology for simulation is shown in Fig 3(a). According to DC IV tables of pullup device and clamping diodes, and with the load condition that R_fix connected to Gnd (i.e, V_fix=Gnd), the simulated rising edge is shown as solid line in Fig 3(b). Compared with actual rising edge provided by IBIS VT tables shown as dotted line in the same figure, it can be seen that there is a far difference between simulation results and measurement results. The same conclusion we can get for the falling case.



(a) the simulation circuit topology



(b) simulated rising signal

Fig 3. Rising signal simulation only based on DC IV tables

Thus, the approach of deriving switching signal only based on static information, i.e., DC IV tables is not valid. The dynamic information provided by IBIS model must be adopted in the generation of analog SPICE behavioral model. The model building principle is to map all IBIS information of both static and dynamic into the SPICE model.

How to express the dynamic information, i.e., transient information of switching VT tables of IBIS model into analog SPICE behavioral model is the critical problem in the model generation. In our approach, we use multipliers extracted from IBIS VT tables to derive switching signals.

2.2. Circuit topology of analog SPICE behavioral model

In IBIS model, the current flowing through pullup transistor is determined by the voltage across it referenced to Vcc, i.e., Ipu(Vout,Vcc), while the current flowing through pulldown transistor is determined by the voltage across it referenced to Gnd, i.e. Ipd(Vout,Gnd). Vout is the voltage at 'die' point. The same current determination is for clamping diodes.

As we know, it is the pullup and pulldown transistors status change that leads to the switching output signal. Thus, it is natural to introduce two time dependent multipliers *Ku(t)* and *Kd(t)* to describe switching behavior of pullup and pulldown transistors respectively. The value range of *Kx(t)* is between '0' and '1', where '0' corresponding to transistor turn-off state and '1' corresponding to turn-on state. The change of multiplier *Kx(t)* from '0' to '1' represents the transistor status change from turn-off to turn-on. The product of *Ku(t)* and *Ipu(V)* is used to describe the pullup transistor switching behavior while the product of *Kd(t)* and *Ipd(V)* to describe the pulldown transistor switching behavior. Thus, for rising edge, *Ku(t)* changes from '0' to '1' while *Kd(t)* changes from '1' to '0', and vice versa for the falling edge. Hence, the circuit topology of analog SPICE behavioral model is derived as shown in Fig 4. The pullup characteristic Ipu(V) and the pulldown characteristic Ipd(V) are combined with the time dependent multipliers Ku(t) and Kd(t) to describe the switching behavior between High and Low level of the buffer output signal. The current source Ipc(V) represents the Vcc-claming effect whereas the current source Igc(V) models the Gnd-clamping effect of the output buffer. The model configuration is IBIS-conform.

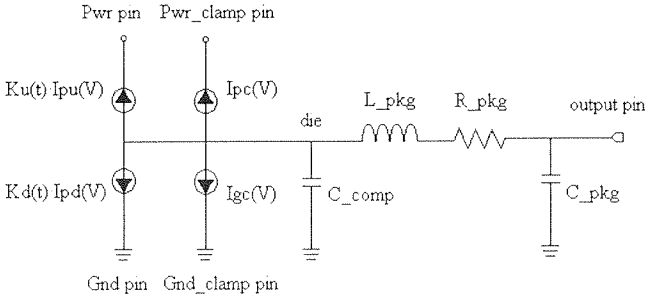


Fig 4. Analog SPICE behavioral model

2.3. Transient representation extraction

The value of multipliers *Kx(t)* can be extracted from switching waveform VT tables in IBIS data. Let us first consider the rising case. In the circuit of Fig 2 with the reference direction of current flowing shown in Fig 4, the following formula exists.

$$-Iout(t) = Ku(t)\cdot Ipu(V) + Kd(t)\cdot Ipd(V) + Ipc(V) + Igc(V) \quad (1)$$

where V is the voltage *Vout(t)* at the 'die' point. At each time point in the rising waveform, there is a corresponding voltage value *Vout(t)* according to VT table. Thus, the corresponding value of *Ipu(V)*, *Ipd(V)*, *Ipc(V)* and *Igc(V)* at that time point can be determined according to IV tables by using piecewise linear interpolation, and also the corresponding *Iout(t)* at that time point can be calculated by SPICE run according to the right portion of circuit shown in Fig 2. Thus, at any time point in the transition process, only two variables *Kur(t)* and *Kdr(t)* are unknown variables.

For the case that only one pair of switching VT tables is provided, in order to solve two multipliers, a relationship between *Kur(t)* and *Kdr(t)* must be assumed. At the beginning time point and the end time point of the transition process, the following relation exists

$$Kur(t) + Kdr(t) = 1 \quad (2)$$

Assume to extend such relation to every time point in the transition process, multipliers *Kur(t)* and *Kdr(t)* can be calculated as following based on the one rising waveform VT table by a SPICE run.

$$Ku(t)\big|_r = Kur(t) = \frac{Iout(t) + Ipc(V) + Igc(V) + Ipd(V)}{Ipd(V) - Ipu(V)} \quad (3.a)$$

$$Kd(t)\big|_r = Kdr(t) = 1 - Kur(t) \quad (3.b)$$

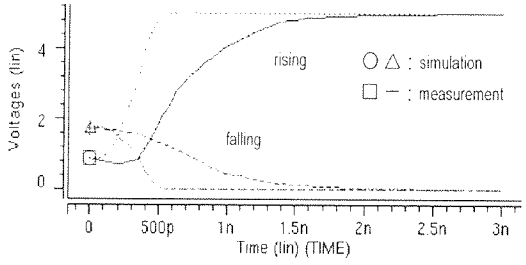
In the same way, the multipliers *Kuf(t)* and *Kdf(t)* for falling case can be calculated according to the falling waveform VT table. However, in the practical reality, the pullup and pulldown transistors do not necessarily start and end the switching process simultaneously. Thus, at any time point during transition process, formula (2) does not exist. So SPICE model only based on one pair of VT tables is not very reasonable.

If two pairs of switching VT tables with different measurement conditions per edge are available in IBIS model, the independent multipliers *Ku(t)* and *Kd(t)* can be derived. Thus, a more accurate SPICE model can be set up.

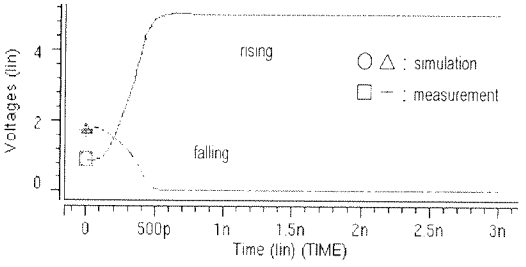
3. Comparison of simulation results of analog SPICE behavioral model

Using the above method, based on IBIS data provided from measurement by Cypress Semiconductor Corporation, some meaningful comparison can be performed.

Based on one pair of switching waveform VT tables, two dependent multipliers can be calculated and a SPICE model can be set up with the topology shown in Fig 4. Using this model to do transient simulation under the load condition of V_fix=Vcc(5.0v) for rising edge and V_fix=Gnd for falling edge, the simulation results shown in Fig 5(a) are quite different from the measurements. The reason is that both in the rising and falling cases, the load conditions for simulation are different from the load conditions used to generate the SPICE model. Hence, the validity of SPICE model based on one pair of switching VT tables is limited to the load condition used in measuring switching waveform VT table which is the basis for the SPICE model generation. Based on two pairs of switching waveform VT tables, a SPICE model



(a) Based on one pair of switching VT tables



(b) Based on two pairs of switching VT tables

Fig 5. Simulation results of SPICE model

with two independent multipliers can be set up. Using this model to do transient simulation, the simulation results fit excellently with the measurements as shown in Fig 5(b). Thus, the SPICE model based on two pairs of VT tables overcomes the strong load dependence of the SPICE model based on one pair of VT tables. SPICE model generated based on two pairs of switching waveform VT tables is more valid.

4. Conclusion

An analog SPICE behavioral model based on the information provided by IBIS model is built up. It can effectively be used to integrate with the simulator SPICE to analyze high-speed switching chip interconnects. Because of its behavioral nature as IBIS model, the simulation speed is increased greatly.

In such analog SPICE behavioral model, the elements of voltage controlled current source (VCCS) are used to describe the static characteristic of I/O buffers. Extracted time dependent multipliers are used to describe the dynamic characteristic of I/O buffers. Based on two pairs of switching VT tables with two different load conditions for each rising and falling edge, independent pullup and pulldown multipliers *Ku(t)* and *Kd(t)* can be extracted which results that the validity of such behavioral model covers a wide range of load conditions.

References

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