Substrate Modeling and Lumped Substrate Resistance Extraction for CMOS ESD/Latchup Circuit Simulation *

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ABSTRACT

Due to interactions through the common silicon substrate, the layout and placement of devices and substrate contacts can have significant impacts on a circuit's ESD (Electrostatic Discharge) and latchup behavior in CMOS technologies. Proper substrate modeling is thus required for circuit-level simulation to predict the circuit's ESD performance and latchup immunity. In this work we propose a new substrate resistance network model, and develop a novel substrate resistance extraction method that accurately calculates the distribution of injection current into the substrate during ESD or latchup events. With the proposed substrate model and resistance extraction, we can capture the three-dimensional layout parasitics in the circuit as well as the vertical substrate doping profile, and simulate these effects on circuit behavior at the circuit-level accurately. The usefulness of this work for layout optimization is demonstrated with an industrial circuit example.

1. Introduction

Decreasing feature size and rising packing densities have resulted in more prominent substrate coupling effects in modern CMOS circuits, invalidating the heuristics that designers have relied on in the past for optimizing I/O and internal circuitry or their layouts to guarantee ESD or latchup reliability [27][6][26][10][23]. Simulation thus becomes increasingly important. To successfully predict the reliability of a design using circuit-level simulation, three elements must be modeled accurately, namely device, interconnect and substrate. This paper addresses the substrate modeling issue for CMOS ESD/latchup reliability, and the results can be extended to areas such as mixed-signal circuit modeling.

Recently, there has been great interest in substrate modeling for CMOS VLSI circuits, especially in mixed-signal [21][25][8] and ESD/latchup reliability [24][2][11][15] applications. In general, research efforts have been in two directions, i.e. full chip substrate modeling and compact device modeling. Full chip substrate modeling is primarily for mixed-signal applications, with the focus on efficient extraction and reduction of the substrate impedance/admittance network model [25][20][14]. Compact device modeling (high-current device and latchup models with substrate terminals) [24][2][11] aims at building accurate circuit-level models for devices and "local" substrate. Here the extraction of model parameters and substrate resistance has been commonly done from measurements or device-level simulations using simulators such as MEDICI [22].

The contributions of this work are twofold. First, this new model bridges the gap between high-current device models and full-chip substrate model, so transient circuit simulation can be performed with simultaneous consideration of devices, substrate and interconnect systems. Second, we developed a novel substrate resistance extractor that can accurately determine the device current injection distributions into silicon substrate. Its accurate estimation is key to lumped resistance extraction simply because such current distributions strongly affect the local substrate potential, which in turn can change the device's operation regime. This work can be integrated into an ESD/latchup layout extraction and optimization framework for complete I/O circuits analysis [4][17].

The rest of this paper is organized as follows. In section 2, we briefly review the high-current device model for the MOS transistor, and point out the importance of accurate substrate modeling. In section 3, we present the new substrate resistance network model. In section 4, the extractor iSREX (**I**llinois **S**ubstrate **R**esistance **EX**tractor) is explained in detail. Then we demonstrate the usefulness of the substrate resistance model through a layout optimization example in section 5, and conclude in section 6.

2. High-Current Device Models

The regions of the I-V curve of a typical NMOS device are depicted schematically in Fig. 1. Regions 1 and 2 are the

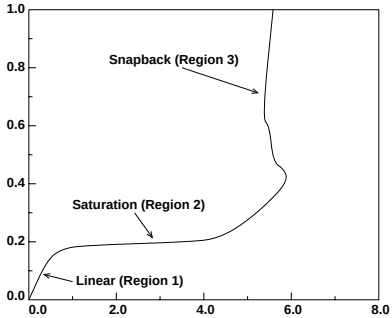

Figure 1. Generic I-V curve for an NMOS transistor under gate bias showing the different regions of operation. Standard SPICE models do not cover region 3.

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linear and saturation regions governed by standard MOS equations. Region 3 is the bipolar or *snapback* region. The NMOS transistor operates in the linear and saturation regions under normal conditions. However, it goes into high current regions, namely avalanche breakdown and snapback, during ESD and latchup events. The avalanche generation of carriers in the high-field region near the drain results in the hole current I_{sub} being injected into the substrate. I_{sub} increases the voltage drop across R_{sub} and raises the local substrate potential V_b, and eventually causes the source-substrate junction to become forward-biased. Standard NMOS models such as BSIM3 [12] can be extended to cover the high current regions with the addition of a lateral parasitic NPN transistor as shown in Fig. 2 [2]. Accurate substrate resistance modeling is critical, for it determines the on/off state of a device and its high current behaviors.

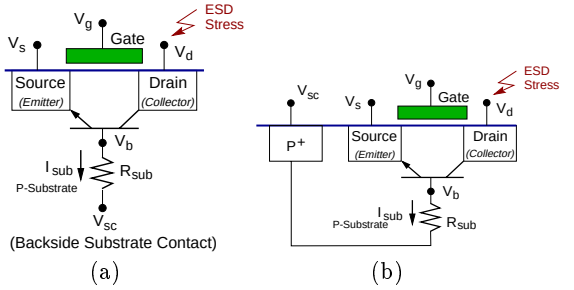

Figure 2. (a) Cross-section of an NMOS transistor showing the currents in the parasitic NPN transistor. (b) Cross-section of an NMOS transistor showing the parasitic NPN transistor and a topside substrate contact.

The single resistor substrate model, shown in Fig. 2(a) and used in previous works [2][11][15], has certain limitations: (1) The substrate may have multiple substrate contacts, each at a different electrical potential due to the voltage drop on the ground bus between them. Depending on its relative location to the substrate contact, each device in the layout can experience a different substrate resistance. The single resistor model fails to capture these effects. (2) It can not model the device interactions through the silicon substrate. Such interactions can significantly affect the circuit's ESD behavior by either enhancing ESD performance [1][18][3], or causing unexpected failure [13][5][9].

3. Substrate Resistance Network Model

We first present the substrate model for a simple circuit with one device, one external substrate injection current and one substrate contact. Then we extend the model to more complicated circuits.

3.1. Modeling External Current Injection

Recall that when an NMOSFET is subject to a positive ESD stress at its drain, the parasitic BJT may turn on due to increased local substrate potential, causing the NMOS to operate in the snapback regime. The trigger or breakdown (drain) voltage at which the transistor enters the snapback regime is affected by V_{sc} (see Fig. 2). Fig. 3. shows the simulated I-V curve for an NMOS transistor with V_g at ground. We can observe that the trigger voltage decreases as the external substrate bias voltage increases. Therefore, inaccurate modeling of local substrate potential may result in incorrect simulated operation condition (on/off state) of an NMOS transistor.

CMOS devices residing in the common silicon substrate are under the influence of substrate currents produced by

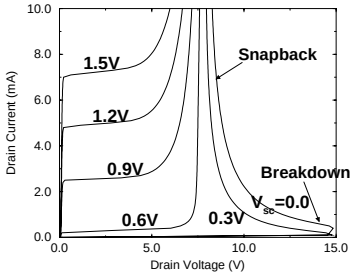

Figure 3. The simulated I-V characteristics of an NMOS transistor for various substrate bias voltages with V_g at ground.

nearby devices ("external" substrate currents). Such currents can affect a device's local substrate potential, and can be modeled by using the concept of *transfer resistance* [23][24], defined as the surface potential at a point away from the injector divided by the injection current. The

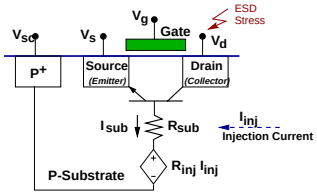

Figure 4. The substrate resistance model of an NMOS transistor under the influence of one external current source.

substrate resistance model for an NMOS transistor with the presence of an "external" current I_{inj} is shown in Fig. 4. R_{inj} is the transfer resistance associated with I_{inj}, and can be represented by a current-controlled voltage source. By definition, R_{inj} can be obtained by dividing the local substrate potential near the emitter junction by I_{inj} when I_{sub} is set to 0. Similarly, R_{sub} can be obtained by setting I_{inj} to 0. Note that one transfer resistance is associated with three elements, namely an injection current source, a substrate contact and a voltage monitoring point.

3.2. Modeling Multiple Devices

Fig. 5 shows an example of a circuit containing multiple substrate current injection sources. The circuit consists of two grounded gate NMOS transistors connected in parallel and a lateral diode to V_{dd}. The lateral diode is more generally modeled as a vertical BJT. The substrate contact is a ring structure surrounding the cell layout.

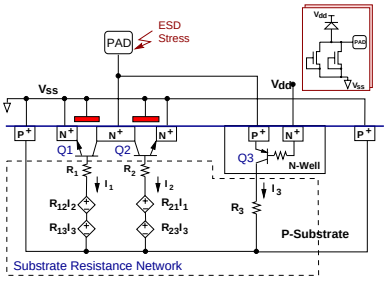

Figure 5. The substrate resistance model with multiple substrate current sources.

Under positive stress from the pad to V_{ss}, there exist three substrate current sources: the impact ionization currents from the collector-base junctions of Q1 and Q2 and the collector current of Q3. Each device's local substrate

potential is affected by all devices. These interactions are modeled by the substrate resistance network shown in Fig. 5 inside the dashed lines. The network includes one transfer resistance for every pair of current source and monitoring location: in the case of Fig. 5, where there are three current sources I_1, I_2 and I_3 and three monitoring locations Q_1, Q_2 and Q_3, the network contains $3 \times 3 = 9$ resistances.

Although the number of transfer resistances increases quadratically with the number of devices, the network can often be simplified in the following cases:

1. The effect of external injection currents on the collector voltage of a vertical BJT can be neglected, since the collector current is, to the first order, controlled by the base current and independent of the collector voltage. As a result, the transfer resistances R_{31} and R_{32} are not included in Fig. 5.
2. Devices of the same kind connected in parallel can be clustered if they are identical, e.g. Q1 and Q2 can be reduced to a single transistor if $I_1 \approx I_2$, $R_1 \approx R_2, R_{12} \approx R_{21}$ and $R_{13} \approx R_{23}$.
3. If a transfer resistance is sufficiently small, the associated voltage source may be omitted (shorted) without affecting the simulation accuracy.

3.3. Modeling Multiple Substrate Contacts

When an I/O circuit layout contains multiple substrate contacts, they may be at different potentials due to the ground bus routing. As a result, these contacts need to be modeled as separate nodes in the circuit model: for each pair of current source / monitoring location, the network should now include one transfer resistance for *every substrate contact*. In Fig. 6, because there are two current sources (I_{inj} and

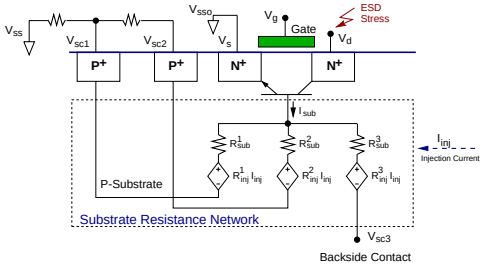

Figure 6. The substrate resistance model with multiple substrate contacts.

I_{sub}), one monitoring location and three substrate contacts (V_{sc1}, V_{sc2} and V_{sc3}), the network contains $2 \times 1 \times 3 = 6$ resistances.

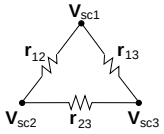

Figure 7. The resistive network modeling the relationships between substrate contacts.

The substrate connection among separate contacts can be represented by a fully connected network of resistors as shown in Fig. 7, where r_{ij} is the resistance between contact node i and j. Note that r_{ij} is an ordinary two-terminal resistor, not a transfer resistance. This model is the same as the multiport impedance/admittance network between substrate contacts commonly extracted for mixed-signal circuits [25], and should be combined with the network in Fig. 6 to complete the substrate model. Again this resistive network can often be simplified: when the resistance of one branch is significantly larger than another branch, it can be approximated as an open circuit and removed.

4. Substrate Resistance Extraction

Recall that for a circuit with m injection current sources, n substrate contacts and p monitoring locations, $m \times n \times p$ transfer resistances must be calculated using the formula

$$R_{ji}^k = V_{ji}^k / I_i \tag{1}$$

for each i, j and k ($i = 1, \cdots, m$, $j = 1, \cdots, p$ and $k = 1, \cdots, n$), where I_i is the injection current, and V_{ji}^k is the voltage at the monitoring location j due to current source i with reference to substrate contact k.

The flow diagram of our substrate resistance extractor iSREX is shown in Fig. 8. For each source and substrate contact pair, the extraction procedure involves two steps: First, the current distribution on the surface of the injection source is determined. Next, the transfer resistances associated with this source and substrate contact pair are extracted for *all* the monitoring locations. In this section we will discuss the details of these two steps, and the extraction of the network among substrate contacts (Fig. 7).

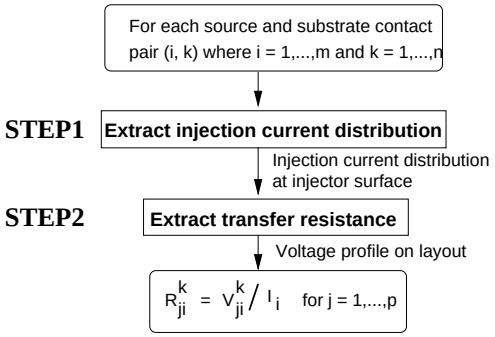

Figure 8. The iSREX transfer resistance extraction flow.

iSREX employs the 3D finite difference (FD) method to extract the substrate resistances. Given a layout structure, e.g. the circuit in Fig. 5, we partition the substrate body in the x, y and z directions, forming a network of grids as shown in Fig. 9. The resistances for the grids inside diffu-

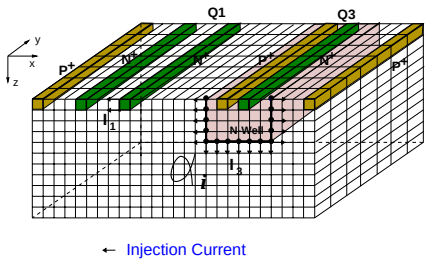

Figure 9. Network of grids for the circuit in Fig. 5 (Q_2 is not shown here, and the substrate contact is a ring structure surrounding the layout).

sions or wells are set to infinity (open circuit), and the resistance for other grids are determined by the doping profile of the substrate and the grid spacings. Then for any injection current distribution, we can just employ nodal analysis to solve for the potential distribution in the substrate.

4.1. Step 2 – Transfer Resistance Extraction

We first explain Step 2 in Fig. 8. For a specific current source and substrate contact pair, we inject the current from the source according to the surface current distribution obtained from Step 1 (e.g. α_i in Fig. 9). For a vertical BJT such as a PNP structure, the current is injected from the n-well to substrate. For an NMOS transistor, the impact ionization current is injected from the side-wall of the drain. The referenced substrate contact is set to ground, while other contacts are set floating. An FD solver is called to calculate the voltage profile across the substrate, and from the potentials at monitoring locations we can calculate the transfer resistances by using Eq. 1.

4.2. Step 1 – Injection Current Distribution Extraction

The injection current distribution along the injector surface is heavily layout dependent. For instance, considering the case of substrate current injection from a p-n diode in an n-well (Fig. 10), we observe that the current will flow along the lowest resistance paths, and the distribution at the injector surface is primarily determined by the relative location of the substrate contact. Since incorrect current distribution will produce erroneous potential simulation results, accurate estimation of the injection current distribution is key for accurate extraction of transfer resistances.

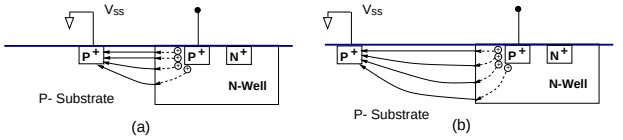

Figure 10. The different current flow due to different substrate contact locations.

In a previous work [24] to develop an analytical 2D transfer resistance model for substrate, the current distribution along the n-well sidewall and bottom was determined by fitting the device simulation results. In iSREX, we use a novel method to determine the injection current distribution based on the fact that the injector (n-well) surface is an equipotential, as follows. We first apply the same grid system shown in Fig. 9. Let the term *source grid points* denote the grid points on the injector surface. Assuming that there are n source grid points, we can determine the distribution of the injection current at these source grid points by solving the following equation:

$$\begin{bmatrix} R_{11} & R_{12} & \cdots & R_{1n} & -1 \\ R_{21} & R_{22} & \cdots & R_{2n} & -1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ R_{n1} & R_{n2} & \cdots & R_{nn} & -1 \\ 1 & 1 & \cdots & 1 & 0 \end{bmatrix} \begin{bmatrix} \alpha_1 I \\ \alpha_2 I \\ \vdots \\ \alpha_n I \\ V \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ I \end{bmatrix} \quad (2)$$

where I is the total injection current, $\alpha_i I$ $(0 \leq \alpha_i \leq 1)$ is the current component at the source grid point i $(i = 1, \cdots, n)$, R_{ij} is the transfer resistance of the source grid point i due to the current injection only at the source grid point j, and V is the common potential at the equipotential injector surface.

R_{ij} can be extracted by applying the FD method repeatedly: for every source grid point j, we inject one unit of current at it, and calculate the resulting substrate potential distribution. The potential value at any source grid point i is then numerically equal to the transfer resistances R_{ij}. Note that for the same 3D grid system, we only need to apply LU decomposition to the admittance matrix of the 3D mesh once; subsequent calculations of potential distributions involve only forward and backward substitution, which is very efficient.

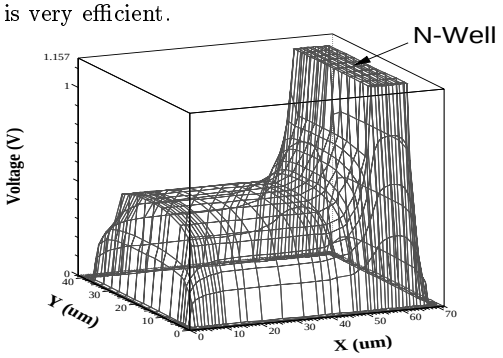

Figure 11. The voltage profile at the silicon surface under 10 mA current injection from BJT Q_3. The layout contains 8 NMOS transistors (Fig. 12). Given a monitoring location such as Q_1, the transfer resistance is calculated as the highest voltage around the emitter junction divided by the total injection current. The run time is 269 seconds on a ULTRA1 SUN workstation, including the time to obtain the injection current distribution.

Fig. 11 shows the simulated substrate potential profile under 10 mA current injection for the circuit in Fig. 5. The potentials at all grid points on the n-well surface are exactly the same, reflecting the correctness of our current distribution calculation.

4.3. Two-Terminal Resistor Extraction

Extracting the network shown in Fig. 7 is straightforward. For each substrate contact pair, we inject one unit of current into one terminal and ground the other, while keeping all other contacts floating. We then apply the FD method to calculate the input terminal voltage, which is numerically equal to the resistance connecting the two substrate contacts under consideration. Note that we can also use other techniques such as the Green's function method [8][20] to extract the network resistance values.

It is important to note that iSREX is significantly different from device-level simulators such as MEDICI. iSREX is more efficient because we are solving 3D resistive networks instead of the complete set of transport equations. However, accuracy is not sacrificed because a novel method is used to determine the injected current distribution. Adaptive griding and superposition principle can also be applied to further improve the efficiency of iSREX. In addition, iSREX can capture the 3D effects of circuit layout and process technology, while many device simulators can only perform 2D simulation for large layout structures within a reasonable time.

4.4. iSREX Run-Time Complexity Analysis

The iSREX run-time is largely determined by the number of nodes in the 3D mesh. The complexity of a matrix solver using the standard Gaussian elimination is $O(n^3)$, where n is the number of grid points. If we use the same mesh for computing both the transfer resistances and the two-terminal resistors, then only one matrix decomposition is needed for the entire iSREX extraction process. Iterative matrix solving methods such as GMRES [19] can also be used to further reduce the computation time.

The computation time of current injection distribution is much shorter than calculating the transfer resistances, because the number of source grid points is much smaller than the total number of grid points in the substrate. We

observe that the run-time for the extraction of injection current distribution usually costs only 20% of the total iSREX extraction time.

5. A Design Example

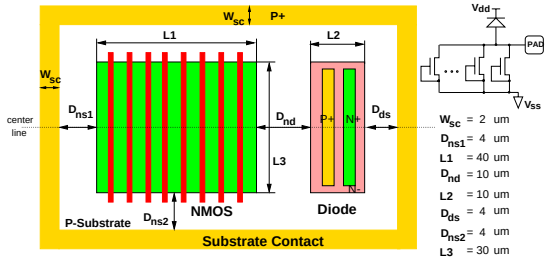

Figure 12. The layout of the protection circuit. The critical dimensions are labeled as D_{nd} (NMOS to diode spacing), D_{ns1} and D_{ns2} (NMOS to substrate contact spacings), D_{ds} (diode to substrate contact spacing), and W_{sc} (substrate contact width) and default values are listed. The default technology parameters are $0.2\mu m$ diffusion junction depths T_{act}, $2\mu m$ well depths T_{well}, $6\mu m$ epi thickness T_{epi}, $10^{16}\ cm^{-3}$ doping concentration for the epitaxial layer and $10^{19}\ cm^{-3}$ for the p+ substrate.

In this section we demonstrate the usefulness of our substrate resistance network model by studying an industrial example [1][18][3]. One possible layout of this design is shown in Fig. 12 (its cross-section is similar to the circuit shown in Fig. 5), along with its critical dimensions and technology parameters. Please note that this layout has been simplified for demonstration purpose; other details such as minority guardrings are not shown.

The circuit consists of a lateral diode to V_{dd} bus and a multifinger NMOS transistor. Assuming the NMOS drain is stressed with positive ESD current with respect to V_{ss}, the lateral diode is extracted as a vertical BJT. Furthermore, if all the NMOS transistors are clustered into a single one, we can extract the circuit schematic under user-specified stress condition by using the layout extractor [16], and obtain simulation results, both shown in Fig. 13.

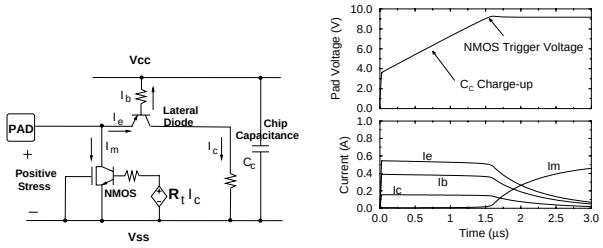

Figure 13. Circuit schematic and simulation results for an I/O protection circuit under positive stress. (R_t is the transfer resistance from the lateral diode to the NMOS transistors)

To ensure ESD/latchup reliability, the critical dimensions of the layout must be optimized such that (1) the BJT collector current can raise the substrate potential high enough under positive ESD stress to trigger the NMOS, (2) the local substrate potential for each NMOS transistor finger should be roughly equal so that they behave uniformly, and (3) the circuit must pass the latchup immunity requirement (it is often in conflict with ESD performance). Here we try to optimize the layout by studying the effects of several parameters, including epitaxial layer thickness T_{epi}, D_{ns1}, D_{nd} and D_{ns}, through circuit-level simulations.

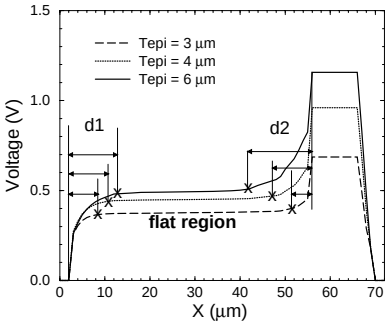

Figure 14. The surface voltage profiles along the center line (see layout in Fig. 12) under 10 mA current injection from the vertical BJT (lateral diode) for various epitaxial layer thickness T_{epi}.

Fig. 14 shows the voltage profiles along the center line of the layout due to the same vertical BJT current with different T_{epi}. There exist three regions in the plot, namely region d_1, a flat region and region d_2. Notice that d_1 and d_2 increase as T_{epi} increases. It is important that all the NMOS transistors reside in the flat region so that they can conduct uniform currents. Therefore, $D_{ns1} > d1$ and $D_{nd} > d2$ should be followed as a design rule.

D_{ds} is another important design parameter. We extract the transfer resistance in the flat region as a function of D_{ds} for various T_{epi} (Fig. 15). Note that all NMOS transistor fingers see the same diode-to-NMOS transfer resistance R_t if the design rule in the previous paragraph is followed. R_t should be large enough to raise the substrate potential and trigger the NMOS transistor during ESD events. We see that when D_{ds} is small, the transfer resistance R_t is greatly reduced. This indicates that a large proportion of the BJT current flows laterally into the substrate contact on the right. When D_{ds} increases, this lateral current component decreases, and more current contributes to the transfer resistance in the flat region. The figure indicates that D_{ds} should be at least T_{epi} away from the diode.

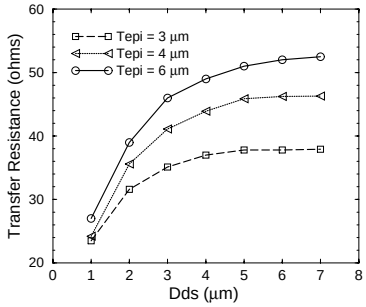

Figure 15. The transfer resistance in the flat region (vertical BJT to NMOS transistors) as a function of D_{s1} for various T_{epi}.

To study the latchup immunity of the circuit, the entire I/O layout, including PMOS drive transistor, must be extracted. Other layout parameters such as the width of substrate contact W_{sc} must be carefully designed, so that the sources of NMOS transistors will not be forwarded-biased when the current is injected from PMOS transistors. At the same time, the transfer resistance R_t should be sufficiently large to allow the triggering of NMOS transistors under ESD conditions. These issues are not discussed here in detail due to the length limit of the paper.

Although the layout example is shown in the epitaxial substrate, the substrate resistance extraction method is general and can be applied to bulk silicon processes, too.

6. Summary

In conclusion, we have proposed a new substrate resistance network model and a novel substrate resistance extraction method for circuit-level simulation of CMOS VLSI circuits under ESD/latchup conditions. The substrate model is linked with a layout extractor to automatically detect parasitic devices and generate simulation input decks. The new substrate model for ESD/latchup reliability is more general than the classical latchup model [23]. With the iSREX 3D exact extraction method, for the first time, the lumped substrate resistance can be determined accurately and efficiently. Further, accurate full chip ESD/latchup analysis will become possible when the substrate model is combined with accurate interconnect models.

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