Panel: Parasitic extraction accuracy; How much is enough?

Chair: Paul Franzon - North Carolina State University, Raleigh, NC
Organizer: Mark S. Basel - Cadence Design Systems, Cary, NC

The effect of parasitic elements on chip performance is well known, however the relative importance of this effect is becoming more critical to a chip's performance. To cope with this new design hazard there are a number of parasitic extraction tools and methodology approaches available to the circuit designer. Some developed for the general market and some developed for internal use. With each product having its own claims and approaches, deciding on a tool or extraction strategy is a confusing exercise. The purpose of this panel is to help the designer and CAD manager determine how to properly compare extractors and how to put them to use. The panel will address a number of questions including; What is the best way to accurately handle parasitic extraction while dealing with increasingly large and complex (SOC, mixed signal) chips? How to determine and achieve the required extraction accuracy for a particular design situation? How is extraction accuracy measured? How can each extractor be compared and contrasted with some degree of confidence? Can circuit design techniques and/or tool methodologies be used to reduce the extraction effort? How should process variations or inductive effects be handled? What's the best way to deal with the data volume problem?

Mark Basel, Cadence Design Systems, Cary, NC
There has been much emphasis recently by designers and the trade publications on parasitic extraction accuracy. While important, accuracy is not the only factor to consider when it comes to extraction. There must be an awareness of the context in which it is used. In timing analysis, for example, coupling capacitors are typically lumped to ground and multiplied by a Miller effect factor. The accuracy of the coupling capacitance extraction is less important in this case unless the true behavior of the signal lines is known and the multiplier is used selectively, e.g. only if lines are switching differentially. Other factors that should be considered when developing an extraction strategy include: the ability to extract a partial or LVS unclean layout, speed and ease of integration into the design flow. Highly accurate extraction is useful in some situations but any design that relies on having highly accurate parasitic values will surely see problems once process variations are taken into account or the design is moved to another fab.

Aki Fujimura, Simplex Solutions, Sunnyvale, CA
Transistor-level and gate-level designers put different priority on extraction capabilities: transistor-level designers put accuracy first - but must have full chip speed and capacity; gate-level designers put speed and ease of use first - but must have bounded +/-10% accuracy. But in all sub 0.25 micron designs, accurate, full-chip, distributed, and coupled RC extraction is critical not only for delay, but also for signal noise, clock skew, IR Drop, and electromigration analysis.

Sharad Mehrotra, IBM, Austin, Texas
Proper analysis of high frequency effects is crucially important for custom microprocessor design. This makes full-chip RLC extraction a requirement for GHz designs. Parasitic extraction needs to be accurate enough for the correct identification of timing critical paths and possible signal integrity violations. However, parasitic extraction is not just a tool for the final stages of design. It is very important to identify design problems early and consistently throughout the design cycle. Usually, the parasitic extraction accuracy question translates to determining how a device model or RLC netlist extracted from a particular design geometry compares to the netlist computed by a more accurate benchmarking tool, e.g. a field-solver. However, this question has several confounding factors: the correlation of timing/signal integrity analysis tools to exact circuit simulation, the correlation of design geometries to manufactured ones, and the quality of the design data itself. The last factor needs special emphasis. Custom designs usually evolve over a long period of time. For the most part, the traditional measure of accuracy of the extraction netlist is a moot point till very late in the design cycle. What is perhaps more important is efficient turnaround in correctly capturing the most significant design problems to allow a designer to converge on a functional design as close to the design limits as possible.

Ron Preston, Alpha Development Group -- Compaq Computer Corporation, Shrewsbury, MA
Interconnect delays are playing an increasingly significant role with each new microprocessor generation. This trend would imply that the accuracy of interconnect parasitic extraction should be a priority for future designs. However, highly accurate extractions of resistance and capacitance that ignore other effects such as inductance, on-die line variation, interconnect aging, and the distributive effects of the extracted lumped components will not be sufficient to produce GHz+ class designs. Run times for parasitic extraction must be reasonable to ensure the designers are not operating on stale layout data. Since a large CPU design may have more than 100 designers making changes, data becomes stale very quickly. Ideally, full parasitic extraction of 100M+ device chips should be possible on a daily basis. In addition, the ERC and timing verification tools that use the parasitic data must have suitable analysis techniques and data capacity to fully utilize the available extraction accuracy. Extraction tools that include all major effects such as on-die variation and inductance while generating consistent and repeatable results with reasonable run times will be more useful that those that focus on high accuracy alone.

Robin C Sarma, Texas Instruments Inc., Dallas, TX
Parasitics need to be extracted with sufficient accuracy to enable a design team to, at least, find and fix hold-time violations and glitches confidently. The sensitivity of parasitics to process variations also needs to be understood well enough to avoid yield loss. To get a reference for accuracy, we have to develop test structures that lend themselves to accurate measurement and represent real route topologies on today's designs. Given the trends toward finer interconnect pitches, faster clock rates and lower threshold voltages, the margin for error is small. Design teams will require accuracy close to that of 3D solvers, managing the run time through hierarchy and by partitioning the task over a large network. In particular, 3D extraction accuracy is needed for the clock tree and the devices in critical cells, such as an SRAM bit cell.

Marty Walker, Frequency Technology, San Jose, CA
With the advent of deep submicron processes, it is common knowledge that the performance of the interconnect dominates chip performance. Thus it is clear that in order to answer the fundamental design question, "Does the design meet spec?", designers need accurate information on the performance of the interconnect. However, it is also clear that designers need to be able to make accuracy trade-offs during the design process. First, they need to quantify accuracy (or more precisely, uncertainty) Then they need to understand the interaction between accuracy and performance, accuracy and chip area, accuracy and design time, etc. Finally they would be able to make the appropriate accuracy tradeoffs.