AN SA-BASED NONLINEAR FUNCTION SYNTHESIZER FOR LINEAR ANALOG INTEGRATED CIRCUITS

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Abstract

Nonlinear functions can be approximated by the linear combination of base functions, which provides a road towards the analog synthesis. An improved Simulated Annealing Algorithm(SA) for nonlinear function approximation and a universal implementation of analog circuits are presented in this paper. Synthesis results demonstrate the validity and efficiency of the proposed approach.

1. INTRODUCTION

By the end of 1990s, most new application-specific integrated circuit (ASIC) designs are incorporated both digital and analog functionality. Most critical applications for such ASIC consumer products, such as network control, mobile communications, conversion, speech recognition, etc. rely on a core of analog circuitry. However, the continuing lack of mature analog EDA tools is a bottleneck in the design process, which hinders the pace of mixed-signal ASICs. Although design automation for analog integrated circuits has gained momentum in recent years[1-5], more attention should be paid to this subject in the near future. There are some embryonic systems for analog synthesis, which can be classified into ad hoc rulebased[1,2], compiler-based[3], and symbolic[4,5] But they are for traditional two-stage operational amplifiers, and can not deal with general analog circuits, especially multi-terminal analog circuits. It is well known that the behavioral model of a multi-terminal analog circuit can be written in terms of the following state space equations[6],

$$\begin{cases} \mathbf{Y} = f(\mathbf{X}, \mathbf{Q}, \mathbf{\dot{Q}}) \\ \mathbf{\dot{Q}} = g(\mathbf{X}, \mathbf{Q}) \end{cases}$$
 (1)

Where, \mathbf{Q} is the state vector, \mathbf{X} and \mathbf{Y} are input and output vectors. All of them are circuit variables such as node voltages and branch currents. f and g are functions that specify the behavior of the circuit.

Q may be derived from \mathbf{Q} through a set of integrators, thus the description of (1) can be structurally realized from the block diagram shown in Fig.-1, and the critical aspect is the functionality synthesis, the realization of f and g.

E.S. Sinencio et al. employ Operational Transconductance Amplifiers (OTAs) to approximate linear, rational, etc., functions[7]. There are also some analog solutions based on piece wise-linear approximations [8]. Although such approaches have proved quite effective when facing some special problem, they can not be generally applied to some rather complex functions.

In this paper, a universal SA-based approach to nonlinear function approximation and an analog circuit structure are proposed, which can be easily realized by squaring cells [9] and current mirrors.

2. AN IMPROVED SA FOR NONLINEAR FUNCTION APPROXIMATION

Suppose $\{\Psi_i(x)\}_{i=1}^{\infty}$ are linear independent, which are often called base functions, then $\forall f(x), x \in [a,b]$

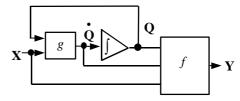


Fig.-1 Structural block realization of Eq.(1)

can be approximated by,

$$f(x) \approx \sum_{i=1}^{N} c_i \Psi_i(x), \quad c_i \in \mathbf{R}$$
 (2)

and coefficients c_i are the solution of the following optimal approximation problem,

$$\min_{\vec{C}} F(\vec{C}) = \max_{x \in [a,b]} \left| f(x) - \sum_{i=1}^{N} c_i \Psi_i(x) \right|$$
 (3)

Where, $\vec{C} = [c_1, c_2, ..., c_N]^T$.

2.1 On Base Functions

The selection of base function set $\{\Psi_i(x)\}_{i=1}^{\infty}$ is the first issue towards the nonlinear function synthesis. The base function set should have three critical properties: a) the function required by $\Psi_i(x)$ can be accurately realized through a small circuit cell, b) $\{\Psi_i(x)\}_{i=1}^{\infty}$ must be suitable for making N in (2) as small as possible, and c) the output of the function generator $\Psi_i(x)$ should be in current mode, because the linear combination of currents can be realized more easily than that of voltages.

Fig.-2 shows a basic squaring circuit and its simplified symbol. The squaring circuit consists of two identical unbalanced emitter-coupled pairs with emitter area ratio S_i cross-coupled inputs and parallel-connected outputs. The differential output current $\Delta I = I_+ - I_-$ can be expressed as [9],

$$\Delta I = \alpha_F I_0 \left\{ \tanh \left(\frac{i \cdot x - VB_i + \beta_i}{2V_T} \right) - \tanh \left(\frac{i \cdot x - VB_i - \beta_i}{2V_T} \right) \right\} \equiv \beta_F I_0 \Psi_i(x)$$
(4)

where, $V_T = kT/q$ is the thermal voltage, α_F the DC

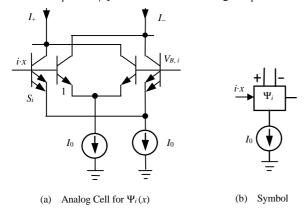


Fig.-2 Analog Cell for Base Function Generation

common-base current gain, I_0 the current sink, and $\beta_i \equiv V_T \ln S_i$.

We select $\Delta I/\alpha_F I_0$ as $\Psi_i(x)$ for three reasons. A) f(x) can be uniformly approximated by (2) in a quite broad range; B) Function generator $\Psi_i(x)$ may be simply realized by BJT[9] or MOS[10] analog cells; and C) S_i can also be treated as design variables besides c_i , which is very helpful to prevent N in (2) from increasing too much for some quite complex function f(x). Base function $\Psi_i(x)$ can also be in other forms, and can be realized by other analog cells. For MOS analog synthesis, the form of $\Psi_i(x)$ is very similar to (4) [10,11]. In order to reduce N for any arbitray nonlinear function f(x), an analog function synthesizer should include as many base function sets as possible.

2.2 An Improved Simulated Annealing Algorithm

Given the base function set, problem (3) can be solved by nonlinear programming method such as NPSOL[12], while better solutions are achieved with SA[13] at the cost of expensive computation time. We prefer SA to NPSOL by virtue of the SA's global convergence. In general, $F(\vec{C})$ is selected as the SA's energy function $E(\vec{C})$. As we just mentioned earlier, SA falls short in spending more computational cost, it is very important to reduce SA's computational cost with no harm to its global convergence.

It is well known that the probabilty of a move with positive energy increment damps exponentially as the annealing procedure cooling down, and \vec{C} , the molecule can not jump out of the valley of the energy function at lower temperatures. In another words, the global convergence of SA is achieved in earlier iterations at hot temperatures. On the other hand, random movements of \vec{C} at lower temperatures waste a lot of time but give little benefit to its global convergence. In fact, employing definite optimization method such as the steepest descendent algorithm will significantly mitigate the computational cost of SA, and does little harm to its global convergence. Our improved SA employ M molecule $\vec{C}^{(m)}$, $m = 1, 2, \dots$ M, to improve the computational efficiency and to garentee the convergency of SA. We treat all these molecule as SA does when the annealing tempeartuer is above the the critical temperature T_C , but start the steepest descendent iteration from "initial point"

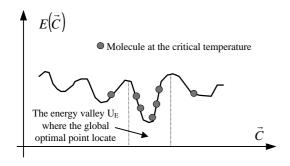


Fig.-3 Sketch Map of Molecule at The critical Temperature

 \vec{C}^I if and only if the annealing temperature is lower than T_C .

Obviously, the selection of \vec{C}^I is the key issue in our algorithm. It is true that as the annealing procedure goes on all the molecule will approximate to the global optimal point. That means if and only if T_C is much smaller than the initial annealing tempeartuer T_0 , most of the M molecule, at the critical temperature, will jump into the energy valley where the global optimal point locats. See Fig.-3 for a sketch map with 7 molecule. The rank of molecule has been introduced in [13] to select the best candidate for \vec{C}^I . Here we take the following simple formulae to set \vec{C}^I ,

$$\vec{C}^I = \frac{1}{M} \sum_{\text{molecule in U}_E} \vec{C}^{(m)}$$
 (5)

As \vec{C}^I is the center of all the M molecule at the critical temperatuer, it must be in the same engergy valley with the global optimal point if and only if the critical temperature is much lower than the initial annealing temperature, and \vec{C}^I is a pretty good guess to the global optimal point, which makes the steepest decendent algorithm moves quikly to the global optimal point.

3. REALIZATION OF FUNCTIONAL SYNTHESIS

Having captured the solution of problem (3) by the improved SA, the linear combination of base functions in (2) can be carried out by the circuit shown in Fig.-4, where $C_i = c_i / \alpha_F$ and the connection rule is,

- if $c_i > 0$, holding the connection of block Ψ_i ;
- if $c_i < 0$, interchanging the two output ports of block Ψ_i :
- if $c_i = 0$, deleting block Ψ_i .

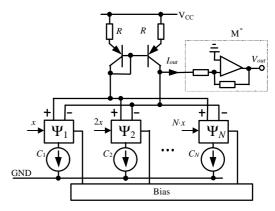


Fig.-4 Circuit Diagram for The Operation Defined in (2)

The output current I_{out} equals to f(x) in quantity. If the circuit designer needs a voltage output, we can use an operational amplifier, indicated by block M^* in Fig.-4, to convert current to voltage. This circuit has high accuracy by virtue of the only need for relative accuracy of resistors and BJTs in current mirrors. For MOS process, the realization of linear combination of base functions is very similar to Fig.-4.

4. EXAMPLES

EXAMPLE-1: Apply our analog function synthesis methodology to a triangle-to-sine wave converter, which is first designed manually by J.W. Fanttaruso and R.G. Meyer [14]. The synthesized circuit consists of 5 fundamental blocks, and its performance is very pleasing. In Fig.-5, the solid curve is the sinusoid computed analytically, while other curves represent the SPICE simulated transfer characteristics of the synthesized triangle-to-sine converter under different temperatures (The load resistance is $2K\Omega$).

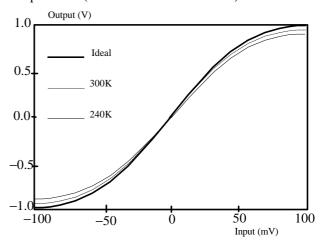
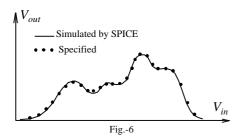


Fig.-5 Simulated transfer characteristic of the synthesized triangle-to-sine wave converter compared with the ideal sinusoid curve.

EXAMPLE-2: Another example is to synthesis a voltage converter with the transfer characteristic shown in Fig.-6. With N=4, the maximum absolute approximation is less than 0.9 percent. To verify the validity of the proposed method, the performance of the synthesized circuit (with $2K\Omega$ resistance load) is analysized by SPICE. To make a clear comparison the simulated result is also drawn in Fig.-6. It is shown that a very fine approximation has been obtained.



5. CONCLUSIONS

In this paper, a functional synthesis methodology of analog circuits is described. Two aspects, the SA-based nonlinear function approximation and its realization by BJT or MOS circuits, are discussed in detail. The improved SA is more efficient than the normal SA. Synthesis examples, verified by SPICE, have proved the validity of the proposed method, too.

The limitation of the base function (4) lies in needing too many fundamental blocks in synthesizing circuits with sharp or steep transfer curves, e.g. comparators. To solve this problem, our analog synthesizer provides several base function sets to meet different necessities.

REFERENCES

- [1] El-Turky F.M., Perry E.E., "BLADES: An Artificial Intelligence Approach to Analog Circuit Design," IEEE Trans. Computer-Aided Design, Vol.8(3), June 1989, pp.680-692.
- [2] Klinke R., Fiedler H.--L., Hosticka B.J., Kokozinshi R., Munster I., "Rule-Based Analog Circuit Design," in Proc. European Design Automation Conf. (EDAC), Sept. 1992, pp.480-484.
- [3] Koh H.Y., Sequin C.H., Gray P.R., "OPASYN: A Compiler for CMOS Operational Amplifiers,"

- IEEE Trans. Computer-Aided Design, Vol.CAD-9(1), Feb. 1990, pp.113-125.
- [4] Gielen G., Walscharts H., Sansen W., "ISAAC: A Symbolic Simulator for Analog Integrated Circuits," IEEE J. Solid-State Circuits, Vol.SC-24(6), Dec. 1989, pp.1587-97.
- [5] Gielen G.G.E., Walscharts H.C.C., Sansen W.M.C., "Analog Circuit Design Optimization Based on Symbolic Simulation and Simulated Annealing," IEEE J. Solid-State Circuits, Vol.SC-25(3), June 1990, pp.707-713.
- [6] Chadha R., Visweswariah C., Chen C.-F., "M³ A multilevel mixed-mode A/D simulator," IEEE Trans. on Computer-Aided Design, Vol.CAD-11(5), May, 1992, pp.575-585.
- [7] Sanches-Sinencio E., Ramirez-Angulo J., Linares-Barranco B., Rodriguez-Vazquez A., "Operational Transconductance Amplifier-Based Nonlinear Function Synthesis," IEEE J. Solid-State Circuits, Vol. SC-24, No.12, Dec. 1989, pp.1576-1586.
- [8] Fattaruso J.W., Meyer R., "MOS Analog Function Synthesis," IEEE J. Solid-State Circuits, Vol. SC-22, No.12. Dec. 1987, pp.1056-1063.
- [9] Kimura K., "A Bipolar Four-Quadrant Analog Quarter-Square Multiplier Consisting of Unbalanced Emitter-Coupled Pairs and Expansions of Its Input Ranges," IEEE J. Solid-State Circuits, Vol. SC-29, No.1, Jan. 1994, pp.46-55.
- [10] Ishizuka O., Tang Z., Matsumoto H., "MOS Sine Function Generator Using Exponential-Law Technique," Electronics Letters, Vol.27(21), Oct. 1991, pp.1937-9
- [11] Liu J.Q., Hwang Y.-S., "CMOS Four-Quadrant Analog Multiplier Using the Bias Offset Cross coupled Pairs," Electron. Lett., Vol. 29, 1993, pp.1737-1738.
- [12] Gill P., et.al., "User's Guide for NPSOL 4.0: a Fortran Package for Nonlinear Programming," Research Report of the Department of Operations Research, Stanford Univ. Jan. 1986.
- [13] Yang H.Z., Fan C.Z., Wang H., Liu R.S., "Simulated Annealing Algorithm with Multi-Molecule: an Approach to Analog Synthesis," ED&TC' 96, Paris, Mar. 1996, pp.571-575.
- [14] Fanttaruso J.W., Meyer R.G., "Triangle-to-Sine Wave Conversion with MOS Technology," IEEE J. Solid-State Circuits, Vol. SC-20, No.2, Apr. 1985, pp.623-631.