I_{DD} Waveforms Analysis for Testing of Domino and Low Voltage Static CMOS Circuits*

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Abstract

This paper describes a test method which relies on the actual observation of supply current (I_{DD}) waveforms. The method can be used to supplement the standard I_{DDQ} test method and it can be easily applied to dynamic and low V_{DD}, low V_T CMOS circuits. The method allows us to detect faults which may not be detected by I_{DDQ} test methods, and is sensitive enough to detect potential faults, which do not manifest themselves as functional errors. A simple built-in current sensor, which proves to be adequate in verifying the feasibility of using the I_{DD} waveforms analysis is proposed to safely observe the current waveforms without significantly changing the waveforms.

1 Introduction

Testing of static CMOS circuits by observing the quiescent power supply current (I_{DDQ}) has been a very popular technique for detecting a large number of physical defects. CMOS ICs showing abnormal I_{DDQ} may contain defects. However, the recent trend in low power design by scaling down the power supply voltage (V_{DD}) and decreasing the threshold voltage (V_T), has caused an increase in the I_{DDQ} current, which reduces the effectiveness of I_{DDQ} testing. Another shortcoming of I_{DDQ} testing is that it cannot be applied to dynamic logic circuits. Hence, to help overcome these shortcomings, we propose a novel test method which relies on the actual observation of the supply current (I_{DD}) waveforms. The method can be used to supplement the I_{DDQ} testing method in trying to detect defects in CMOS circuits. Previous research on I_{DD} waveform analysis shows that it can be used to detect and locate stuck-at-faults [1]. The work is done using Pseudo-NMOS 2-input NAND followed by a CMOS inverter with the s-a-0 and s-a-1 faults being modeled with a bridge of 10kΩ between the NAND output with GND and VDD, respectively. However, they do not consider the Dynamic and FCMOS logic applicability or the weak transistor and resistive open faults which are presented in this paper.

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Defects which cause electrical shorts and opens that cause floating CMOS inputs are detectable by observing the quiescent current (I_{DDQ}). Our objective is not to target such faults which can be detected by I_{DDQ} testing, but to be able to detect weak opens (high resistance shorts) or individual weak transistors. In fact, such faults may not even show any logic functionality error in the circuit, but can cause delay faults, and can affect reliability issues with marginal circuit performance at certain process corners. Such defects show up as a change in the waveforms of the supply current.

The rest of the paper is organized as follows. In section 2, we describe a method to analyze the waveforms of the supply current. In section 3, we verify that the defects which we try to detect indeed cause errors in the waveforms for static CMOS, and precharged Domino circuits. A simple built-in current sensor which shows the feasibility of actually observing the I_{DD} waveforms is evaluated in section 4. In section 5, a complete 8-bit adder circuit is used to verify that the method is applicable to a group of gates. We summarize with a list of key results and directions for future work in section 6.

2 Supply Current (I_{DD}) Waveforms Analysis Method

First, we temporarily neglect the issue of whether it is physically possible to accurately observe the supply current waveforms, without significantly altering the waveforms. We assume that there is a current sensor which is able to safely observe the waveforms. In sec-

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tion 4, we consider the design of a current sensor to observe the supply current waveform. With the above assumption, we can represent our CMOS circuit as the system shown in Figure 1 . V(t) is the input voltage waveform from the previous stage, H(t) is the transfer function of the CMOS circuit, and I(t) is the supply current.

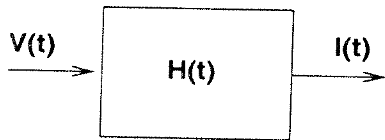

Figure 1: Model of a CMOS circuit.

There are two factors which can alter the supply current waveform I(t):
• A change in the input voltage waveform V(t). This change can happen because of a fault in the previous stage.
• A change in the transfer function of the CMOS circuit H(t). If the entire stage becomes stronger or weaker, H(t) is proportionally scaled by a constant factor.

The current I_{DS} which flows through the drain and source of a group of serially connected, saturated mode PMOS transistors is proportional to

$$K_P(V_{DD} - V_T)^2 \tag{1}$$

where K_P is the *gain factor* of the device, V_{DD} and V_T are the power supply voltage and the threshold voltage, respectively. Hence, we can approximately model the charging or discharging of the output capacitances by a serially-stacked, saturated PMOS or NMOS transistors as

$$C\frac{dV}{dt} = I_{DS} = \alpha K'(V_{DD} - V_T)^2 \tag{2}$$

where C is the capacitance being charged or discharged, α is the proportionality constant, K' the equivalent K_P (or K_N) of the transistor stack, V_{DD} and V_T are the supply voltage and the threshold voltage of the PMOS (or NMOS) devices, respectively. A weak transistor changes K' in the above model. Simulation results from SPICE show that the current waveforms change as K' changes. The actual defects, which are more likely to be shorts or opens, have I/V characteristics that are linear (resistive) or exponential (diode). Hence, the supply current I(t) equation is very different from one mode to another. We model the weak opens as being ohmic.

To compare a faulty circuit with a good circuit, we analyze the Fourier components of the supply current. The relative magnitudes of the Fourier components correspond to the relative supply current waveforms. The relative magnitudes of the Fourier components are expressed as

$$F_r = \frac{F_i - F_1}{F_1} \tag{3}$$

where F_r,F_1,F_i are the normalized Fourier component, the fundamental component, and the ith component, respectively.

The frequency components of the output current I(f), which is equal to H(f)*V(f), are then measured. In actual operation, any error in V(f) or H(f) will cause a change in I(f). The advantage of using the normalized Fourier components in the analysis is to make the method tolerants to process and temperature variations, since the normalized Fourier components depend only on the supply current waveforms.

3 I_{DD} Waveforms Analysis for FCMOS and Pre-charged Domino Circuits

We verify that the I_{DD} waveforms analysis does indeed work for CMOS circuits. For the purpose of verification, the SPICE simulations for circuits were carried out using a 0.6μm, HP CMOS process. Figure 2 shows the simulation model. In our SPICE model, we

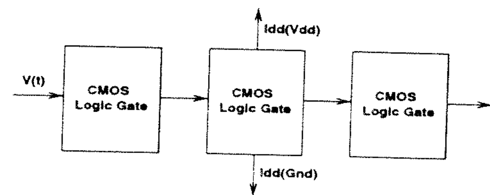

Figure 2: SPICE model.

observe the supply and ground currents of a single isolated gate. Furthermore, in order to provide realistic operating conditions for the gate, we drive the input of the isolated gate with an identical gate and load the output with a similar gate. The loading effects by other gates on the power and ground lines are also included before we simulate the circuit.

3.1 Fully Complementary MOS (FCMOS) Circuits

An inverter and a 2-input NAND gate are used to verify the I_{DD} waveform analysis for FCMOS circuits. The circuit with 2-input NAND gate used in the simulation is shown in Figure 3. In order to detect the weak opens (high resistance shorts) and the weak transistors faults, the following fault effects are simulated for the inverters and NAND gates:

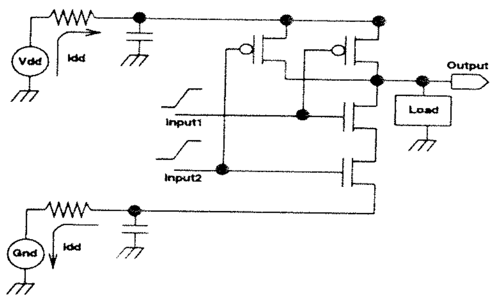

Figure 3: SPICE Model for FCMOS Circuit with 2-input NAND.

• High resistance shorts, modeled by a high resistance at the drains of the transistors.
• Weak transistors, modeled by decreasing the width of the transistors.

We then simulate the circuit and obtain the input-output waveforms, the supply current I_{DD} and the ground current I_{GND} waveforms with their corresponding Fourier components. We use 2-input NAND gates to illustrate the simulations. The waveforms obtained from the simulations with the weak transistor faults are shown in Figure 4, and the waveforms from the simulations with the resistive shorts are shown in Figure 5.

Figure 4 shows the normalized Fourier components of the supply current I_{DD} (top) and the ground current I_{GND} (bottom). The family of waveforms in Figure 4 is obtained by changing the width of the PMOS devices of the NAND gates with a ratio of 0.5, 1.0 and 2.0. Changing the width of the PMOS devices correlates directly to changing the strength of the transistors. The significance difference among the waveforms obtained makes it possible to differentiate the good circuit with the defective circuits. We just need to observe the relative shape of the first three or four components of the waveforms to differentiate the circuits. This can be easily done without the need to know the absolute values of each components.

In Figure 5, the normalized Fourier components for I_{DD} and I_{GND} are shown in the top and bottom half of the Figure, respectively. The resistive shorts are simulated by adding a resistance at the drains of the transistors. The range of the resistance values used is from 1 to 100Ω. The modeled resistor values have been selected such that the correct functionality of the NAND gates is still maintained properly. This implies that the fault is not easily detected by conventional testing method, such as functional test. The normalized Fourier components are markedly different from the components in Figure 4. It is slightly easier to detect the resistive shorts compared to the weak transistor faults.

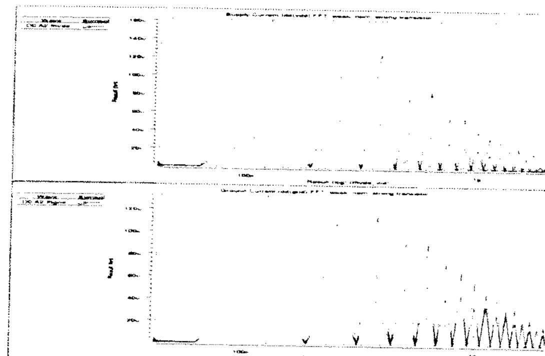

Figure 4: Normalized Fourier components for NAND with weak transistor defects.

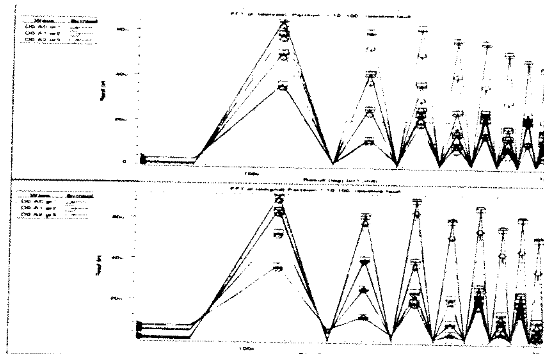

Figure 5: Normalized Fourier components for NAND with resistive shorts defects.

3.2 Pre-charged Domino Logic Circuits

A 4-input NAND gate, coupled with a static CMOS inverter, is used to verify the I_{DD} waveforms analysis for pre-charged domino circuits. The circuit used in the simulations is shown in Figure 6. The weak transistors and high resistive defects are then introduced in the circuit. During the pre-charge phase, by observing the I_{DD} and the I_{GND} currents, we can detect the weak transistor defects in the PMOS of the NAND gate and in the NMOS of the static CMOS inverter simultaneously (illustrated by the dashed arrow in Figure 6). Similarly, the faults in the NMOS stack of the NAND gate and in the PMOS of the static CMOS inverter can be detected simultaneously by observing the I_{DD} and

I_{GND} currents during the evaluation phase (illustrated by the solid arrow in Figure 6).

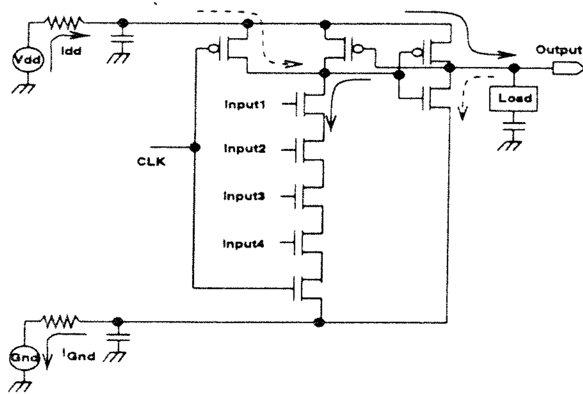

Figure 6: Simulation setup to obtain I_{DD} and I_{GND} waveforms for domino logic.

Figure 7 shows the comparison of the normalized Fourier components of both the I_{DD} and the I_{GND} current waveforms between the good circuit and the circuit with weak transistor defects. In order to be able to differentiate between the good circuit and the defective circuit, we again just observe the general shape of the Fourier components instead of focusing on the absolute values of each individual harmonics. The family of waveforms is obtained by varying the strength (width) of the transistors. By observing the first four or five harmonics of the I_{DD} (top half of Figure 7), it is possible to differentiate the good circuit and the defective circuit easily. For the I_{GND} (bottom half of Figure 7), unlike the I_{DD} waveforms counterpart, it is a bit harder to differentiate between the harmonics from the good circuit and the defective circuit.

Figure 8 shows the normalized Fourier components of the I_{DD} (top half of Figure 8) and the I_{GND} (bottom half of Figure 8) currents for both good circuit and the defective circuit with high resistive shorts. The family of the waveforms is obtained by varying the resistance fault values introduced in the circuit during simulation. Again, by observing the general shape of the waveforms instead focusing on the absolute value of each harmonics, it is possible to differentiate between the good circuit and the defective circuit with high resistive shorts.

4 Current Sensor

In order to carry out the I_{DD} waveforms analysis, a good method to safely measure the current waveforms is needed. We need an accurate current sensor which can faithfully observe the current waveforms without significantly distorting the waveforms. We have designed a simple current sensor which proves to be adequate in fulfilling our need in verifying the feasibility of using the I_{DD} waveforms analysis to try to detect faults in CMOS circuits. The schematic of the current sensor is shown in Figure 9. The circuit is a simple amplifier which senses the voltage difference at the source terminals of the PMOS transistors. The NMOS current mirror provides the load for the PMOS transistors. The reference voltage at the input gates of the PMOS transistors is set to a value such that all the transistors are in saturation mode. There are on-going studies in designing effective current monitor for both on and off-chip. The current sensor presented here is over-simplified and may not be suitable in practice because of the lack of voltage stabilization within the current mirrors. However, the main purpose of the current sensor here is to validate our test methodology and a more involved work on the current sensor can be done eventually in the future. The applicability of this current sensor is put to a test by using it to measure the I_{DD} waveforms in our simulations. The circuit under test is modeled by 100 serially connected static CMOS inverters. We obtained the output waveforms from the resistive voltage drop across the source terminals of the PMOS transistors. There are certain amount of distortions in the waveforms due to the lack of bandwidth in the current sensor. In typical CMOS circuits, the supply line capacitance is high, and this capacitance smooths out the current waveforms. As a single current sensor is being used for a large num-

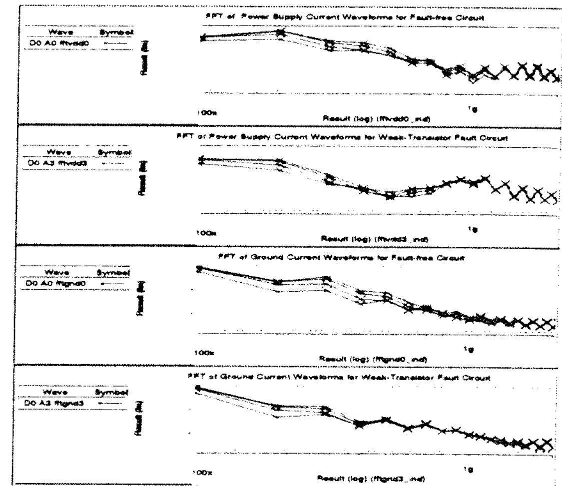

Figure 7: Fourier components for domino logic NAND gate with weak transistor faults.

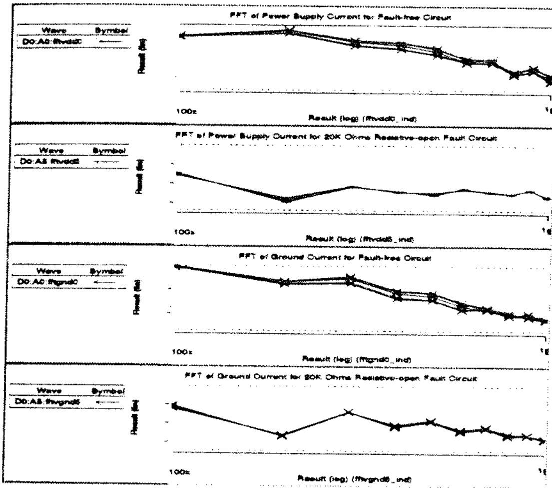

Figure 8: Fourier components of I_{DD} and I_{GND} waveforms for domino NAND with resistive shorts .

ber of gates, the current waveforms are slow enough that they can be adequately measured by the current sensor circuit.

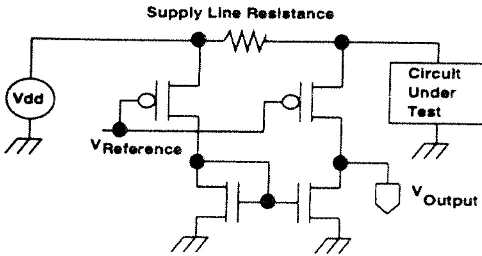

Figure 9: Current sensor.

We define the partition of the circuit to be a collection of gates with one current sensor. The supply current of all gates is measured simultaneously with a single current sensor. Partitions sizes in the range of 2 to 128 gates are simulated. Increasing the partition size causes a smoothing effect to the current waveforms, and also slows down the current waveforms which makes it easier for the current sensor to accurately duplicate the current waveforms. However, increasing the partition size makes it more difficult to observe the changes in the output waveforms. This is because the power supply line can be modeled as a low pass filter whose cutoff frequency is inversely related to the partition size. Hence, a loss of high frequency components occurs. From the simulation results for domino logic and FCMOS gates, we observe that a partition size of 64 identical gates can be safely used.

5 8-bit Adder

While the above results verify that the I_{DD} waveform analysis is capable of detecting defects which are undetectable by standard I_{DDQ} techniques, we need to verify further that the method is practically tenable for a large enough circuit. To verify this, we do SPICE simulations on a FCMOS 8-bit carry propagate adder.

The adder consists of standard 26-transistors FCMOS full-adders. The layout of the whole structure is done in HP CMOS 0.6μm process. The interconnect capacitances are fully extracted for simulation purposes. We introduce a 40Ω resistance in the power supply lead. Actual simulations show that the worst case supply noise is under 20mV. In practice, the 40Ω resistance can be achieved by using a small strap of polysilicon. The current sensor described in the previous section is used to sense the voltage across the 40Ω resistor.

We set the input test vectors such that the entire carry chain toggles by changing the *carry* input. We also ensure that all the *sum* outputs toggle. Using these inputs, we attempt to detect an error in the second bit position of the adder. Resistive shorts with resistances of 5, 10, and 20Ω are then simulated. We observe that although the fault causes the delay of the second stage to increase, the functionality of the adder remains unchanged. Figure 10 shows the voltage drop across the 40Ω resistor, which is around 20mV. The amplified output of the current sensor, shown at the bottom half, is around 360mV. It clearly shows that although the current sensor does not faithfully follow the actual waveforms, it does mimic the low frequency components well. We use the Fourier components over a large frequency range to highlight the lack of bandwidth. The clear difference in the Fourier components for the first three components makes it easy to detect faults in the circuit. The fact that the zero order component is identical in all the cases implies that the fault is undetectable by the standard I_{DDQ} testing methods. To diagnose that the fault is in the second bit position, it is sufficient to have the Fourier components from the faulty circuit to be pre-computed for various faults. These will be used as a reference for comparison to narrow down the fault location. However, this process can be time consuming. Alternatively, we can use a set of input test vectors which will toggle only a few nodes, by which we can narrow down the search area for the fault location. A fault in the NMOS stack shows up as an error in the I_{GND} waveform, while a

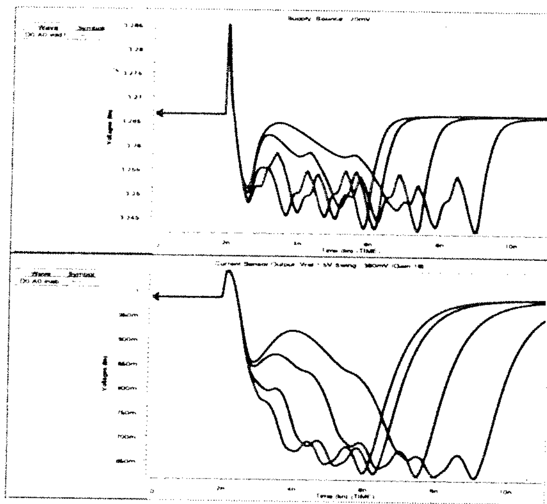

Figure 10: Current waveforms for an 8 bit adder.

fault in the PMOS stack shows up as an error in the I_{DD} waveform. In the above simulations, the fault is in the PMOS stack.

The fact that we can detect the fault in spite of all the outputs switching shows us that I_{DD} waveform analysis is quite a sensitive method. In fact, it may be possible that it detects faults which do not alter the proper operation of the circuit. A more significant contribution of this testing methodology is that it allows us to find marginal operation defects in both static and dynamic logic families.

6 Summary and Future Research

I_{DDQ} testing is a widely used technique to detect faulty CMOS circuits because of its effectiveness in detecting shorts and certain opens. However, I_{DDQ} testing significantly loses its effectiveness when it is applied to large circuits with small feature sized devices where the leakage component is high. I_{DDQ} testing is also not capable in detecting defects such as high resistive shorts and weak transistors, which do not substantially alter the quiescent current. Unlike I_{DDQ} testing, I_{DD} waveform analysis can be easily applied to dynamic logic and low power, low voltage threshold logic circuits. I_{DD} waveform addresses all these issues by the following techniques:

• Partition the circuit into smaller blocks and use built-in current sensors to measure the current of these blocks.

• Measure the waveforms generated by the I_{DD} current rather than the average current. We explicitly look at the first, second and third harmonics of the current waveforms and discard the zero order component. Hence, constant DC component like leakage current does not affect this technique.

• Most defects, which cause a change in the pull down or pull up strength of NMOS or PMOS stacks, cause a change in the I_{DD} waveform and can thus be detected. Furthermore, as we have shown, the I_{DD} waveform analysis method is sensitive enough to detect small resistance shorts.

• I_{DD} waveform analysis also acts as a fault diagnosis tool because of the capability of simultaneously monitoring a number of output nodes.

While this paper shows the viability of I_{DD} waveform analysis, it is lacking in methods and algorithms for applying test vectors to locate faults. However, any method which can cause transitions to propagate from input to output while simultaneously prevent the gates at the same level from switching should suffice.

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