THE CHINESE ABACUS METHOD: CAN WE USE IT FOR DIGITAL ARITHMETIC?

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ABSTRACT

This paper discusses how to apply the approach used in the Chinese Abacus to implement digital arithmetic. Firstly, we examine the representations and the basic techniques used in the Chinese Abacus; then, we propose a MOS realization of the basic functions required; finally, we discuss a novel 12 bit full adder based on the Chinese Abacus method. Simulations of 0.5 μm CMOS realizations showed that a parallel solution can run at 200 MHz while a pipeline realization can achieve 1 GHz of clock frequency. The complexity of the circuit is quite limited; thus, the use of the Chinese Abacus approach results a competitive technique with respect to conventional methodologies.

1. INTRODUCTION

The Chinese Abacus is a very popular technique used for centuries in many parts of the world (mainly in China) to perform arithmetic functions. The use of the Chinese Abacus is very efficient and a trained operator often compete with electronic pocket calculators.

Similar efficiency can be attained in an electronic version; therefore, with this paper we consider advantage and disadvantages for a possible implementation of a Chinese Abacus calculator. Firstly we recall the techniques used to perform basic arithmetic operations. Then, we identify the basic functions required and we study the speed performances using a 0.5 μm CMOS technology comparing them to similar published implementations [1], [2]. On the basis of the achieved results, our conclusion is that a suitable combinations of basics blocks allows us to build a pretty fast Chinese Abacus calculator while using a limited chip area.

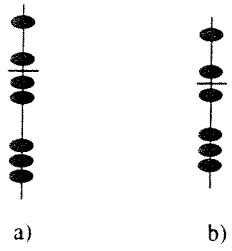

Fig. 1 - a) Chinese Abacus Coding of the decimal number 7
b) Coding with base 4 of the decimal number 5

2. USE OF THE CHINESE ABACUS

The Chinese Abacus is made up of a set of unity elements representing the various decades of decimal numbers. Each element has five beads having a unity weight and two beads having a weight of five. The configuration shown as Fig. 1 a) represents the number 7.

The coding rule in the main part of the Abacus is thermometric, thus, to represent a number lower than 5 the same number of beads will be raised in the main part unit. For numbers higher than 5 one bead with weight 5 will be lowered. In such a way, a basic element is able to represent a decimal number comprised in the range from 0 (all beads equal to 0) to 15 (all beads equal to 1). The key feature of the Chinese Abacus is the use of two beads with weight 5. This allows the operator to minimize the transmission of rests, which even in electronic circuits, is a limit to speed. Moreover, the use of the thermometric code permits fast implementation of elementary arithmetic functions like addition and subtraction.

The number representation of the Chinese Abacus refers to the digital numeric system. As we are mostly interested in binary based coding, it is more convenient to use a basic element made up of 4 unity-weight beads and two beads having a weight of four units (see Fig. 1 b)). In practice, we use a base of 2^2=4, and the basic element is able to represent decimal numbers in the range from 0 to 12. The configuration shown in Fig. 1 b) represents the number 5.

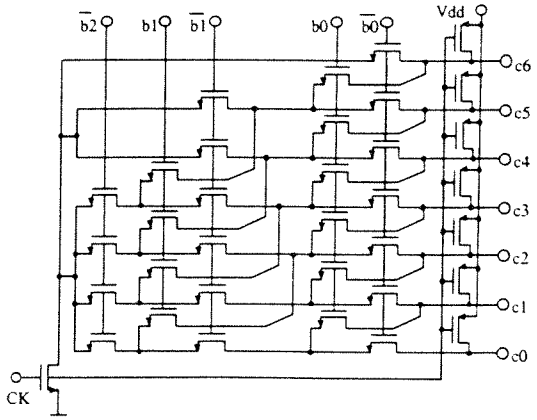

Fig. 2 - Binary to thermometric representation (B/T)

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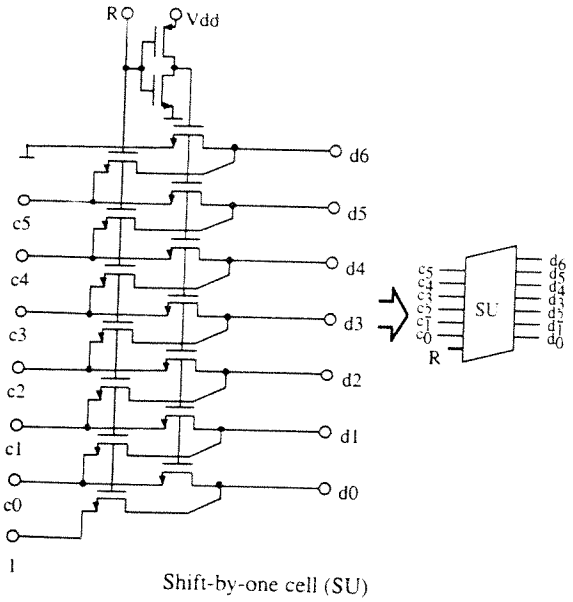
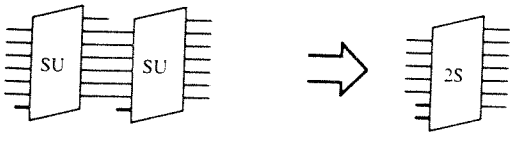
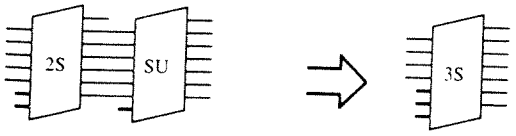


Shift-by-one cell (SU)



Two shift-up commands(2S)



Three shift-up commands(3S)

Fig. 3 - Shift-up blocks

Here again, the given coding is able to represent numbers exceeding the full scale by half of the base of the numeric system. Having over-scale room is the key to the operation of the method.

Basic arithmetic functions are achieved by moving the beads in the Chinese Abacus according to a number of simple rules. For example, in the addition operation one of the addendum is established in the Abacus and the other is used to change the Abacus configuration by rising beads in the main parts or by lowering beads in the upper parts. We don't give here details on how to achieve other functions: the used techniques are mainly based on the same basic operations.

3. CHINESE-BEAD BASIC BLOCKS

An analysis of the Chinese abacus use permitted us to identify the following key functions:

- Binary-to-Thermometric (B/T) (or Digital to Thermometric) transformation
- Shift-up by one, two or three (SU, 2S, 3S) beads

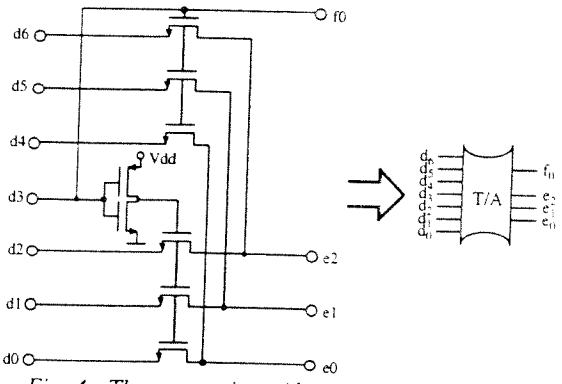


Fig. 4 - Thermometric to Abacus conversion (T/A)

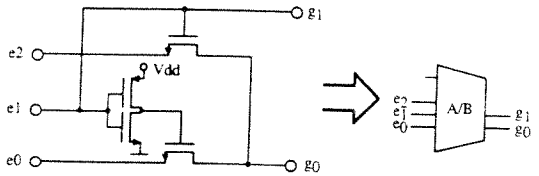


Fig. 5 - Abacus to Binary converter (A/B)

- Thermometric-to-Abacus (T/A) transformation
- Abacus-to Binary (A/B) transformation, to achieve the result back in the normal binary representation.

We propose to carry out the above functions using the pass transistor approach [3]. Fig. 2 shows a converter from 3 bits to thermometric representation (B/T). The control is given by the inputs b_0, b_1 and the complements $\overline{b}_0$, $\overline{b}_1$, $\overline{b}_2$. The output is made by a thermometric 0 representation or high impedance [4]. When the output nodes are in the high impedance condition they are set to 1 during Cl=0 by the precharge to a logic 1.

The SU function is achieved by the circuit in Fig. 3. It shifts up (SU) the input by one position and provides an extra one on the output, d_0. The two shift-up block is depicted in the Fig. 3 as well, it utilizes the shift-up symbol with two shift-up commands and the label 2S; moreover, the cascade of a 2S block and a SU block (that will be used shortly) is represented similarly using the label 3S. The 2S and 3S blocks have two and three shift-up input commands respectively; a ticker line distinguish these inputs.

Fig. 4 shows the thermometric-to abacus (T/A) transformation (with 6 inputs). The logic input d_3 is used to switch the inputs d_0, d_1 and d_2 or the inputs d_4, d_5 and d_6 towards the lower beads e_0, e_1 and e_2. The input d_3 itself constitutes the value of the upper bead, f_0. The A/B function is performed by the circuit in Fig. 5. The operation of this simple circuit is self-explaining.

The basic blocks described above are quite fast since they are based on the pass transistor logic; moreover, the number of pass transistor is always limited to 4. To have a quantitative figure of the speed we simulated the basic blocks using a digital 0.5 μm CMOS technology. Fig. 6 shows the transient response of the circuit in Fig. 2 cascad-

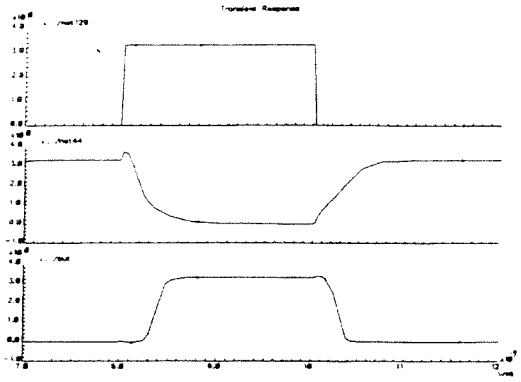


Fig. 6 - Transient response of the B/T converter

ed with the thermometric to abacus conversion (Fig. 4) The worst-case situation of the input signals are used. We have two plots; one is the direct output of the block and the other is the same response passed through a CMOS inverter. It can be observed that the delay between the clock edge and the data at the output is less than 0.5 nsec. On the basis of this preliminary figure we can expect an excellent speed of operation compared with recent published works [5], [6]; moreover, we have an early indication of the benefits of the proposed approach.

4. THE CIRCUIT OF THE SUM OPERATION

The basic blocks discussed in the previous section can be properly combined to achieve arithmetic functions. Below we provide an example of a possible architecture: an N bits full adder (we use N=12 but the method can be extended to any N value thanks to the modularity of the architecture).

The operation required is:

$$\bar{G} = \bar{A} + \bar{B} \tag{1}$$

$$\bar{A} = a_N 2^N + a_{N-1} 2^{N-1} + \ldots + a_1 2^1 + a_0 2^0 \tag{2}$$

$$\bar{B} = b_N 2^N + b_{N-1} 2^{N-1} + \ldots + b_1 2^1 + b_0 2^0 \tag{3}$$

$$\bar{G} = g_{N+1} 2^{N+1} + g_N 2^N + \ldots + g_1 2^1 + g_0 2^0 \tag{4}$$

The sum results from the following partial sums

$$G_{\alpha,\beta,\gamma} = A_{\alpha,\beta,\gamma} + B_{\alpha,\beta,\gamma} \tag{5}$$

$$A_{\alpha,\beta,\gamma} = a_\alpha 2^2 + a_\beta 2^1 + a_\gamma 2^0 \tag{6}$$

$$B_{\alpha,\beta,\gamma} = b_\alpha 2^2 + b_\beta 2^1 + b_\gamma 2^0 \tag{7}$$

Where the indexes (α,β,γ) are (2,1,0); (5,4,3); (8,7,6) and (11,10,9). The sum $\bar{G}$ is then given by

$$\bar{G} = G_{2,1,0} + G_{5,4,3} 2^3 + G_{8,7,6} 2^6 + G_{11,10,9} 2^9 \tag{8}$$

Thus, we calculate the sum by adding three by three the bits of the two addenda; this allows us to use conveniently the B/T block in Fig. 2 and the T/A block in Fig. 4 to represent three bit words into Abacus form. The operation of the entire full adder and the partial sums $G_{\alpha,\beta,\gamma}$ will be discussed with the help of Fig. 7. It shows the lower half of the entire circuit and calculates the first two terms of equation (8). If we concentrate our attention on the lower part of Fig. 7 we notice two B/T blocks which provide the ther-

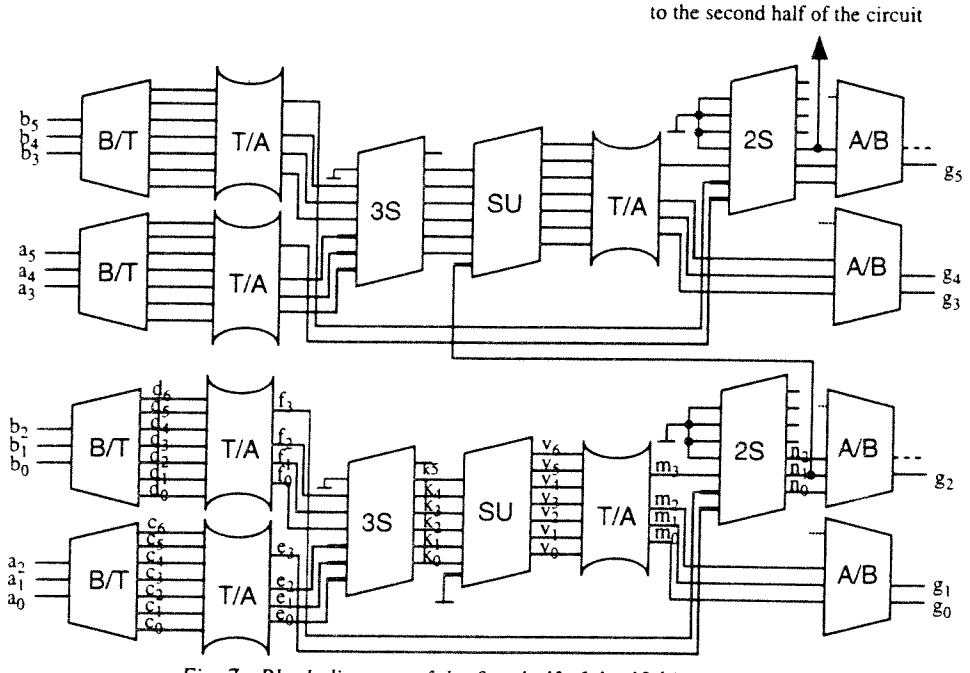


Fig. 7 - Block diagram of the first half of the 12 bits full adder

mometric outputs C and D; they are transformed into Abacus by the cascaded T/A converters. The maximum thermometric code at the outputs C and D corresponds to 7: thus, only one upper bead is necessary. Now we have to add the lower beads of E and F and this is done by the same method followed by a Chinese abacus operator: he/she changes the beads configuration of one addendum by raising as many beads as the number of the other addendum; the upper bead is then lowered in the case the lower representation exceeds the full scale. The circuit in Fig. 7 accomplishes this operation in three steps: the (3S) block provides the thermometric representation of the sum, a SU block accounts for a possible carry coming from the lower stage (not present in the first chain of our architecture) and, finally a T/A converter transforms the thermometric result into Abacus. Obviously, the maximum output K is 6, a possible rest rises it to 7 and the T/A converter must provide at the output only one upper bead, m_3.

Next stage of the chain combines the upper beads e_3 and f_3 with m_3, and finally all the result is transformed into binary by A/B converters. When $G_{2,1,0}$ is equal to or more than 8 (n_1=1), there is a carry. It is transferred to the upper chain by the command to the SU block.

The circuit in Fig. 7 performs the sum operation in one clock period; however, it is also possible to accomplish the sum using a pipeline solution. The given architecture can be directly transformed into a pipeline by braking the processing chain in a number of stages. Just a few modifications are required. Namely, it is necessary to add digital storing elements to preserve logic signals during precharge periods and pass them to the successive pipeline stage.

5. Simulations and Implementation

We have simulated the proposed circuit with Spice using the transistor models of a 0.5μm CMOS process [7]. The results obtained for the parallel implementation and the pipeline implementation of the 12 bit adder are summarized in Table 1. We can notice that for the pipeline implementations the precharge phase and the I/O delay due to the transfer-gate operation are less than 0.5 nsec. Therefore the maximum possible clock frequency is, in the nominal case, 1 GHz. By contrast, the delay due to the long chain of pass transistors used in the parallel implementation slows down the speed to 200 MHz.

The total number of transistors required by the circuits is limited, it is 792 and 1472 respectively for the parallel and pipeline realization. These figures are quite acceptable for the functions implemented. Moreover a custom layout allows a good compactness to be obtained. A possible layout shown in Fig. 8 for the binary-to-thermometric converter: we can accommodate 35 transistors within a 22 x 25 μm space, leading to an area per single transistor which is as small as 16 μm^2. Assuming that the overhead for block interconnections is 100% of the basic block area we can estimate that the entire 12 bit pipeline full adder can be accommodated in 0.05 mm^2. The above estimation is rough; nevertheless, the result achieved gives us an idea of the possible chip area of the proposed solution. Thus, the proposed approach permits to increase the speed significantly while requiring a limited silicon area.

PARAMETER	PARALLEL	PIPELINE
# of pass trans.	19	4
Pre-charge delay	2.46 nsec	0.44 nsec
I/o delay	2.49 nsec	0.48 nsec
Max Frequency	200 MHz	1 GHz
Trans. count	792	1472

Tab. 1 - Features of the Abacus arithmetic circuit

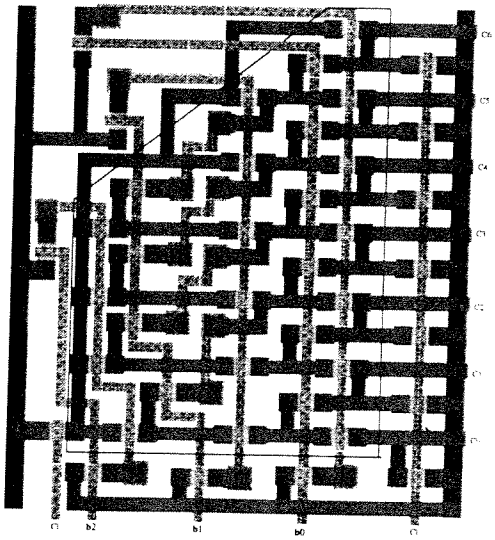


Fig. 8 - Layout of the B/T converter

Acknowledgments

We thank G. Torelli for helpful discussions. Chen Gang acknowledges the bursary support of the Italian Ministry of Foreign Affairs.

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