Modeling of Shift Register-based ATM Switch

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Abstract

In this paper, we present the modeling of shift register-based ATM switch to find the cell loss probability, throughput and delay. The results are compared with other switch architectures based on input queueing, input smoothing, output queueing and completely shared buffering. It is observed that although our switch is an input-buffered switch, it's performance is better than other switches based on traditional queueing approaches.

1 Introduction

It is well known that head-of-line (HOL) blocking limits the throughput of an input-queued switch with FIFO queues to approximately 58%. Many different switch architectures have been proposed to improve the throughput of input-queued switches. In these switch architectures, rather than maintaining a single FIFO queue for all cells, each input port maintains a separate queue for each output [1] [2]. Thus for an N-input switch, N FIFOs are maintained by each input port. HOL blocking is eliminated because a cell is not held up by a cell queued ahead of it that is destined for a different output. However, the main drawbacks of these switch architectures are

- Complex design with too many buffers.
- A global scheduling protocol is needed to coordinate the FIFOs.
- For a given priority class, a set of N FIFOs has to be maintained at each input.

We proposed a new ATM switch which overcomes HOL blocking and is simple in design and hardware implementation [3]. The performance analysis of this switch is done in [4] by finding cell loss probability using numerical simulation. Since the simulation was run for one million time slots, cell loss probability up to the order of 10^{-6} can be reached. However, numerical simulation is impossible for investigating cell loss probabilities of the order of 10^{-12}. In this paper, analytical modeling of the new switch is done to find cell loss probability, throughput and delay.

The paper is organized as follows. In Section 2, the architecture of shift register based ATM switch is briefly reviewed. Section 3 deals with the switch modeling to find cell loss probability, throughput and delay. Section 4 discusses the results and compares the performance of the proposed switch with switches based on traditional queueing approaches. Section 5 concludes the paper.

2 Proposed Switch Architecture

The block diagram of shift register-based ATM switch is shown in Fig. 1. The main features of the switch are

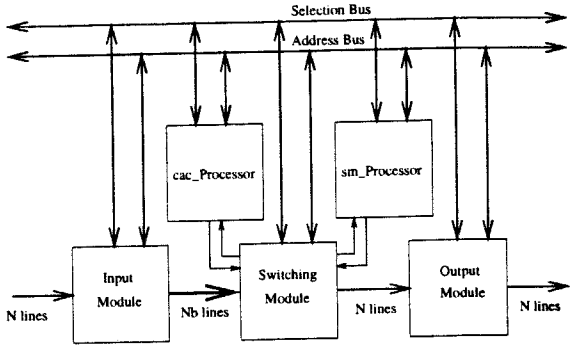

Figure 1: Block diagram of the switch architecture.

- Cells are stored in shift register buffers located in the input module. Each input port has its own bank of input buffers.
- All shift registers are directly connected to the switching module to overcome HOL and low throughput problems.

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- The switching module routes cells between input and output ports in bit serial format. Hence no serial-to-parallel conversion is required.
- All cells are routed simultaneously and internal data rate matches the line rate.
- Each output port has virtual output queues to store only the addresses of the cells stored in the input buffer and destined to that port.
- The switching module is a crossbar switch. However, it does not suffer from output blocking because the switch is driven by its outputs and not by its inputs.
- Connection admission control (CAC) and operation and management (OAM) functions are supported by the switch.
- QOS and multicast functions are provided by the switch.

In the switch there are two buses connecting the modules: address bus and selection bus. The address bus carries the input buffer address, where a particular cell is stored. The selection bus carries the destination port address. When a cell arrives at an input port, it is stored in an empty shift register buffer. The address of the input shift register buffer where the cell is stored is written in the corresponding virtual queue of the destination port through address bus and selection bus. For multicast or broadcast cells, it may be required to write the address of input shift register buffer in the virtual queue of more than one output port.
Routing of a cell is done in the following way. From the virtual queue of an output port a cell address is selected. This address selects a shift register buffer using the address bus. The output port plus the contents of the address bus provide the necessary routing information for the switching fabric.

3 Modeling the Switch

In this section, modeling is done for an $N \times N$ switch with b shift register buffers in each input port and Nb buffers in the virtual queue of each output port. Analysis is done to find the cell loss probability, throughput and delay. The following assumptions are made for modeling the switch.

- Cell arrivals on the N inputs is modeled by independent and identical Bernoulli processes.
- In any given time slot, the probability that a cell will arrive on a particular input is p.
- Each cell has equal probability $1/N$ of being addressed to any output port and its address is written in the virtual queue of that port.
- Within the virtual queue of a given output port a cell has equal probability of being selected by the output scheduler.
- Cell loss due to time out is not considered i.e. a cell is not lost even if it is delayed by more than a certain given time.

3.1 Cell loss modeling

Let us define the random variable A as the number of cells arriving at the switch inputs and destined for a particular output in a given time slot. Then A^i denotes the number of cell arrivals destined for output port i. For finite N, A^i depends on $A^j (j \neq i)$. This is due to the fact that at most N cells arrive to the switch, a large number of cells arriving for one output implies a small number for the remaining outputs. As N increases, A^i becomes an independent Poisson random variable (with mean value p). We will use the Poisson and independence assumptions even for finite N [5]. Thus the probability that k cells are destined to an output port is given by the Poisson distribution

$$a_k = Pr[A = k] = \frac{p^k e^{-p}}{k!} \quad k = 0, 1, 2, \ldots \quad (1)$$

Let us define another random variable Q as the steady-state number of cell addresses stored in the virtual queue of a particular output port at the end of a given time slot. Then Q^i denotes the steady-state number of cell addresses stored in the virtual queue of output port i. The virtual queue of each output port is modeled as an $M/D/1$ queue for which the steady-state queue size probabilities are obtained directly from the balance equations for the Markov chain shown in Fig. 2. Equations (2)-(5) numerically provide the steady-

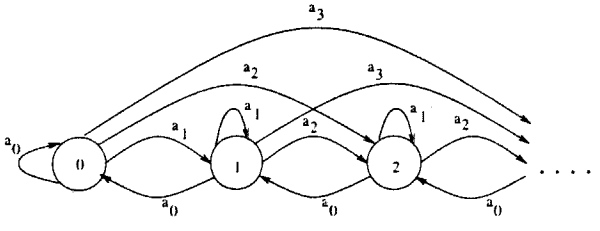


Figure 2: The discrete-time Markov chain state transition diagram for the output queue size.

state queue size probabilities [1].

$$q_0 = Pr(Q=0) = 1-p \tag{2}$$

$$q_1 = Pr(Q=1) = \frac{(1-a_0)}{a_0} \cdot q_0 \tag{3}$$

$$q_2 = Pr(Q=2) = \frac{(1-a_1)}{a_0} \cdot q_1 - \frac{a_1}{a_0} \cdot q_0 \tag{4}$$

$$\vdots$$

$$q_n = Pr(Q=n) = \frac{(1-a_1)}{a_0} \cdot q_{n-1} - \sum_{i=2}^{N} \frac{a_i}{a_0} \cdot q_{n-i} - \frac{a_{n-1}}{a_0} \cdot q_0 \quad n > 2 \tag{5}$$

Let us define the random variable S as the steady-state total number of cell addresses stored in output. Then

$$S = \sum_{i=1}^{N} Q^i \tag{6}$$

The steady-state probability that the total number of cell addresses stored in output is k is given by

$$s_k = Pr(S=k) = Pr(\sum_{i=1}^{N} Q^i = k) \tag{7}$$

The steady-state probability s_k can be calculated by the N-fold convolution of $NM/D/1$ queues [5].
Let us assume that each input port has infinite buffers. However, if an input port has more than b cells, it is evident that cell loss will take place because each input port actually has b buffers only. Let P_0 denote the probability that no cell is lost and P_{0k} denotes the probability that no cell is lost when k cell addresses are stored in the outputs. Then probability that no cell is lost is given by

$$P_0 = \sum_{k=0}^{\infty} \text{Prob.[no cell is lost} \mid k \text{ cell addresses stored in outputs]} \cdot \text{Prob.[}k \text{ cell addresses stored in outputs]}$$

$$P_0 = \sum_{k=0}^{\infty} P_{0k} \cdot s_k \tag{8}$$

[1] The steady-state queue size probabilities in Eqns. (13)-(15) of reference [6] are for the case when cell flows through the switch without suffering any delay i.e. a cell arriving in a given time slot may be transmitted out in the same time slot. In our case there is a minimum delay of one time slot. An arriving cell is not transmitted out in the same time slot and hence the modifications to (2)-(5).

If CLP denote the cell loss probability in the switch then

$$CLP = 1 - P_0 \tag{9}$$

If the total number of cell addresses in the output is less than or equal to b then there will be no cell loss. This is because, in the worst case, all the addresses stored in the outputs may be due to cells stored in one input port. Since each input port has b shift register buffers to store cells, there will be no cell loss. If the total number of cell addresses in the output is k, where k is greater than b but less than or equal to Nb, then cells may be lost due to one or more input ports being full. In this case, if P_{Fl} denote the probability that l input ports are full then

$$P_{Fl} = (\text{Prob.[more than } b \text{ cells are stored in a particular input port]})^l \cdot \text{Prob.[choose } l \text{ ports from } N \text{ ports]}$$

$$P_{Fl} = (r_k)^l \cdot I_l \tag{10}$$

But, probability that more than b cells are stored in a particular input port is given by

$$r_k = 1 - \sum_{l=0}^{b} \text{Prob.[}l \text{ cells are stored in a particular input port]}$$

$$= 1 - \sum_{l=0}^{b} a_{kl} \qquad b+1 \le k \le Nb \tag{11}$$

where a_{kl} denotes the probability that the input port contains l cells out of a total of k cells. But, probability that l cells are stored in a particular input port is given by

$$a_{kl} = \binom{k}{l} (\frac{1}{N})^l (1-\frac{1}{N})^{k-l} \quad \begin{cases} b < k \le Nb \\ 0 \le l \le b \end{cases} \tag{12}$$

Also, the probability of selecting l input ports out of N ports is given by

$$I_l = \binom{N}{l} (\frac{1}{N})^l (1-\frac{1}{N})^{N-l} \quad l = 0, 1, \ldots, N \tag{13}$$

Thus, probability that none of the input ports are full if k cell addresses are stored in the output is given by

$$P_{0k} = 1 - \sum_{l=1}^{v} \text{Prob.[}l \text{ ports are full]}$$

$$P_{0k} = 1 - \sum_{l=1}^{v} I_l \cdot (r_k)^l \quad \begin{cases} v = k \bmod b \\ b < k \le Nb \end{cases} \tag{14}$$

Also, if the total number of cell addresses in the output is greater than Nb then it is sure that there is cell loss. This is because, in the best case, all the addresses stored in the output may be of the cells which are equally divided in all input ports. Even in this case, it is sure that shift register buffers of at least one port is full. Thus

$$P_{0k} = \begin{cases} 1 & 0 \le k \le b \\ 1 - \sum_{l=1}^{v} I_l \cdot (r_k)^l & \begin{cases} v = k \bmod b \\ b < k \le Nb \end{cases} \\ 0 & k > Nb \end{cases} \quad (15)$$

By using equations (6)-(15), cell loss probability in shift register-based ATM switch is given by

$$CLP = 1 - \sum_{k=0}^{Nb} P_{0k} \cdot s_k \quad (16)$$

3.2 Throughput modeling

In output buffered switches a cell is always transmitted out if the output queue is not empty. Similarly, in shift register-based ATM switch, one address from the virtual queue of each output port is selected and the corresponding cell from input buffer is transmitted out through cell switch fabric. Thus, a cell will always be transmitted from each output port if the output virtual queue is not empty. Thus, similar to output buffered switches, an optimal throughput is achieved in shift register-based ATM switch. If ρ_0 denote the throughput of shift register-based ATM switch then it is given by [5]

$$\rho_0 = p(1 - CLP) \quad (17)$$

Thus, the normalized throughput R is given by

$$R = \frac{\rho_0}{p} \quad (18)$$

Thus, we are able to study the switch throughput if the switch CLP is determined.

3.3 Delay modeling

In shift register-based ATM switch, one address from the virtual queue of each output port is selected and the corresponding cell from input buffer is transmitted out. This cell address is selected from the virtual queue of each output port on a First-Come-First-Serve (FCFS) basis in order to preserve the cell sequence. Thus, the virtual queue of each output port is a FIFO buffer. Hence, the mean waiting time (T) for a cell in an output FIFO is obtained from Little's result and is given by

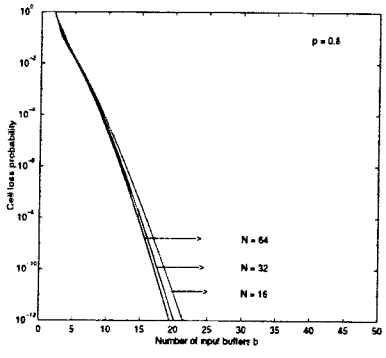
$$T = \frac{C_{avg}}{\rho_0} \quad (19)$$

where C_{avg} is the average number of cell addresses present in the output FIFO virtual queue and is given by

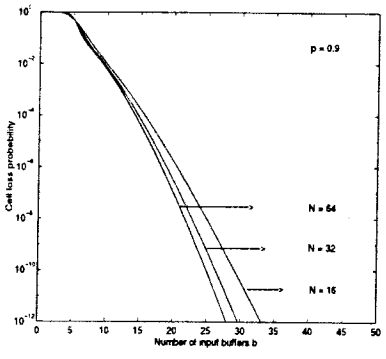
$$C_{avg} = \sum_{n=1}^{Nb} n \cdot q_n \quad (20)$$

Thus, we are able to study the mean waiting time in shift register-based ATM switch.

4 Results



(a)



(b)

Figure 3: Cell loss probability for shift register-based ATM switch. (a) Traffic load = 0.80. (b) Traffic load = 0.90.

Cell loss probability, throughput and delay are calculated using the formulas developed in the previous section and the results are discussed. Fig. 3. shows the cell loss probability for different values of N and

traffic load of 0.8 and 0.9. The throughput of shift register-based ATM switch is shown in Fig. 4. for $N = 16$ and traffic load $= 0.90$. Thus, it is seen that

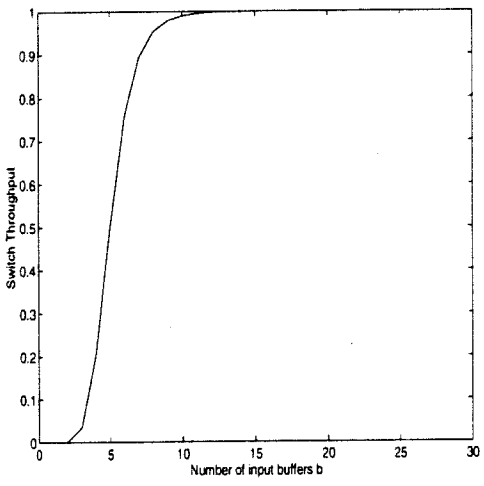


Figure 4: Throughput for shift register-based ATM switch, $N = 16$, $p = 0.90$.

100% throughput can be achieved in shift register-based ATM switch.

Fig. 5. shows the mean waiting time for different traffic loads. The number of input buffers b is 35, large enough to have very small cell loss probability. It can be seen that there is a minimum delay of one time slot in shift register-based ATM switch. The performance of shift register-based ATM switch

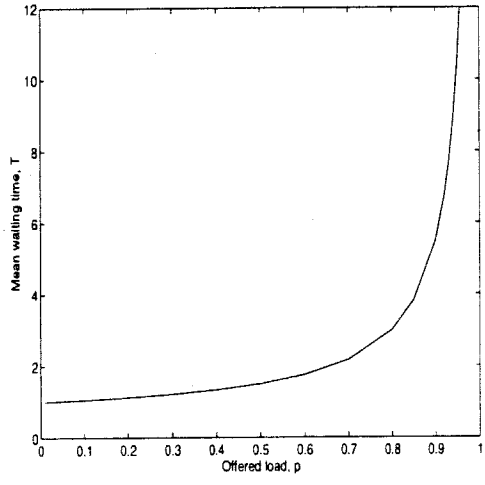


Figure 5: Mean waiting time for shift register-based ATM switch, $N = 16$, $b = 35$.

is compared with the performance of switches based on input queueing, input smoothing, output queueing and completely shared buffering in Fig. 6. It can be

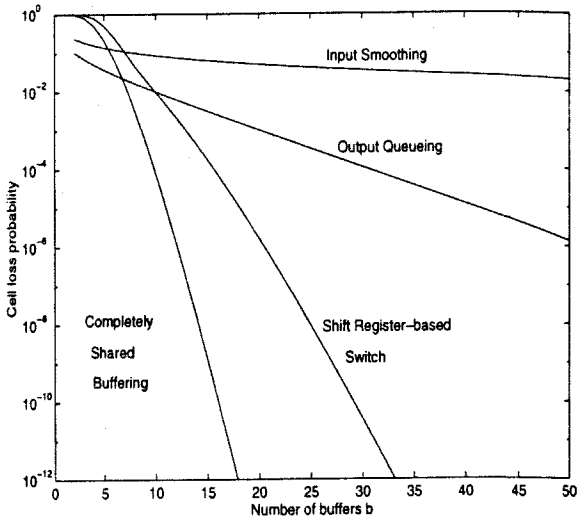


Figure 6: A comparison of cell loss probabilities, $N = 16$, $p = 0.90$.

seen that for same number of buffers, shift register-based ATM switch has lower cell loss probability as compared to input smoothing and output queueing switches. One reason for lower cell loss probability in shift register-based ATM switch as compared to output queueing is that in output queueing at most N cells can enter the buffer in a particular time slot and only one cell can go out in that time slot. However, in shift register-based ATM switch only one cell enter the buffer in a particular time slot and at most N cells can go out in that time slot. The cell loss probability is much lower in case of completely shared buffering switches. Also, the number of inputs/outputs grow as Nb in input smoothing switches and as $N(b+1)$ in completely shared buffering switches [5]. However, in shift register-based ATM switch only the number of inputs grow as Nb.

5 Conclusion

In this paper modeling of shift register-based ATM switch is done to find numerically the cell loss probability, throughput and delay. The performance is compared with other traditional queueing approaches in ATM switch. It is observed that to achieve desired cell loss probability, less number of input shift register buffers is required. Also, an optimal throughput-delay performance is achieved in this switch.

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