A NOVEL 1.5-V CMOS MIXER

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Abstract

New and simple CMOS mixer powered with 1.5 V is presented. It works with a 200-MHz clock, and has a -7-dB IP_3. Moreover, it elaborates signals up to 150 mV with 1-dB compression point. The particular topology makes it useful for an integration in fully digital ICs.

I. INTRODUCTION

In the last years low voltage has become a target in most of digital and analog integrated circuit (IC) applications because this allows to reduce the power dissipation, which, in turn, means both an increase in the packing density of IC, and an increase of the battery life-time in portable equipment. Therefore, design of analog ICs with a low power supply is becoming mandatory, and a great effort is devoted to develop new solutions working with a 1.5-V or even less power supply [1-4].

Moreover, thanks to the reduction of transistor dimensions, CMOS analog circuits are now able to process high frequency signals and the non-linear circuits, belonging to this family [5-12], are used in some fundamental building blocks of RF transceiver systems [13-16].

One of the most useful non-linear block, which has wide applications in RF systems, is the multiplier [17-19]. Indeed it is a basic building block to perform various non-linear function. When the multiplication is performed between an input signal and a clock signal but its output is independent on the clock amplitude (i.e., the multiplication is performed between the input signal and the clock sign) we say that the multiplier is a modulator (or mixer) which is widely used to perform up and down frequency conversion in RF systems [20-24].

In this communication a new and simple CMOS mixer is presented. It works with a power supply of 1.5 V and a 200-MHz clock, it has a -7-dB IP_3 and elaborates signals up to 150 mV with 1-dB compression point. Moreover, its particular topology makes it useful for an integration in fully digital ICs..

II. CIRCUIT DESCRIPTION

The proposed circuit is shown in Fig. 1. Transistors M1-M2, biased by M3, realize the input stage and perform a voltage-to-current conversion. The common mode bias voltage was set to 1.2 V. With this bias value, transistors M1-M2 can accept signals with an amplitude of few hundred of mV giving two currents, i_{d1} and i_{d2}, which can be considered linearly related to the differential input as follows

$$i_{d1} = g_{m1,2}\frac{v_{in}}{2} \tag{1.a}$$

$$i_{d2} = -g_{m1,2}\frac{v_{in}}{2} \tag{1.b}$$

Transistors M8-M9 and M10-M11 are two folded current mirrors which acquire the output of the transconductor and feed it to the common node of the two sources coupled pair M4-M5 and M6-M7. Indeed i_{d1} and i_{d2} will flow through the low resistance of diode-connected transistors M8 and M10 and will be mirrored to the drain of M9 and M11 respectively.

The two clock signals, V_{CK1} and V_{CK2}, generated by the circuit shown in Fig. 2, are two squared waveforms in opposition of phase and will drive transistors M5-M6 and M4-M7, respectively. All transistors M4-M7 work as switches and perform the modulation. Indeed, when V_{CK} is high, V_{CK1} is high and V_{CK2} is low, which in turn means transistors M5 and M6 switched on and transistors M4 and M7 switched off. Thus currents i_{d1} and i_{d2} flow through M5 and M6 and will be further mirrored with the folded mirrors M12-M13 and M14-M15, resulting in the output voltage, V_o, given by

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$$v_o = (i_{d1} - i_{d2})R_o = g_{m1,2}R_o v_{in} \quad (2)$$

On the other hand, when V_{CK} is low, V_{CK1} is low and V_{CK2} is high. In this case transistors M4 and M7 are switched on and currents i_{d1} and i_{d2} will flow through them and will be mirrored with M12-M13 and M14-M15. Therefore, now we get the output voltage of (2) with the opposite sign

$$v_o = -(i_{d1} - i_{d2})R_o = -g_{m1,2}R_o v_{in} \quad (3)$$

Relationships (2) and (3) show that output signal, v_o, is independent on the clock signal amplitude and, as a first approximation, only depends on both the aspect ratio and the bias current of the differential stage and on the value of output resistors, R_o.

Moreover, since (2) holds for V_{CK} high and (3) holds for V_{CK} low, both relationships can be rewritten into a single one as follows

$$v_o = g_{m1,2}R_o \,\mathrm{sgn}(V_{CK})v_{in} \quad (4)$$

which, as expected, describes the modulating operation.

The two clock signals driving the modulator are generated by the circuit in Fig. 2. As far as this is concerned, it is able to generate two squared waveforms in opposition of phase starting from a sinusoidal one. To get this target the circuit is made of a series of inverter stages of different area in order to properly drive the capacitive load offered by the modulation stage. To obtain the opposition of phase, V_{CK1} is realised by cascading two inverter while V_{CK2} by cascading three of them. But at the modulator working frequencies, the propagation delays of the two paths will be different and the modulator would not work properly. To avoid this problem a dummy stage, performed by transistors M30-M31, has been included in the shorter path in order to add an extra delay in the propagation of V_{CK1}, thus getting an equal propagation delay in both the paths.

III. SIMULATION RESULTS

The proposed circuit has been simulated with SPECTRE using the model parameters of a 1.2-μm CMOS process.

The circuit parameters are summarised in Tab. I. All the simulations have been performed with a 200-MHz and 1.5-V_{pp} sinusoidal clock signal and in order to get a 10-MHz centred output signal. The power supply and the common mode input voltage was set to 1.5 V and 1.2 V, respectively.

A qualitative characterisation of the circuit is shown in Fig. 3 in which its output time response to a 190-MHz and 50-mV input signal is given.

In the first place, analysis of circuit non-linearity has been done in terms of 1-dB compression point. Results of transient simulations realized for increasing input values from 25 mV to 175 mV are summarized in Fig. 4 where the gain factor (expressed in dB) versus the input voltage is plotted. The modulator exhibits a gain factor of 4.8 dB and reaches its 1-dB compression point for an input signal greater than 150 mV.

A performance index for characterising a modulator stage can be obtained by calculating IM_3 for a given input value of amplitude. Simulations have been performed by driving the circuit with a two-tone input signal of 189.5 MHz and 190.5 MHz in order to obtain a two-tone 10 MHz centred frequency output. The frequency response to a two tone input signal with 25 mV of amplitude is shown in Fig. 5. We get an output signal with two fundamental components at 9.5 MHz and 10.5 MHz of 43.1 mV of amplitude (-27.3 dBV) and two spurious component at 8.5 MHz and 11.5 MHz of 136 μV of amplitude (-77.3 dBV) which yields to an IM_3 of 50.0 dB. Simulation with a 50-mV amplitude gives the fundamental components amplitude equal to 89.9 mV (-20.9 dBV) and the spurious ones euql to 1.12 mV (-59.0 dBV), yielding to an IM_3 of -38.1 dB. For such values of IM_3, IP_3, (the input signal where fundamental components are equal to the spurious ones) can be estimated to -7 dBV.

Simulations show also that the total power dissipation is 3.4 mW.

IV. COLCLUSION

A new analog CMOS modulator topology working with 1.5-V power supply has been proposed. With a clock signal up to 200 MHz it can elaborates 150-mV of amplitude input signals with a compression point less than 1-dB while dissipating 3.4 mW. Moreover, the particular topology makes it useful for an integration in fully digital ICs.

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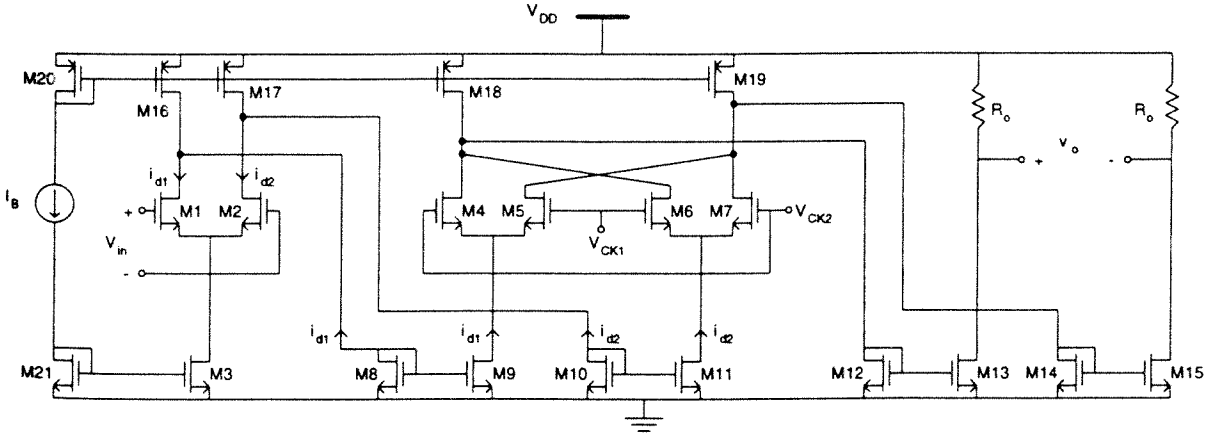

Fig. 1

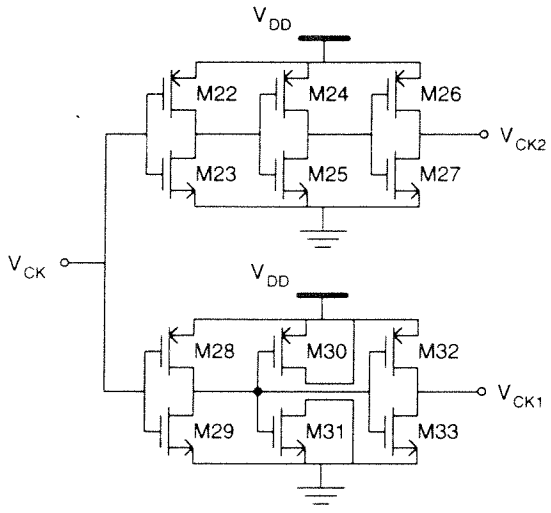

Fig. 2

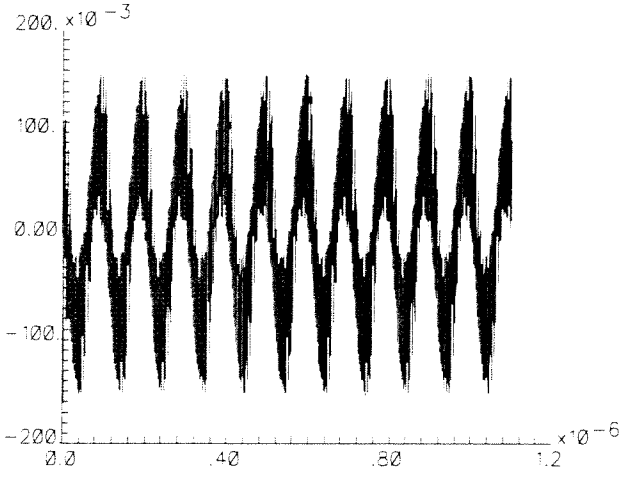

Fig. 3

Component	Value
M1, M2	100/1.2
M3	100/1.2
M4, M5, M6, M7	25/1.2
M8, M9, M10, M11	25/1.2
M12, M13, M14, M15	25/1.2
M16, M17, M18, M19	100/1.2
M20, M21	100/1.2
M22	225/1.2
M23	75/1.2
M24, M26	75/1.2
M25, M27	25/1.2
M28, M32	75/1.2
M29, M33	25/1.2
M30	90/1.2
M31	30/1.2
R_o	8 kΩ
I_B	200 µA

Tab. I

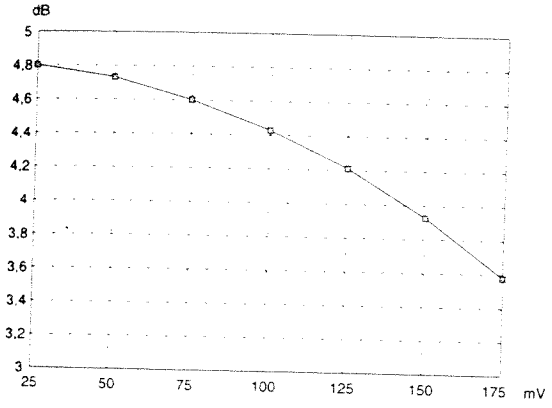
dB
5
4,8
4,6
4,4
4,2
4
3,8
3,6
3,4
3,2
3
25
50
75
100
125
150
175
mV

Fig. 4

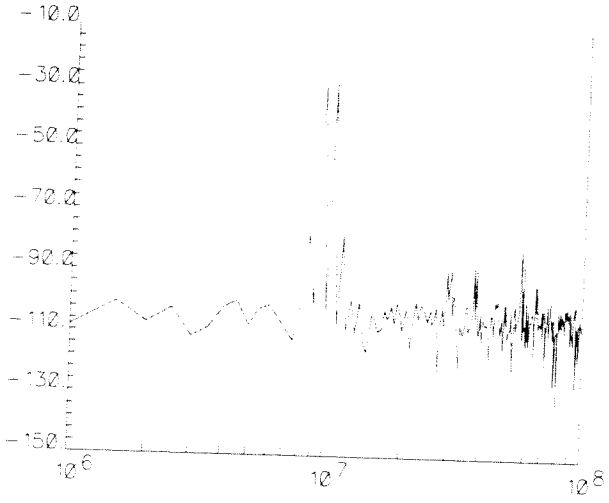
-10.0
-30.0
-50.0
-70.0
-90.0
-110
-130
-150
10^6
10^7
10^8

Fig. 5