

600 MHz Digitally Controlled BiCMOS Oscillator (DCO) for VLSI Signal Processing & Communication Applications

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Abstract

A 16-bit digitally controlled BiCMOS ring oscillator (DCO) is described. This BiCMOS DCO design provides improved frequency stability under thermal fluctuations compared to a CMOS DCO design presented in [1]. Simulations of a 5-stage DCO using 1 μ m BiCMOS process parameters achieved a controllable frequency range of 90 - 640 MHz with a linear/quasi-linear range of around 300MHz. Monotone frequency gain (frequency vs control-word transfer function) with fine stepping (tuning) in several KHz was verified. This augurs the prospect of accurate frequency lock in a BiCMOS all digital PLL (ADPLL) application in digital VLSI communication systems. Worstcase jitter due to digital control transitions at pathological control-word boundaries for the BiCMOS DCO was observed to be less than 50 ps, which is lower than that for the CMOS DCO.

1: Introduction

Recovering accurate timing and delay information in received signals from remote sources is an well-known problem in VLSI signal processing, information and communication systems. Voltage controlled oscillators (VCOs) and Phase-Locked-Loops (PLLs) have been the kernel prescriptive solutions to many such problems. Specifically, VCOs have been utilized in many high speed clock recovery systems.

With the growing trend of implementing major communication electronics in digital VLSI circuitry, development of precision digitally controllable VCOs (referred to as digitally controlled oscillators, DCOs) is of primary importance. In contrast to VCOs which employs an analog voltage level [2][3] to determine the oscillator frequency, DCOs uses a digital control-word to divide and step the inherently available frequency range.

Efforts in true digital frequency synthesis is quite recent as most known all-digital PLL systems (ADPLLs) usually require a high frequency clock source that constraints application in digital communication. Lately a CMOS ring oscillator DCO was reported in [1]. In an n-bit DCO, there are n binary weighted (e.g., using binary scaled MOSFET device aspect ratios) input signals to the DCO, and by incrementing or decrementing the DCO control-word (resident in a DCO control register) the phase and the frequency of the DCO is modulated [1].

Reported work on BiCMOS DCOs (the natural next step) has so far been rare. Considering the increasing use of BiCMOS circuitry which combines the advantages of complementary MOS & bipolar device behavior, this paper presents a 16-bit BiCMOS DCO that uses such duality in device attributes in enhancing frequency stability under conditions of thermal fluctuations.

In a pure CMOS design the DCO's frequency is considerably susceptible to mobility (μ_n, μ_p) degradation due to increasing temperature [6]. The MOS strong inversion channel current being a majority carrier drift current ($n\mu_n qE, p\mu_p qE$) is directly affected by the mobility variation with temperature. On the other hand, forward active(or saturation) bipolar currents being mostly minority carrier diffusion currents ($D_n \frac{dn_p}{dx}, D_p \frac{dp_n}{dx}$), the effect of mobility variation with temperature is less pronounced [7]. In a VLSI implementation whereby the DCO is a part of a high performance micro-processor as in [1][5], the operating temperature can fluctuate considerably thereby inducing a corresponding drift in the DCO's frequency. Thermal stability of the CMOS DCO's frequency was not addressed/investigated by the authors in [1]. The proposed BiCMOS DCO is thus aimed at providing higher overall system performance (under similar

applications as in [1]) through accurate frequency lock and stability under conditions of thermal stress/fluctuations.

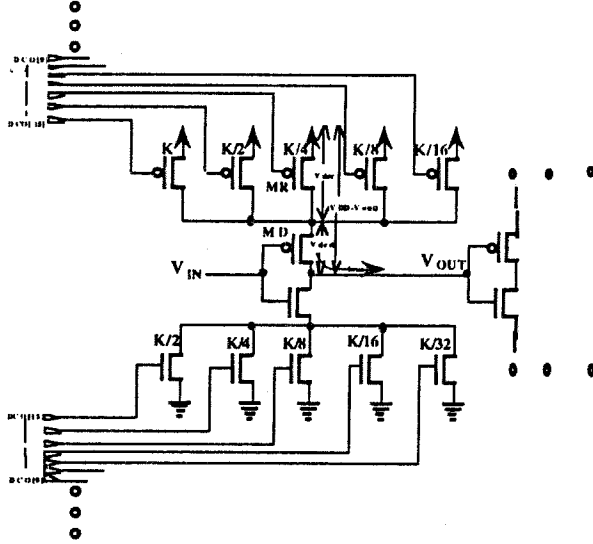


Fig. 1 : A fundamental CMOS DCO cell(stage) with source degeneration at the power supply rails, K being the largest device aspect ratio.

2: BiCMOS DCO Design

The dominant VCO architecture consists of an odd-numbered ring of inverting gain stages connected back on itself [2]. The variation in the frequency of the ring is obtained by varying the time-rate (the slew-rate in case of large amplitude oscillations) of the voltage change (charging/discharging) at the ring nodes. One well-known way of effecting this, is setting and controlling the pull-up/pull-down delay-time per inverting gain stage. The authors in [1] used a similar scheme to implement digital frequency control (through digital delay-time control). MOSFET triode regime resistors (with binary weighted aspect ratios) are introduced as source degeneration at the VDD & VSS rails of the CMOS inverter gain stage. Variation of the source degeneration produces a monotone variation in the delay-time per ring-stage and hence the oscillation frequency of the ring. The constituent DCO cell with control bits developed in [1] is displayed in Fig. 1.

In order to improve the stability of the load current (and hence the pullup/pulldown delay-time) in this configuration, we replaced the CMOS inverter with a BiCMOS inverting gain stage (similar to a BiCMOS totem-pole output gain stage) as shown in Fig. 2. The difference in the stability of the output current under thermal fluctuations is analysed as follows.

Considering the BiCMOS stage (Fig. 2) first, we assume that the temperature rises slightly from T to $T + \Delta T$ at time t . The consequent decrease in mobility, $\Delta\mu$ (due to scattering by lattice vibrations (phonon collisions) [6]) tends to substantially decrease the drain current I_d (the majority carrier drift current) through the triode regime PMOS resistor MR. However, the slight increase in temperature also causes the space charge regions in the bipolar device (the depletion regions at the junctions) to shrink marginally and hence the voltage V_{ce} of the NPN QD to reduce slightly [4] (as shown in Fig. 3(a)). This results in only a small *early effect* related decrease in the collector current I_c (the minority carrier diffusion current). The slight drop in V_{ce} is transmitted to the channel of the series connected PMOS device MR (in the form of a slight increase in the drain-to-source voltage across the MOSFET resistor) since voltage across the stage output (MOSFET gate input capacitive load) cannot change instantaneously. The slight increase in V_{ds} (ΔV_{ds}) offsets (to some extent) the effect of mobility degradation in the PMOS resistor device MR (V_{ds} being very small for triode region operation). i.e., using standard notations we have,

$$I_d(T) \cong \mu C_{ox} \frac{W}{L} (V_{gs} - V_{Th}) V_{ds}$$

$$I_d(T + \Delta T) \cong (\mu - \Delta\mu) C_{ox} \frac{W}{L} (V_{gs} - V_{Th}) (V_{ds} + \Delta V_{ds})$$

and, $I_d(T) \cong I_d(T + \Delta T)$

This arrests the large depreciation of the output load charging current (I_{out}) with temperature (i.e., $I_d(T) = I_c(T) = I_{out}(T) \cong I_d(T + \Delta T) = I_c(T + \Delta T) = I_{out}(T + \Delta T)$). This complementary behavior between the NPN device & the PMOS triode regime device can be termed as Junction-to-channel thermal "feedback" voltage compensation and is expressed graphically in Fig. 3(a). On the other hand, in the case of a CMOS stage (Fig. 1), there is no complementary interaction ("feedback") between the PMOS triode regime resistor MR and the PMOS driver device MD, as the current for both the devices (both being majority carrier drift currents) is effected equally by the mobility degradation, resulting in a net reduction in the output current (as shown in Fig. 3(b)).

It is interesting to note from Fig. 3, that thermal stress ΔT at time t causes the operating point(I, V) to traverse in an almost horizontal direction for the BiCMOS DCO (almost constant current), compared to an almost vertically down trajectory for the CMOS DCO (almost constant voltage).

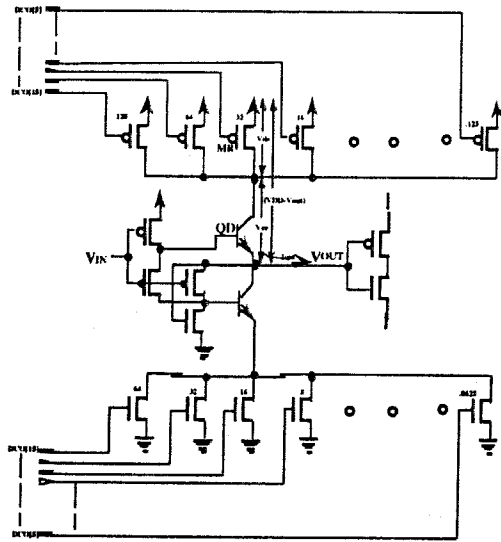
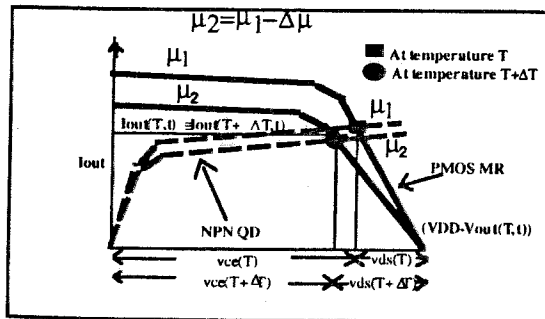
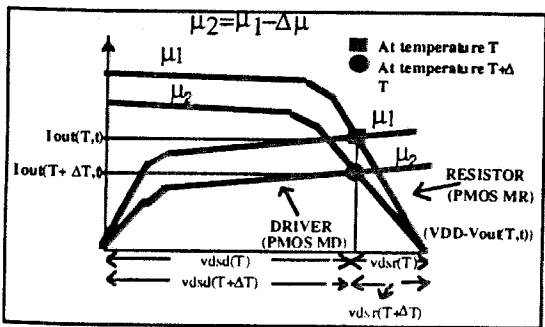


Fig. 2 : A fundamental BiCMOS DCO cell(stage) with 11 bit control vector (MOSFET aspect ratios are as shown with lower significant control bit MOSFETs being long channel devices).



(a)



(b)

Fig. 3 : Graphical illustration of the effect of small temperature fluctuations on DCO output current where (a) the higher stability of the output driving current in a BiCMOS DCO stage compared to (b) the considerable depreciation of the CMOS DCO stage output current due to mobility degradation.

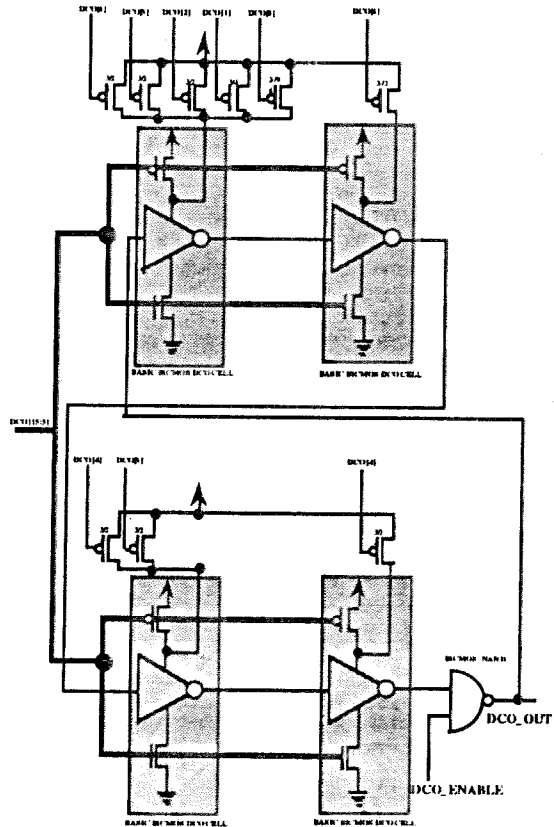


Fig. 4 : A complete 5-stage BiCMOS DCO (including a BiCMOS NAND enable stage) with 16 control bits (control-word) from the DCO control-word register CWR.

3: Simulation Results

Extensive simulations were carried out using standard $1\mu\text{m}$ BiCMOS ($V_{TH} \cong \pm 0.8\text{V}$) process parameters and a power supply of 5V. In the fundamental BiCMOS DCO cell of Fig. 2, the control devices consist of 11 CMOS pairs to obtain the first 11 control bits. The largest PMOS resistor device has an aspect ratio of 128, with its NMOS counterpart having half the size (to account for the higher mobility). The rest of the MOSFET triode regime devices have the aspect ratios as shown to achieve a binary weighted control. Long channel devices were used for lower significant control bits. The DCO control-word is resident in a 16-bit parallel loadable control-word register CWR. Fig. 4 displays the complete diagram of a 5-stage BiCMOS DCO which includes a BiCMOS NAND enable stage. Fig. 4 also shows how the remaining five control bits were achieved by utilizing technique explained in [1].

Exhaustive simulations were carried out to prove the superiority of the BiCMOS DCO structure.

Fig. 5(a) shows the effect of junction-to-channel thermal "feedback" voltage compensation. The voltage across the channel of the PMOS triode regime resistor MR is found to adjust with temperature variation during the greater part of a pull-up cycle (average values of Vds being .378V @ 0°C, .452V @ 50°C and .515V @ 100°C) thereby preventing large thermal fluctuation of the pull-up current Id (average values of the drain current Id being 5.06mA @ 0°C, 4.99mA @ 50°C and 4.97mA @ 100°C). Whereas, Fig 5(b) clearly shows the depreciation of the output current Id with temperature during a pull-up cycle for the CMOS DCO, with the drain-to-source voltage Vds remaining almost unchanged.

Fig. 6 shows the approximate thermal sensitivity of the BiCMOS DCO compared to the CMOS DCO for a temperature range in which lattice scattering (phonon scattering) is the dominant mechanism of mobility degradation. The average temperature sensitivity of the BiCMOS DCO was found to be $\cong 1,800$ ppm/°C compared to $\cong 4,800$ ppm/°C for the CMOS DCO.

This is a significant improvement considering that no additional thermal compensation circuitry has been used. The drift of the oscillator period with increasing temperature as shown in Fig. 6, is thus more pronounced for the CMOS compared to the BiCMOS DCO. The effect of mobility degradation (due to phonon scattering) in the CMOS case is thus clearly evident. Fig. 7 (a) - (d) shows several simulated DCO output frequencies while Fig. 8 shows the monotone frequency - control-word characteristic for the wide control range of the BiCMOS DCO. The 16-bit binary control vector provides a controllable DCO frequency range of 90-640 MHz (with a linear/quasi-linear range of around 300 MHz) using the 1µm BiCMOS process parameters.

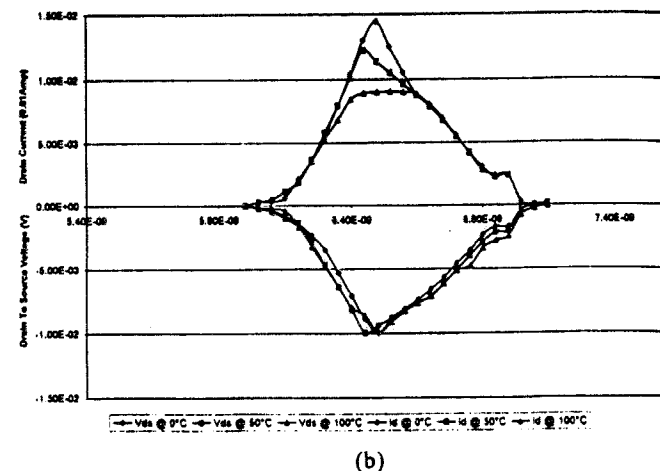
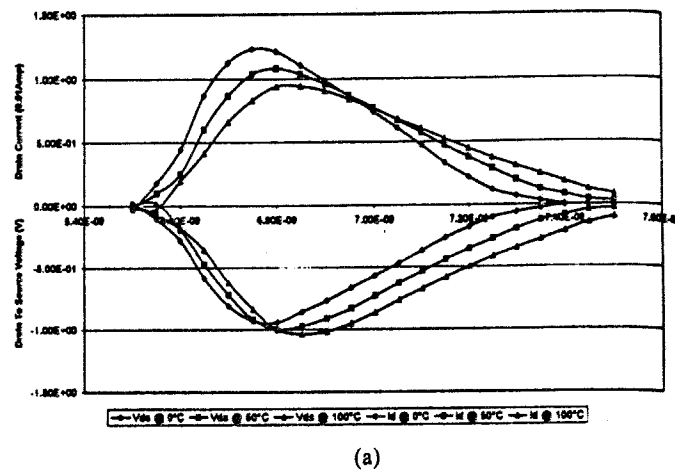


Fig. 5 : (a) The effect of Junction-to-channel thermal "feedback" compensation in a BiCMOS DCO cell(stage) (b)The depreciation of drain current with temperature for a CMOS DCO cell(stage).

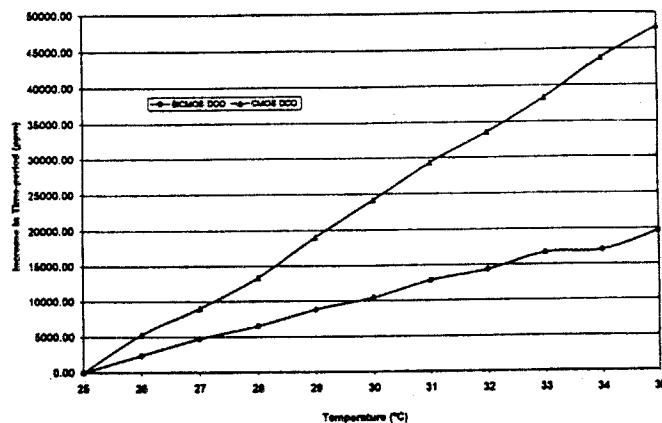
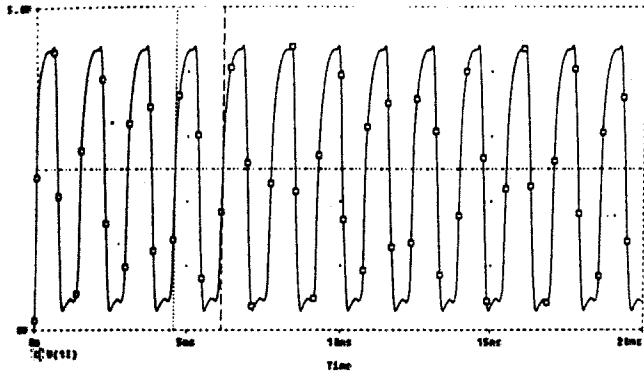
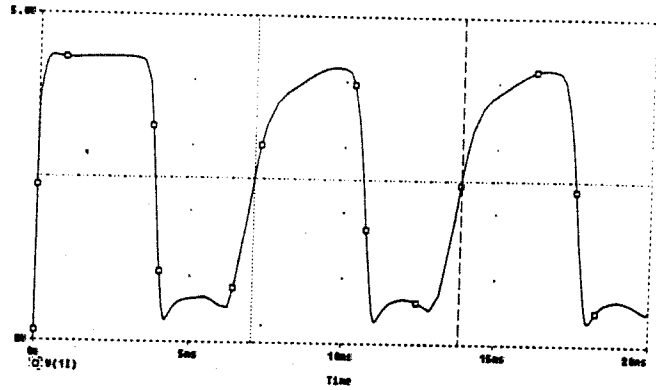


Fig. 6 : The approximate temperature sensitivity of the BiCMOS DCO compared to that for the CMOS DCO.



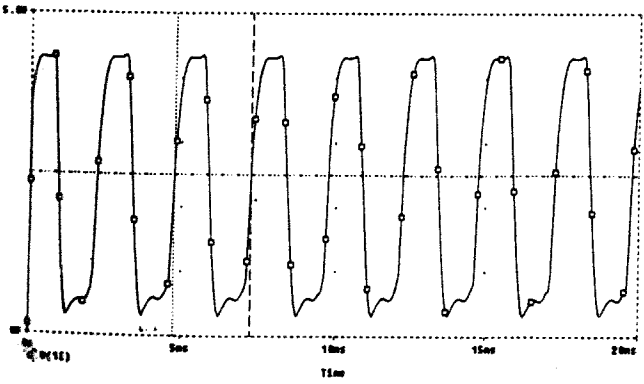
7(a)

CWR=FFFH, DCO FREQUENCY=640.984MHz



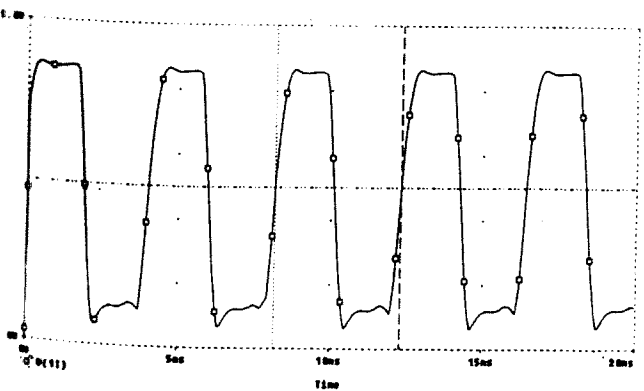
7(d)

CWR=01FFH, DCO FREQUENCY=146.486MHz



7(b)

CWR=1FFFH, DCO FREQUENCY=400.769MHz



7(c)

CWR=07FFH, DCO FREQUENCY=241.803MHz

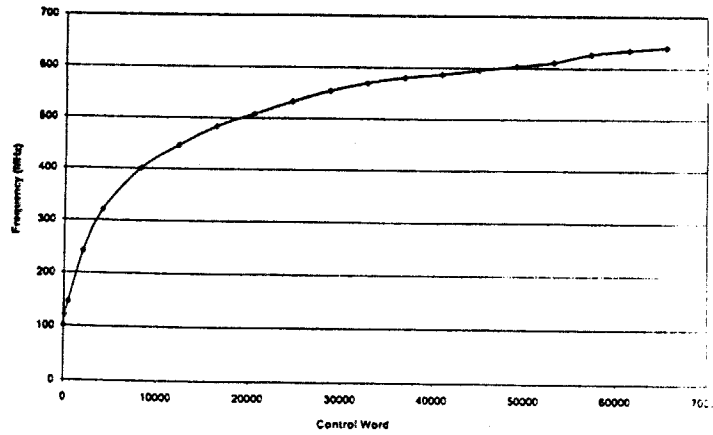


Fig. 8 : Frequency gain characteristic of the BiCMOS DCO .

4: Conclusion

A BiCMOS DCO for digital VLSI communication system with improved stability under thermal fluctuations has been designed. The duality in MOS & bipolar device attributes contributes to this improved stability. The DCO has a large frequency range that can be set (controlled) by a 16-bit control vector.

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