Power Reducing Techniques for Clocked CMOS PLAs

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Abstract

Power saving techniques for CMOS Programmable Logic Arrays (PLAs) are discussed. Two new techniques are introduced, an AND-plane pulse generator, and Wired-OR CMOS. Power reduction in excess of 75% over Pseudo-NMOS techniques and 50% over some clocked PLA techniques is possible.

Keywords: Pulse generator, Wired-OR CMOS, Single-phase clock, Self-timed logic.

1 Introduction

Power management has become an important topic for embedded-systems designers. The sources of power consumption in CMOS chips have been well documented[1]. Vdd voltage is the most important factor, but within a particular technology, the designer must work with a given Vdd value. Beyond that worthwhile savings can be achieved by paying careful attention to design techniques.

A recent analysis of the ARM7TDMI embedded processor, reveals that its Arithmetic/Logic Unit, Programmable Logic Arrays, and register bank are the dominant contributors to power consumption[2]. In this paper effective power management features for clocked PLAs are presented.

2 Current Practice in PLA design

PLAs can be designed using a variety of implementation techniques [3, 4, 5]. Both speed and space reduction is obtained by the NOR-NOR logic style, using Pseudo-NMOS (PN) techniques for AND-plane and OR-plane pull-up. Unfortunately, PN also uses more power than either dynamic PLAs, or synthesized logic gates.

A good start on power reduction is to clock the PN pull-ups so that DC current only flows during half of the clock cycle. There are a variety of ways to do this. Blair proposes to use a domino style clocked OR-plane with a clocked PN AND-plane [4]. Fig. 1 shows the timing for this method. Note that PN DC power is consumed for the hold half-cycle in the AND-plane. Also, this technique always drives the AND-OR-plane outputs to zero during their pre-discharge/pre-charge half cycles.

3 A Low-Power PLA Clocking Scheme

One of the ways to save power in a logic block is to reduce the number of signal transitions [6]. Precharging schemes force all signals to either high or low values, sometimes unnecessarily. One of the advantages of PN for both AND- and OR-planes is that when input signals change, only the required AND/OR output signals change.

Fig. 2 presents a clocking scheme which permits PN logic style for AND- and OR-planes, as well as supporting considerably reduced power consumption. The OR-plane PullUp (PU) pulse is easy to generate as a self-timed pulse from either the falling edge of the system clock, or the rising edge of the AND-plane PU clock. However, the AND-plane PU clock should have its falling edge delayed as much as possible from the rising edge of the system clock (see *maximize*).

Fig. 3 shows a circuit schematic which can be used to generate a well behaved delayed AND-plane PU pulse, apz. A typical Hspice simulation is shown in Fig. 4 with the transistor sizes indicated in Fig. 3 (0.8 micron CMOS process parameters were used). Schematic transistors P2,P3 are used to control the pulse delay. For a given length of P2, the pulse delay is linearly dependent upon the length of P3. The length of N3 also contributes to the pulse delay. It would be quite straightforward to automate the selection of this for a particular clock period. A conservative choice would be to set the delay for a quarter of the clock period. P4 and N3 should be sized to give apz reasonable rise/fall times, according to the load in the AND-plane (a load corresponding to about 10 minterms was used).

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A self-timed OR-plane pulse generator is shown in Fig. 5. In this circuit, the length of P2 can be adjusted to control the pulse width of opz. Alternatively, the load between P2 and N3 can be made equal to the worst case load in the OR-plane.

Undesirable AND-plane power consumption is caused by false Minterms during the PN part of the clock cycle. The new delayed AND-pulse scheme can conservatively reduce this to a quarter clock cycle. Furthermore, the clocking strategy of Fig. 2 does not require any signals to change unnecessarily. This will more than offset the DC power used by the short self-timed OR-plane pulse. Another advantage of delaying the AND-pulse is that rising-edge clocked flip-flop outputs have time to stabilize before the PLA uses any power.

Overall, the new clocking scheme can reduce PLA power consumption by over 75% in comparison to unclocked PN approaches, and by 50% in comparison to other clocked PLA designs (e.g. Blair's method). Some layout area is needed for the pulse circuitry, but this can be tucked into the corners of a PN PLA layout which typically has unused space due to the protrusion of the PMOS pull-ups.

4 Wired-OR CMOS

Suppose that a 6-input NOR gate is required. The pull-up of such a gate may be very slow compared with the pull-down. It is difficult (or impossible) to scale it effectively. However, by breaking the device up into 2 3-input NOR gates and wire-ORing the outputs together, we get 2 parallel pull-up paths, as shown in Fig. 6. This structure uses DC power the same way that a PN device does. The obvious disadvantage over PN is that there are nearly twice as many transistors. This disadvantage is rapidly diminishing in importance as deep submicron processes become available.

Wired-OR CMOS (WOC) can use considerably less power than PN. Since there are 2 (or more, but we will restrict discussion to 2) pull-up paths one can choose to make each path use half of the DC power that is used by a similar PN device, while pull-up performance remains comparable to PN (each path will be slightly degraded, but this can be compensated for as a design parameter). This half-power case is close to the worst case scenario.

Expected power is much less due to the pair of 3-input gates. For 6 inputs there are 64 input combinations, but only 10 of them cause DC power consumption (5 ways for each of abc, def to pull down while the other pulls up). If, as is often the case with state machines, the designer knows which combinations of inputs are most frequent, they can be applied to the WOC gate in such a way as to minimize power consumption.

WOC gates are not intended for a general replacement of standard CMOS gates. Any place a PN circuit is used, the WOC technique could be considered as an alternative. In particular, they can be used in the OR-plane of a small PLA. The main advantage of this is that no OR-plane clocking is required.

5 Conclusion

PLAs are still being used in commercial chips, partly because of their speed, and partly because they use less area than synthesized logic [2]. However, in the case of the ARM7TDMI, power consumption in synthesized logic was found to be as little as 50% of the PLA power consumption.

We have presented techniques for reducing PLA power consumption to levels that are competitive with synthesized logic. Further studies should be performed to compare synthesized logic with PLA equivalents.

References

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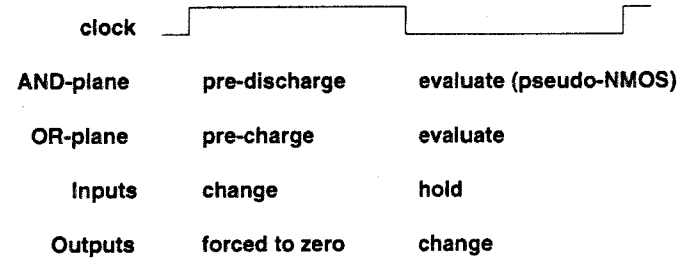

Figure 1: Timing characteristics of Blair's PLA [4].

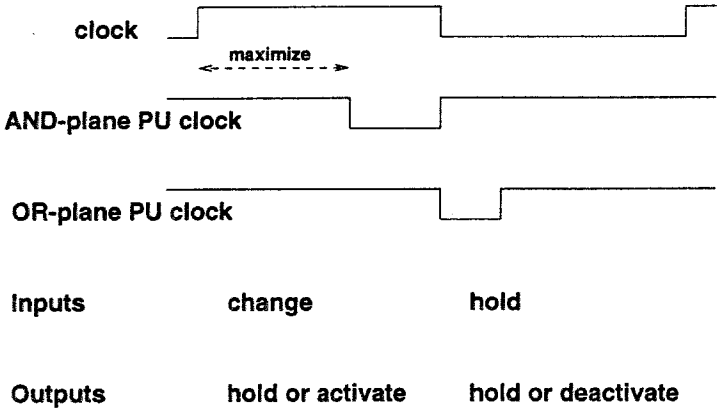

Figure 2: Improved PLA timing.

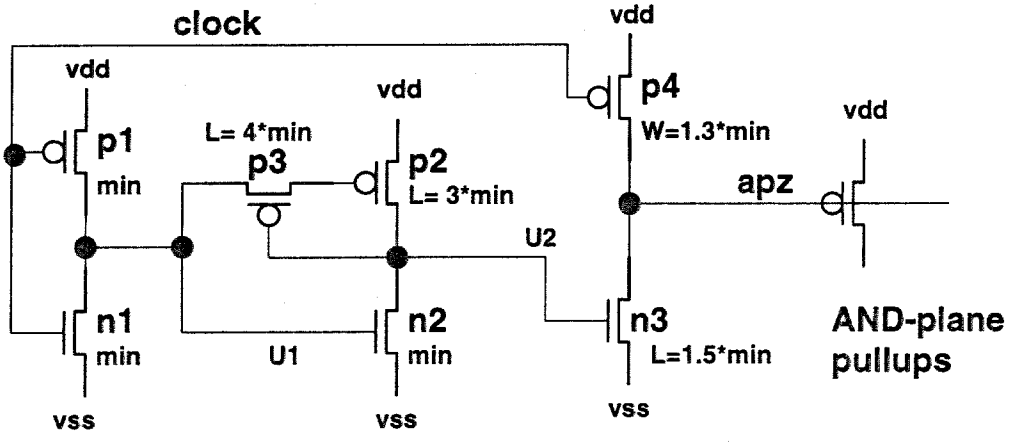

Figure 3: Schematic of delayed AND-plane pulse generator.

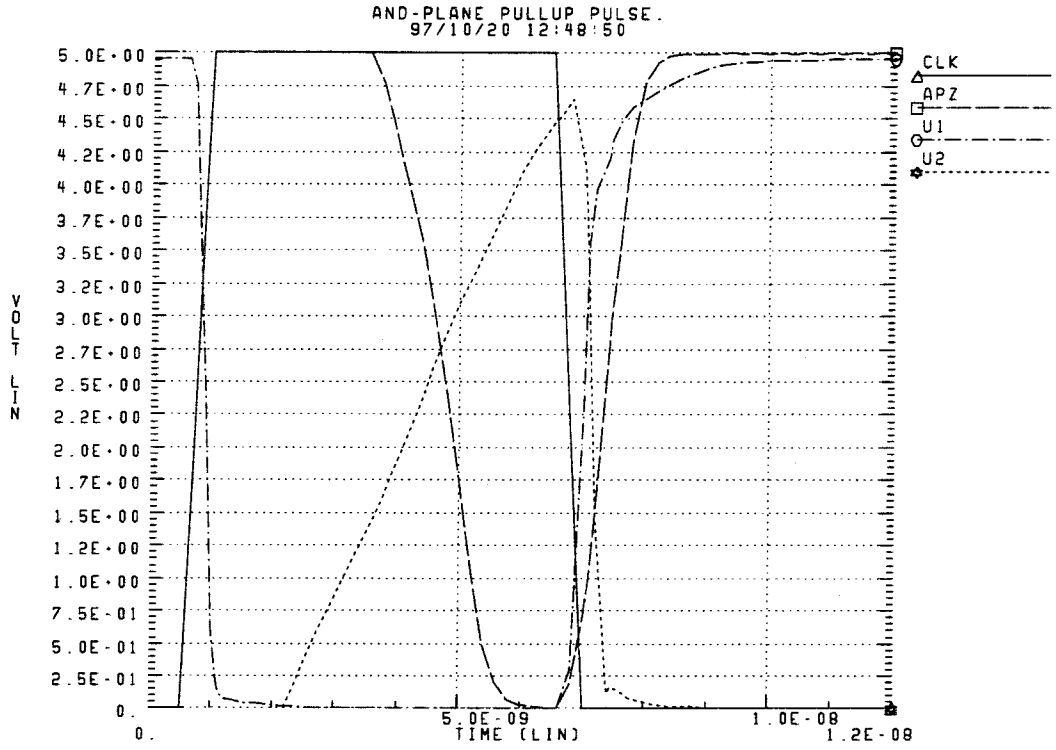

Figure 4: A typical delayed AND-plane pulse simulation.

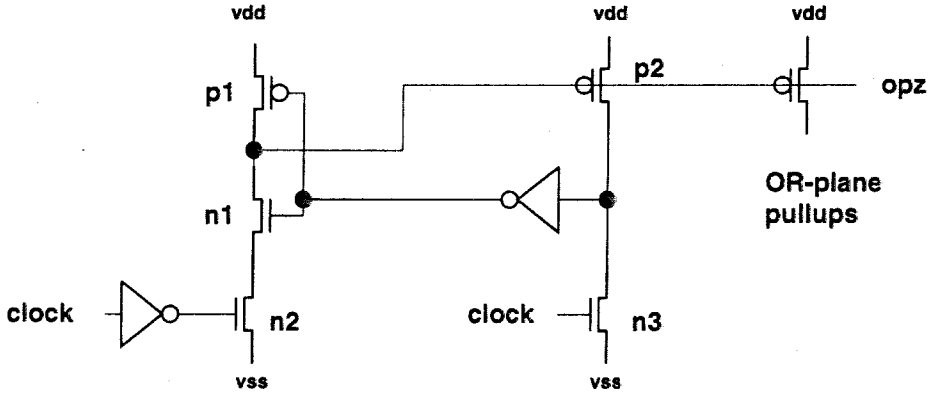

Figure 5: Schematic of a possible self-timed OR-plane PU pulse generator.

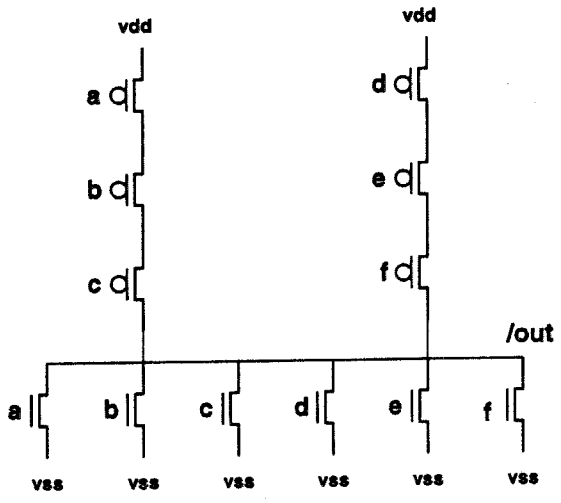

Figure 6: Schematic of a 6-input Wired-OR CMOS gate.