A Low Power 50 MHz FFT Processor With Cyclic Extension and Shaping Filter

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Abstract- This paper presents the architecture, design and implementation of a 16 point FFT processor for a high speed Wireless Local Area Network. The 110,000-transistor chip is implemented in 0.6μm TLM CMOS, operates worst case at 50 MHz at a supply voltage of 2.5 volts, and consumes 80 mW.

I. INTRODUCTION

This paper describes a structured custom version of a 50 MHz FFT processor that is central to a Discrete Multi-Tone (DMT) modem being implemented at Macquarie. This chip also represents the first result of a design flow that has been expressly created for the rapid design of high performance DSP architectures from Verilog. The chip features the following:

- 16 point FFT with cyclic extension
- 9 bit imaginary and real data
- 50 Mbs throughput
- 16 point frequency shaping filter
- 2.5 V operation

II. SYSTEM OVERVIEW

This chip implements a 16-point FFT which is the dominant computational block in a Discrete-Multitone modem. The chip architecture is shown in Figure 1. It comprises an FFT block, a 16 tap filter and a cyclic extension module,

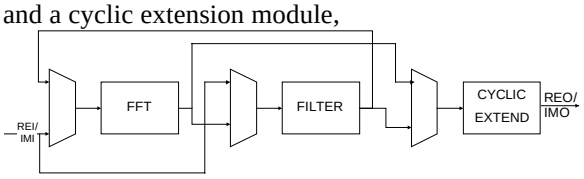

Figure 1. FFT Chip Architecture

III. CHIP ARCHITECTURE

The FFT module architecture is shown in Figure 2.

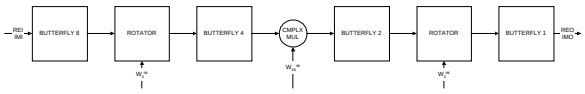

Figure 2. FFT Module Architecture

The algorithm used in this chip follows that used in earlier FFT chips designed by the CSIRO [3][4][5] and was originally described by Despain [6]. The 16 point transform is decomposed into two sets of 4-point transforms separated by a phase rotation of W_{16}^{nk}, which are further decomposed into 2-point transforms separated by phase rotations of W_4^{nk}. This reduces the number of complex multipliers to one, the 90° phase rotators being relatively straightforward to implement.

IV. DESIGN METHODOLOGY

The FFT chip was implemented using a new, high productivity design flow that permits the creation of high performance layouts automatically from a Verilog structural netlist [7][8][9].
This flow based on CADENCE tools and custom software written at Macquarie has the following key points:

- The CADENCE SmartPath tool allows automatic generation of high performance, high density and low power datapaths from the Verilog design level (and include synthesized control logic).
- Extensive scripts were written to automate the design flow.
- The MacPisces standard cell generation and characterization system (written at Macquarie) allows the fully automatic generation and characterization of standard cells in any CMOS process.

The generation of a new characterized library in a new CMOS technology takes roughly four hours. The original design of the FFT chip took about three months with an average of 2.5 people. The generation of a complete new iteration of the FFT chip (assuming a logic change) takes about 2 hours.

V. IMPLEMENTATION

The chip was implemented in the HP14 0.6µm three level metal CMOS process through the MOSIS service. The core area is 3mm by 3mm with an overall chip size of 3.5mm by 3.5mm. The die contains 110,000 transistors. The chip is packaged in a 64-pin ceramic PGA. Clocking is via a single level of buffering with clock buffers on all datapath registers.

The chip dissipates 80mW operating at 50MHz and 2.45 volts. As this represents one of the two significant computational blocks in the decoder, we can safely say that at 50 MHz and in a process that is a generation behind current CMOS 0.35µm technology, the power consumption of the DSP portion of a multitone modem is relatively small. This is much less than an equivalent equalizer based strategy.

VI. CONCLUSIONS

We have presented the architecture and design of a low power 50 MHz FFT chip for a 50 Mbs WLAN modem. The chip was fabricated and was fully functional at rated speed at 2.5 volts. This chip served to validate and calibrate a new design methodology which enables the rapid capture of high performance digital blocks and the automated design of small, low power layouts by people who are not primarily chip designers.

VII ACKNOWLEDGEMENTS

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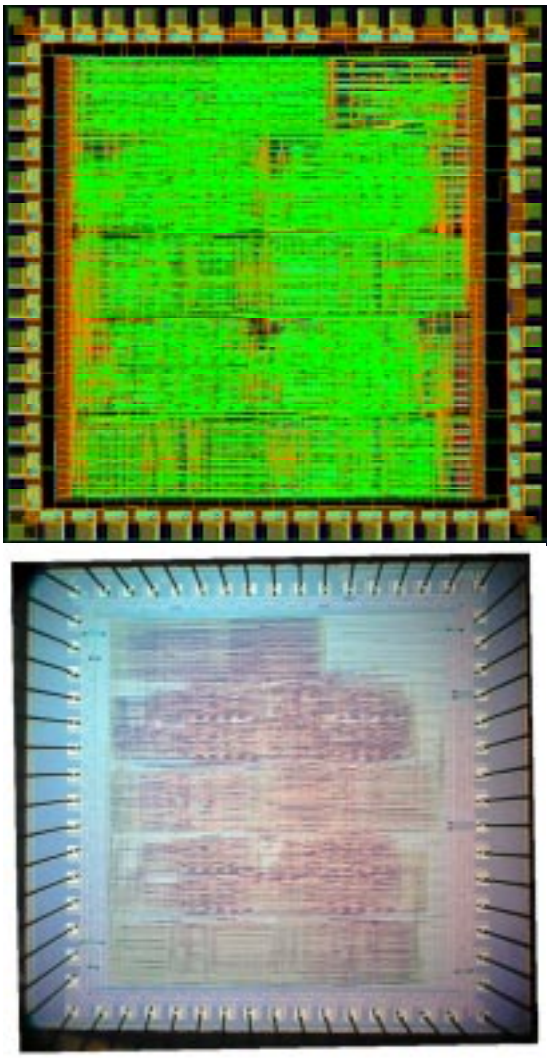

Figure 5. FFT Chip Plot and Photograph