ANALOGUE LSI RF SWITCH AND BEAMFORMING MATRIXES FOR COMMUNICATIONS SATELLITES

Markku Åberg, Anssi Leppänen, Arto Rantala, Jouko Marjonen
Technical Research Centre of Finland, Electronics, IC Group
P.O.Box 11012, FIN- 02044 VTT, Finland
email: markku.aberg@vtt.fi

ABSTRACT

Communications satellites use steerable antenna arrays for their communication links. These arrays need multi channel signal routing circuits up to several tens of channels. Traditionally this circuitry has been realized with hybrid technology. This has resulted to tens of Watts in power consumption and several kilograms of payload weight. In this paper we describe monolithic integrated switch and vector modulator matrixes for signal routing and beamforming, operating in the 160 MHz IF range. These 12 - 16 I/O channel LSI level analogue circuits reduce power consumption of the satellite beamforming circuitry to a few watts and weight to less than one kilogram. The power consumption per matrix node is 10 - 20 mW compared to the 100 - 500 mW consumption in the hybrid solutions.

INTRODUCTION

System parameters applicable to Personal Communication Satellite systems drive towards solutions with larger number of beams in the coverage area, primarily due to low antenna gain and limited transmission power at the user personal portable terminal. There are several possible architectures available [1], depending on the orbit choice and other system parameters: fully analog, fully digital, and hybrid with digital switching and signal processing but analog beamforming. The circuits in this paper are intended for the fully analog system. The block diagram of the system architecture called “Analogue Repeater Architecture” is displayed in Fig. 1 [1].

Traditionally switch matrixes and beam formers (vector modulators) have been manufactured with hybrid solutions [2,3,4]. The drawback of these solutions have been large power consumption and weight. The power consumption can be as high as 100 - 500 mW per matrix node, and the weight of the unit can be several kilograms. Therefore we studied the possibility of rising the integration level from a hybrid to a monolithic circuit solution, to reduce the power consumption and weight. The object of the design is an IF range narrow band (160/30 MHz) analog crosspoint switch or vector modulator matrix. The packages available restricted the size of the circuit to 16 input and output (I/O) channels in the switch matrix and 12 I/O channels in the vector modulator matrix. The maximum specified power consumption is 2 W for the switch and 3 W for the vector modulator, and minimum isolation 35 dB.

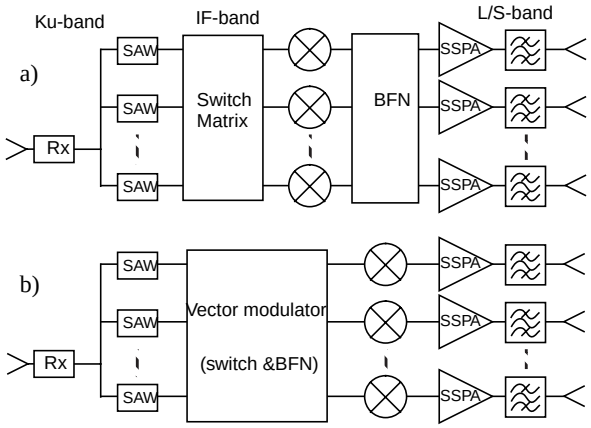

Figure 1. Block diagram of the “Analogue Repeater Architecture”; beamforming in: a) rf-region, b) if-region.

The selected technology was AMS (Austrian Micro Systems) 1.2 and 0.8 µm BiCMOS processes. The I/O signal demands; input from -20 to -10 dBm, output maximum 0 dBm, and low insertion loss demands (<3 dB) made the power economy as one of the most critical aspects in the design. Another difficulty was to keep the effect of switching configuration on insertion loss and phase variation low.

CIRCUIT DESIGN

A diode-transistor coupled type switch topology was chosen because of the low power consumption. The other alternative; differential pair switch, would have double bias current and power consumption, if the input transistor transconductance is biased to the same operating point. Except power consumption, the electrical performance of this type of switch was found to be equal with the differential pair switch topology. A differential pair would have better power supply rejection ratio, thus reducing the cross-coupling via supply lines, but the main source of cross-coupling is the output amplifier, which is single-ended in any case.The combined basic schematic of the circuit is in Fig. 2.

The input bias circuit is based on a voltage reference double current mirror. A bandgap circuit has been used as the voltage reference for minimizing the temperature dependence. The mirror is of emitter follower augmented (EFA) type [5]. This

type of mirror is very suitable for this kind of application with as many as 16 outputs for one input, because of its higher effective current amplification β. The output current drop of the EFA mirror is only 0.2% compared to 17% of a basic mirror with 16 outputs.

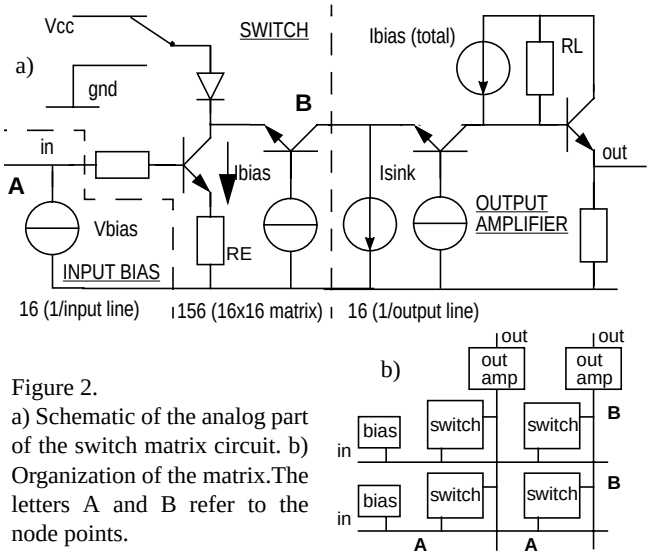

Figure 2.
a) Schematic of the analog part of the switch matrix circuit. b) Organization of the matrix.The letters A and B refer to the node points.

The matrix switch element is a diode coupled switch, Fig. 2. In off-state the diode is connected to supply voltage, reverse biasing the switch output transistor base-emitter junction. In on-state the diode is reverse biased and the output transistor is forward biased. The same bias current runs all the time through the switch input transistor, either through the switch diode or through the output transistor from the output amplifier dc bias source. Hence the power consumption of the switch matrix is constant and independent of the switching state. The bias current level is about 300 µA. Theoretically this circuit topology gives a very high isolation. However, as a single sided structure, it is sensitive to voltage supply noise, which can be very profound in this kind of very large circuit. In off-state the power supply is coupled with little attenuation via the forward biased diode to the emitter of the switch output transistor. Even when this is in off-state, the high output capacitance C_{oss} of the reverse biased transistor couples some noise to the output. To prevent this a 7 pF grounding capacitor has been added to the anode of the switching diode.

The output amplifier has a common base input stage and an emitter follower as output, Fig. 2. To minimize the power consumption, the bias current of the resistor RL is directed for biasing the switch elements, too. A parallel dc current source (Ibias, Fig. 2), realized with a PMOS transistor, has been added for keeping the amplification and dynamics high enough with 5 V supply voltage. Because of the large dependence of the PMOS capacitance and thereafter in the output phase and amplitude on the current, a pre-biasing current sink (Isink, Fig. 2), was added to reduce the load (switch biasing) current variation from 16:1 to 4:1. The current of Isink is inversely proportional to the number of on-switches.

The goal was voltage amplification Vout/Vin = 1. Theoretical calculations are according to Equation 1

$$V_{out} = V_{in} \cdot gm \cdot RL/(1 + gm \cdot R_E) \quad (1)$$

Where RE is the switch input transistor emitter degradation resistor, Figure 3. The transconductance gm of QS1 is I_C/V_T = 12mS with 300 µA bias current. This gives, according to Eq. 1, a value of RL ≈ 500 Ω for unit voltage amplification. In the real matrix the parasitic capacitance of the long lines and other switches reduce the signal so much that the value of RL was set to 1.5 kΩ to compensate the losses.

Encouraged by the good results with the switch matrix we decided to increase the integration level and add vector modulation capability on the matrix nodes. For beamsteering purpose the goal of the design is to achieve a full vector (360°) phase control and an amplitude control in the order of 15 dB. Phase shift of the signal is controlled digitally and amplitude control has been done with an analog control. The power consumption in one steering element has to be under 10 mW. Thus the total power consumption in whole 16 x16 matrix would be about 2 W (for the modulators, without DACs and control logic). The challenge in this design is to achieve an accurate phase control over the full frequency band. Because of the large layout area of the whole matrix, one element has to be as small as possible. Therefore several topologies were studied: single ended, differential and ladder network. The principle of the final solution, ladder network, is briefly discussed in the following section. The ladder network, DACs and digital control are discussed in more detail in [6] and [7].

By using a single RC structure to shift the phase, it is not possible to reach even a decent accuracy, because of the process and the frequency variation. One way to reduce the influence of the process and the frequency variation is the two path serial ladder structure, Fig. 3. Signal is controlled by two path switch blocks, to have a specific phase value at the output. Phase can be shifted from 0° to 360° and the smallest step is determined by the shift of the last block. The upper path of the block is always the reference (virtual 0°) and the lower is set to a specific phase shift. Digital data is enough to control the system, because of the simple mosfet switch control. One bit is sufficient for each block, because switches in the parallel paths are always in opposite states.Amplitude is adjusted with a common base amplifier controlled by a DA-converter.

The principle of the ladder node is shown in Fig. 4. When the signal is splitted to the original and its inverse and then driven as shown, the result vector can have all values from the 0° to 180° (half circle). The length of the vector equals the radius of the half circle and thus the amplitude remains constant. Paral-

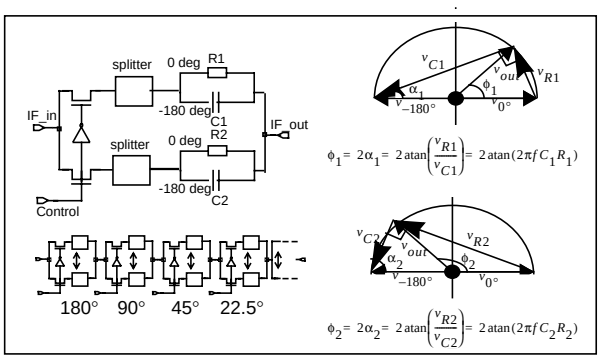

Figure 3. The principle of the ladder node (allpass filter).

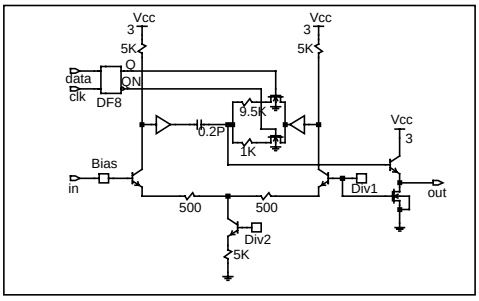

Figure 4. The design of the ladder node

lel block is needed to create a reference to ensure the accurate phase shift. The reference block is compensating the influences of the 30 MHz frequency band and the process tolerances. The best accuracy is achieved, when the result vectors are symmetrical in relation to the vertical axis. Amplitude levels at the output node will be the same regardless of the path, because of this unity gain (allpass) shifting technique.

The splitter in Fig. 3 could be realized with a pair of identical differential pairs, but this would be too area and power consuming. The design can be simplified by noting that both signal paths of the block are almost similar. By replacing the switches as shown in Fig. 4, it is possible to get rid of the other differential amplifier. The reference path consists now only of one resistor and thus the layout area and the power consumption are halved. By making the switch transistor wide enough, there will switch resistance process variation will have no effect on the phase shift accuracy. With this circuit it is possible to realize all except the 180° phase shift block, which is basically a standard inverting/non-inverting amplifier.

MEASUREMENTS

The main parameters measured on the matrix were: power consumption, phase linearity over bandwidth, insertion loss, isolation and cross-coupling over bandwidth and from port to port. Table 2 shows the insertion loss at the circuit output as a function of switch sate (SS) and supply voltage Vcc. Table 3 shows the phase variation over the band width and as a function of the switching state. The variation after the switching state comes from capacitance variation of the PMOS dc bias current source of the output amplifier, Fig. 2.

The biasing difference explains also the difference in phase variation over the bandwidth between different switching states. Table 4 shows the isolation (from input to output) and cross-coupling (from on to off-channel) as a function of the switch state. One can see that the isolation is a strong function of the switch state. Analyses show that this is due to the power supply line parasitic resistance and the package parasitic inductance. The power line parasitic are in the order of 0.5 - 2 Ω. The maximum ac current of 3.75 mA will generate a voltage ripple of 7.5 mV. The package inductance of one pin is in the order of 10 nH. It is high enough to block the ripple inside of the package and to couple it to other cells in the matrix. Multiple ground and power pins and double bondings were used in the package and the 16 output stages have each an own separate V_{cc} pin. The total number of pins is fixed in the package and therefore with a certain matrix size there is a lower limit of the inductance.

output (160 MHz), input -10 dBm	SS1 to 1	SS 1 to 16
x (V_{cc} 5V)	-1.54 dB	-3.24 dB
$\overline{x}$ (V_{cc} 4V)	-1.7 dB	-2.9 dB

Table 1. On-state output level

Phase variation in degrees	
145 - 175 MHz; switch state 1 to 1	12.5°
145 - 175 MHz; switch state 1 to 16	9.4°
Between switch states; max. at 160 MHz	4.6°

Table 2. Phase variation

Isolation (160 MHz) related to SS 1 to 1 output level		
Supply voltage V_{cc}	4 V	5 V
Switch state all off	39.9 dB	45.5 dB
Switch state 1/16 on	51.4 dB	34.8 dB
Switch state 15/16 on	22.0 dB	17.3 dB

Table 3. Isolation and cross-coupling as a function of on-state output channels.

Power consumption (W)	all off	all on
x (V_{cc} 4V)	1.64 W	1.12 W
$\overline{x}$ (V_{cc} 5V)	2.90 W	2.00 W

Table 4. Power consumption as a function of supply voltage and switching state.

An important factor in this kind of multi-channel matrix is the uniformity of the signal level in different channels. The output level variation over the output channels was measured with an input signal in one input switched to all 16 outputs. The worst case variation found to be 1.2 dB with -10 dBm 160 MHz input signal. Table 4 gives the power consumption. It should be independent of switch state, but again power line parasitics are causing some biasing errors, thus making difference between all on and all off state consumption. Fig. 5 shows wide band measurements from 10 MHz to 500 MHz. The specified oper-

ation bandwidth was 145 - 175 MHz, but Figs. 5 shows that the practical operating range could be much wider. The humps at 50 MHz and 350 MHz in the isolation come from package resonance. With other packaging solutions, e.g. flip chip mounting, a better isolation could be achieved.

Measurements of the first vector modulator prototype, where there is only one 45° block, shows that the basic idea of the shifting technique is working reasonable well. Phase shift accuracy and frequency response over the band is good. Troubles were occurring, when more shifting blocks were connected in series. Phase difference between the slopes should be again 45° but as the measured curves show, Fig. 6, relative accuracy over the band is lost: the phase slopes are steeper and more nonlinear. Behavior of the amplitude response is also a bit strange, when it is analyzed over broadband. This instability is probably due to parasitic components. By having a serial structure, all the different error components are multiplied with each other. The power consumption was well within specifications, maximum 2.6 W with V_{cc} 3 V and V_{dd} 5 V, of which the amplitude control DACs are taking about 1 W.

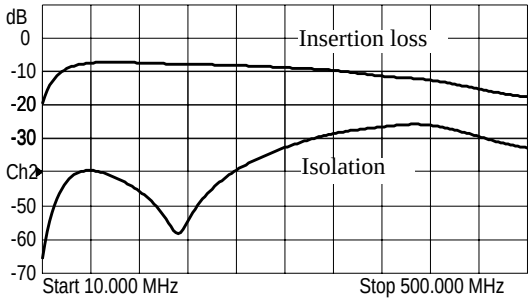

Figure 5. Insertion loss with 1 input to 1 output and isolation with all switches off, -10 dBm signal to one input.

CONCLUSIONS

One can conclude that the switch matrix circuit itself is in concordance with the requirements. The power consumption was 1.6 W or 6.3 mW per node with V_{cc} 4 V. Most of the performance limitations come from package; one can state that the circuit is now package limited, not silicon technology limited. The greatest reason for limitations is the package inductance, which can be 10 - 15 nH/pin. At 160 MHz this corresponds 10 - 15 Ω impedance. Because the pads in present packages must be located at the edges of the chip, there will be in addition a 5 Ω parasitic series resistance in the metallization lines, and a total of 20 Ω impedance from the active element "ground" to the real ground of the system.

The first prototype of the vector modulator showed that it is possible to design at IF range large matrixes with more complex functions than mere switching. In the serial architecture there was too large variation of phase difference over bandwidth. By drawing conclusions from the good results of the one block measurements, solution for this problem may be found from the parallel topology having only one amplifier stage as a phase splitter. The serial design had power consumption of 2.6 W or 10 mW per node. The new parallel design is expected to have slightly smaller consumption, 9 mW per node, which yields a total of 1.3 W for a 12 x 12 matrix.

ACKNOWLEDGEMENTS

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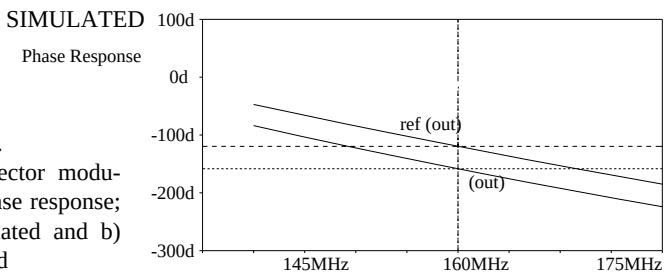

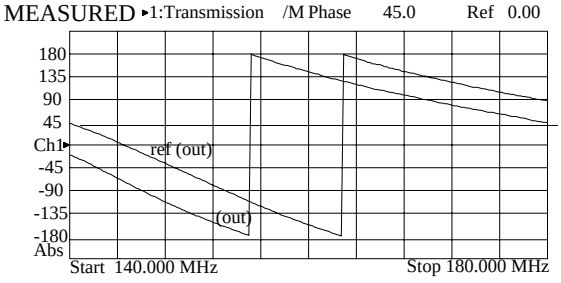

Figure 7.
Serial vector modulator phase response; a) simulated and b) measured