A Sequential Procedure for Average Power Analysis of Sequential Circuits *

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Abstract

A new statistical technique for average power estimation in sequential circuits is presented. Due to the feedback mechanism, conventional statistical procedures cannot be applied to infer the average power of sequential circuits. As a remedy, we propose a sequential procedure to determine an independence interval which is used to generate an independent and identically distributed (iid) power sample. A distribution-independent stopping criterion is applied to choose an appropriate convergent sample size. The proposed technique is applied to a set of sequential benchmark circuits and demonstrates high accuracy and efficiency.

I. Introduction

Power estimation problem in sequential circuits is much more complicated than in combinational circuits because of feedback loops. Unlike those at primary inputs, switching characteristics at latch inputs cannot be acquired without analysis of the embedded finite-state machine (FSM). The analysis of FSM poses a great impediment to accurate power estimation due to its exponential complexity with the number of latches.

In this paper we propose a statistical approach, as outlined in Fig. 1, to overcome this difficulty. In general, statistical mean estimation procedures require an iid sample, i.e., a random sample of mutually independent power data. However, in sequential circuits power dissipations in consecutive clock cycles are temporally correlated. Thus, special care has to be taken in collecting the sample power data for mean analysis. We propose a sequential procedure to dynamically determine a proper *independence interval* separated by which two sample power data can be treated as mutually independent. This procedure is based on three independence tests which examine with certain *significance* the hypothesis that a power sequence is independent. Using the independence interval, an iid power sample can be generated. Sample size is controlled by measuring the convergence of the average power estimate by a distribution-independent criterion developed previously [5]. Compared with previous approaches [1, 2, 3, 4], our technique has the advantage of improved accuracy and simulation efficiency.

The rest of the paper is organized as follows. In Section II we propose a random process model for power dissipation in sequential circuits and explain its effect on the performance of conventional statistical techniques. In Section III we introduce a sequential procedure to select an independence interval for generation of iid power sample. The implementation of the proposed technique is described in Section IV along with the experimental results of a set of benchmark circuits, followed by concluding remarks in Section V.

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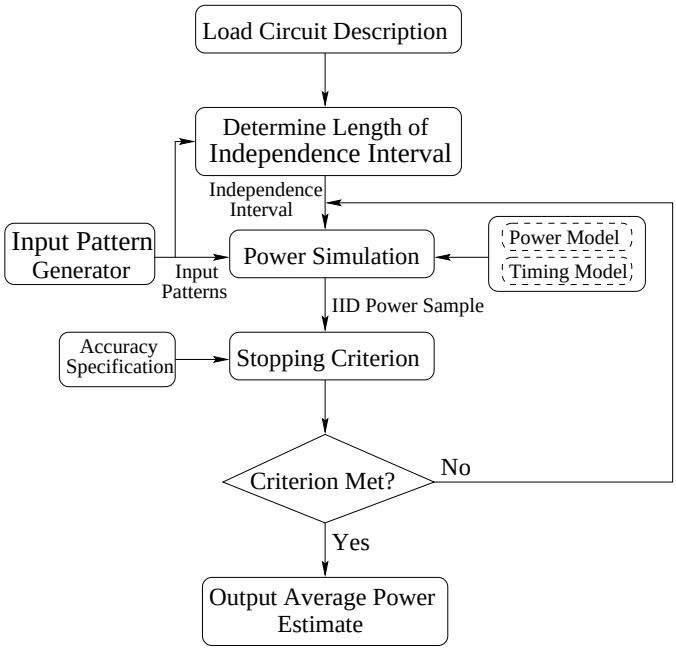

Figure 1: Flowchart of the proposed power estimation approach.

II. Statistical Power Dissipation Model

Ignoring the contribution due to leakage power, switching activity accounts for the major source of power dissipation in CMOS circuits which can be described by the following model:

$$\boldsymbol{P} = \frac{V_{DD}^2}{2T} \sum_{i=1}^{N_g} C_i \boldsymbol{n}_i(\boldsymbol{V}_{k-1}, \boldsymbol{S}_{k-1}, \boldsymbol{V}_k, \boldsymbol{S}_k), \qquad (1)$$

where N_g is the number of elements of the circuit, $\boldsymbol{V}_j$ and $\boldsymbol{S}_j$ ($j = k-1, k$) are the primary input pattern and state vector during jth clock cycle, respectively. C_i is the effective loading capacitance which takes into account short circuit power and internal capacitances. $\boldsymbol{n}_i$ is the transition count at node i. T is the clock cycle time and V_{DD} is the power supply voltage. Because $\boldsymbol{V}$ and $\boldsymbol{S}$ are random quantities, so does $\boldsymbol{P}$. In addition, the feedback of latch signals introduce

temporal correlations among power dissipations in neighboring clock cycles. Thus, the power dissipation behavior of sequential circuits needs to be modeled as a *random process*. For average power estimation, unfortunately, due to temporal correlations conventional statistical techniques can no longer apply. For a correlated power sequence, while it remains true that sample mean is an unbiased estimator of μ, sample variance s_n^2 is not an unbiased estimator of σ^2. If the sample data are positively correlated, as is very often the case in practice, the sample variance will have a negative bias, i.e., $E[s_n^2] < \sigma^2$. In statistical power estimation, s_n^2 is used to construct a confidence interval of the mean which directly determines the sample size that meets the convergence criterion. With negative bias in s_n^2, the confidence interval will be overly narrow. This causes premature termination of power simulation and less-than-specified estimation accuracy.

III. Generation of IID Power Sample

The above problem justifies the need to develop a technique to generate a random power sample from a sequential circuit. Unlike previous approaches which resort to explicit or implicit FSM analysis, our approach "extracts" a random sample directly from the correlated power sequence. This task is equivalent to extracting an iid sequence from the original time series since a random sample can be viewed as generated from an iid random process. To proceed, we assume that $\{\boldsymbol{P}_j\}$ is ϕ-mixing [8] and stationary with finite variance. In essence, ϕ-mixing refers to the property that the behavior of $\{\boldsymbol{P}_j\}$ at two time instants become increasingly independent of each other as they get further apart. This is a mild assumption and is mostly true in practice. Given an observation sequence $P_1, P_2, \ldots, P_n$ of $\{\boldsymbol{P}_j\}$, by stationarity all P_k's have identical distribution functions $F(p)$. If there is an interval of m clock cycles such that P_k and P_{k+m} are independent, then $P_1, P_{1+m}, P_{1+2m}, \ldots$ is an iid sequence, again by stationarity. The existence of m is guaranteed by that $\{\boldsymbol{P}_j\}$ is ϕ-mixing. If we can manage to find an *independence interval* m, a random sample can be obtained simply by recording the power dissipation once for every m clock cycles. To do this, first we use *hypothesis tests* to quantify the independence of a data sequence. Based on the test results, we develop a sequential procedure to dynamically choose the independence interval.

III-A Hypothesis Tests for Independence

In an independence test, we test the validity of the following hypothesis and its alternative

$$\begin{aligned} H: &\quad \text{Sequence is independent} \\ A: &\quad \text{Sequence is not independent} \end{aligned} \tag{2}$$

In the following, we apply three such tests to determine the likelihood of the hypothesis for a power sequence. These tests examine various aspects of $\{\boldsymbol{P}_j\}$, therefore minimize the probability of erroneous test outcome due to statistical fluctuations in the observation sequence.

Lag-One Autocorrelation Coefficient Test

For a power sequence $P_1, P_2, \ldots, P_n$, the maximum likelihood estimator $\widehat{R}_k$ of its lag-k autocovariance is

$$\widehat{R}_k = \frac{1}{n-k-1}\sum_{j=1}^{n-k}(P_j - \overline{P}_n)(P_{j+k} - \overline{P}_n), \quad k \in 0, \ldots, n-1. \tag{3}$$

Using (3), the lag-k autocorrelation coefficient $\widehat{\rho}_k$ can be estimated by $\widehat{R}_k/\widehat{R}_0$. If $P_1, P_2, \ldots, P_n$ is an iid sequence, then the following test statistic

$$D_n = \sqrt{n}\widehat{\rho}_1 \tag{4}$$

has an asymptotic standard normal distribution $N(D_n)$ as $n \to \infty$. Intuitively, for an iid sequence $\widehat{\rho}_1$ is most likely close to zero due to lack of correlation. Thus, for $P_1, \ldots, P_n$, a small value of $|D_n|$ confirms the hypothesis while the alternative tends to be accepted if $|D_n|$ is large. Between the two opposite outcomes, a *critical value* c is chosen such that the hypothesis is accepted only when $|D_n| \le c$. Choice of c is determined by the *significance level* α of the test, where α is probability of type I error in which the hypothesis is erroneously rejected:

$$\begin{aligned} \alpha &= \Pr(\text{Reject } H | H \text{ is true}) \\ &= \Pr(D_n > c | H \text{ is true}) + \Pr(D_n < -c | H \text{ is true}) \\ &= 2(1 - N(D_n)). \end{aligned} \tag{5}$$

With α specified, the corresponding c can be found by

$$c = N^{-1}(1 - \frac{\alpha}{2}). \tag{6}$$

An alternative but related test concerns the following statistic:

$$e_n = 1 - \frac{\sum_{k=1}^{n-1}(P_k - P_{k+1})^2}{2\sum_{k=1}^{n}(P_k - \overline{P}_n)^2}. \tag{7}$$

If $P_1, \ldots, P_n$ is an iid sequence, the test statistic

$$C_n = \sqrt{\frac{(n^2-1)}{(n-2)}}e_n \tag{8}$$

also converges to the standard normal distribution as n increases [6]. This result can be understood by expressing C_n in terms of D_n

$$C_n = \sqrt{\frac{n^2-1}{n(n-2)}}\left[\frac{(n-2)D_n}{(n-1)} - \frac{(P_1 - \overline{P}_n)^2 + (P_n - \overline{P}_n)^2}{2(n-1)\widehat{R_0}}\right]. \tag{9}$$

As n increases, C_n and D_n become asymptotically equivalent and thus have identical limiting distributions. Nevertheless, when n is finite, C_n and D_n distribute differently. In practice the values of C_n and D_n may even be different enough to lead to opposite test outcomes. Therefore, both tests are adopted to minimize the effect of finite sample size on test results,

Spectral Test

The independent hypothesis can also be examined from the spectral perspective of a power sequence. The spectrum of $\{\boldsymbol{P}_j\}$ is defined as

$$g(\lambda) = \frac{1}{2\pi} \sum_{k=-\infty}^{\infty} R_k e^{-j\lambda k}, \quad -\pi \leq \lambda \leq \pi, \qquad (10)$$

where R_k is the lag-k autocovariance of $\{\boldsymbol{P}_j\}$. If $\{\boldsymbol{P}_j\}$ is an iid process, (10) reduces to

$$g(\lambda) = \frac{R_0}{2\pi}, \qquad (11)$$

because $R_k = 0$ for all k but $k = 0$. Thus the spectrum of an iid process is constant over all frequency. For a power sequence of finite length n, we use the *periodogram* method to estimate its spectrum. In this method, $2\pi g(\lambda)$ is approximated by the sum of its components T_j at frequency $2\pi j/n$, where $j = 1, \ldots, n/2$:

$$T_j = \widehat{R}_0 + 2\sum_{k=1}^{n-1} \widehat{R}_k \cos\lambda_j k \qquad (12)$$

$$\lambda_j = \frac{\pi j}{K}, \quad j = 1, \ldots, K = \frac{n}{2}.$$

(12) uses the symmetric property of R_k, i.e., $R_{-k} = R_k$. Using T_j, we define the *normalized cumulative periodogram* S_k as

$$S_k = \frac{\sum_{j=1}^{k} T_j}{\sum_{j=1}^{K} T_j}, \quad k = 1, \ldots, K, \qquad (13)$$

as an estimate of the *cumulative spectral distribution function*:

$$F(\lambda_k) - F(-\lambda_k) = \frac{\int_{-\lambda_k}^{\lambda_k} g(\lambda)d\lambda}{\int_{-\pi}^{\pi} g(\lambda)d\lambda} = \frac{\int_{-\lambda_k}^{\lambda_k} g(\lambda)d\lambda}{R_0}. \qquad (14)$$

Because of its flat spectrum, the cumulative spectral distribution function of an iid process is

$$F(\lambda_k) - F(-\lambda_k) = \frac{R_0}{2\pi}(2\lambda_k)\frac{1}{R_0} = \frac{k}{K}, \qquad (15)$$

a uniform distribution. Using this result, the independence of a power sequence can be tested by comparing its spectral distribution function with (15) using the Kolmogorov-Smirnov test [7], whose test statistic is

$$E_n = \max_k \left(\left| S_k - \frac{k}{K} \right| \right). \qquad (16)$$

The critical value of E_n can be found in the same manner as the lag-one autocorrelation test.

III-B Selection of Independence Interval

Based on the independence tests, a sequential procedure is depicted in Fig. 2 for selection of a proper independence interval. Initially the trial independence interval

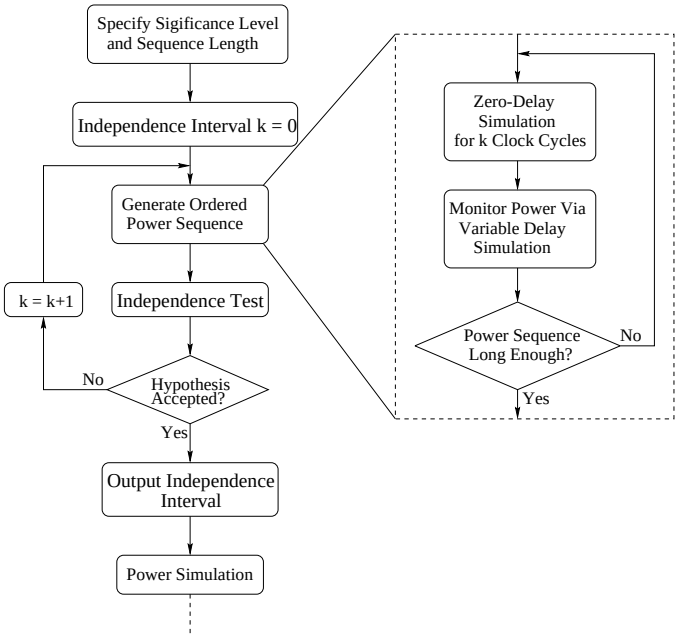

Figure 2: Iteration procedure of independence interval selection.

is set to zero and a power sequence is collected by simulating the target circuit for n consecutive clock cycles. The sequence length n is determined by the trade-off between simulation cost and stability of test outcome. The sequence is then tested by all three independence tests for the user-specified significance level. If the hypothesis is accepted unanimously, the iteration stops and and a zero independence interval is returned. Otherwise the trial interval is incremented by one clock cycle to reduce the temporal correlation and a new power sequence of the same length is generated and tested again. The iteration continues until the desired significance level is achieved. The trial interval at the end of iteration is an appropriate independence interval at which an iid power sample can be generated for convergence analysis.

VI. Average Power Estimation and Experimental Results

With the selected independence interval, a two-phase simulation approach is adopted to generate an iid power sample for the sake of efficiency. A zero-delay simulator is invoked to simulate the circuit over the independence interval and power is monitored by a general-delay simulator during the sampling clock cycle. To determine convergence of the average power estimate, we use a nonparametric criterion based on the order statistics [5].

The proposed procedure has been implemented on top of our distribution-independent power estimation tool (DIPE) [5]. The default significance level of the independence tests is 0.10 to minimize the probability that a power sequence is erroneously taken as independent when it is autocorrelated. The power sequence length n used in the tests needs to be carefully chosen as well. For simulation efficiency, a small n is desirable; however, the sequence needs to be of appropriate length since the stability of test outcome improves with increasing n. In the following experiments, we

Circuit Name	SIM (mW)	$I.I.$	$\overline{\mu}_p$ (mW)	Sam. Size	CPU Time(s)
s208	0.276	1	0.276	4896	138.3
s298	0.430	4	0.430	2624	93.4
s344	0.751	2	0.750	864	19.0
s349	0.785	5	0.785	992	67.9
s382	0.433	3	0.433	2272	83.9
s386	0.519	2	0.520	1856	40.8
s400	0.418	5	0.419	2336	116.9
s420	0.353	2	0.354	4576	184.5
s444	0.427	3	0.428	2400	85.5
s510	1.175	5	1.175	3072	212.0
s526	0.443	2	0.433	2368	77.3
s641	0.786	2	0.787	1152	39.9
s713	0.804	2	0.804	1088	41.1
s820	0.957	3	0.957	1920	91.6
s832	0.941	3	0.941	2016	96.3
s838	0.443	4	0.443	2880	182.7
s1196	3.080	3	3.083	672	104.6
s1238	3.009	3	3.143	672	114.5
s1423	2.773	3	2.774	2528	604.5
s1488	1.844	4	1.843	4032	492.9
s1494	1.735	4	1.731	3904	433.2
s5378	6.667	4	6.659	672	336.0
s9234	2.008	6	2.005	928	746.0

Table 1: Power estimation results.

Circuit	II_{min}	II_{max}	II_{avg}	S_{avg}	D_{avg}	Err(%)
s208	1	8	2.69	5001	0.78	0.0
s298	3	8	3.76	2659	1.07	0.0
s344	2	10	2.93	954	0.98	0.0
s349	2	9	3.19	961	1.00	0.0
s382	2	8	3.35	2249	0.99	0.0
s386	2	7	2.44	1791	1.04	0.0
s400	3	9	3.50	2291	1.05	0.0
s420	1	8	1.53	4287	1.22	0.9
s510	1	6	1.43	3138	1.04	0.0
s526	2	8	3.06	2231	1.06	0.0
s641	1	8	2.42	1075	0.99	0.0
s713	1	10	2.44	1094	0.94	0.0
s820	2	8	3.23	1946	0.97	0.0
s832	2	8	3.32	2049	0.92	0.0
s838	1	28	10.65	2718	1.84	1.5
s1196	1	7	2.41	672	0.84	0.0
s1238	1	8	2.33	672	0.82	0.0
s1423	2	8	3.30	2415	1.09	0.1
s1488	2	7	3.63	4010	1.17	0.1
s1494	2	10	3.67	4015	1.19	0.0
s5378	2	19	6.01	672	0.87	0.0
s9234	3	9	4.76	884	0.81	0.0

Table 2: Performance summary from 1000 simulation runs.

choose $n = 640$ as a good trade-off between stability and efficiency.

We test our implementation with a set of ISCAS89 benchmark circuits on a SPARC 20 workstation with 244 MB memory. Circuits operate at 20 MHz of clock frequency and 5V power supply. The maximum allowable error is 5% with 0.99 confidence level. Primary input signals are assumed to be mutually independent and have probabilities of 0.5. Table 1 shows the power estimation results of the test circuits. In Table 1, SIM is a very accurate estimate of the real average power. $I.I.$ is the independence interval determined by the procedure in III-B. $\overline{\mu}_p$ is the average power estimate from a sample of size listed under column Sample Size which achieves the accuracy specification. The last column reports the CPU time usage. It is shown that our technique can produce accurate average power estimates with reasonable amount of time. With random input patterns, an independence interval of a few clock cycles usually suffices to generate an iid power sample. The capability of dynamic independence interval selection offered by this technique preserves the simulation efficiency of DIPE.

To evaluate the average performance of the technique, we conducted 1,000 simulation runs for every circuit and summarized the results in Table 2. In this table, II_{min}, II_{max} and II_{avg} are the minimum, maximum, and average length of the independence interval, respectively. S_{avg} is the average sample size and D_{avg} is the average percentage deviation of the estimation results from the reference value. Err is the percentage of the total runs violating the accuracy specification. Table 2 shows that the estimation results produced by the proposed technique indeed meet the accuracy specification and are in general very accurate.

V. Conclusion

We have proposed a new statistical technique for average power estimation in sequential circuits. Due to the feedback mechanism, power dissipations of a sequential circuit in consecutive clock cycles are temporally correlated. On the other hand, statistical average power estimation requires an iid sample. We have developed a sequential procedure to select a proper independence interval using which an iid sample can be generated. The sample is then analyzed by a distribution-independent stopping criterion to determine an appropriate convergent sample size. The accuracy and robustness of this technique have been successfully demonstrated.

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