A New 4-2 Adder and Booth Selector for Low Power MAC unit

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ABSTRACT

The integration level of VLSI system increases as the technology improves. The power dissipation of the data processing unit in the digital signal processing systems must be kept as low as possible. Thus, we newly designed a 4-2 adder and a booth selector by using transmission gate circuits to accomplish low power consumption without performance sacrifice. The proposed 4-2 adder consumes lower power than the conventional 4-2 adder by 16% and the proposed booth selector consumes less power than the conventional booth selector by 60%. We designed a 32-bit MAC unit with the proposed 4-2 adder and the booth selector. The power dissipation of the 32-bit MAC unit is 124mW at 100MHz with 2V power supply, with the area of 1.3mm×2.4mm.

1 INTRODUCTION

A parallel multiplier is a key component in digital signal processors which are integrated in system LSIs for signal processing or multimedia applications. Since most of multimedia applications are oriented toward hand-held form, it is critical to design system LSIs such that total power consumption is as low as possible, which results in the prolonged battery life. Some researches suggest the pass transistor circuits for low power consumptions. If the threshold voltage of PMOS transistor is equal to that of NMOS transistor, pass transistor circuits consume more power than the conventional CMOS circuits due to the DC power dissipation by turn-on of PMOS transistor. Also, the pass transistor circuits can be slower than the conventional static CMOS circuits because the driving capability of the buffer depends on the range of the input voltage. Therefore, in this paper, we propose a new low power 32-bit MAC unit for DSP applications. We use the transmission gate circuits in the circuits of MAC unit as a modified type to get the full swing of the node voltages. Since power consumption is proportional to area of MOS transistors, the widths of MOS transistors are minimized as small as possible with the aid of SPICE simulations. First, we designed the MAC unit at architecture level with Verilog-XL simulator. When we described the MAC unit with Verilog HDL, we minimized the I/O pin connection of each sub-block and removed the redundancy of each sub-block. After verification of the removal of the redundancy, we designed the each sub-block at circuit level. At circuit design level, since the multiplier mainly consists of three parts, Booth block, Wallace tree and parallel adders, we minimized power dissipation in Booth block and Wallace tree by reducing the number of transistors and optimizing the width of each transistor.

2 DESIGN OF A MAC UNIT

Since the dynamic power dissipation is proportional to the capacitance and the supply voltage, we approach the low power design of 32-bit MAC unit through two aspects, the reduction of the number of transistors and the scaling of the supply voltage. First, we started the design of MAC unit by fixing the supply voltage at 2 volt considering our process conditions to get the appropriate performance. Second, we select the circuit types which is more efficient than other circuits for the given supply voltage.

2.1 Circuit Types

To decide the circuit types of our 4-2 adder and booth selector, we compare two circuit types, pass-transistor circuits and transmission gate circuits. In the pass-transistor circuits, the discharging of the capacitance depends only on NMOS transistor. Assuming that discharging current is constant, the discharging time of pass-transistor circuits is given by (1).

$$Discharging \quad time = \frac{C\Delta V}{I} \tag{1}$$

In the transmission gate circuits, the discharging conditions are worse than the pass-transistor circuits because of the drain capacitance of PMOS and the larger swing voltage. However, for the charging conditions, as the voltage of output node increases, the current of NMOS transistor decreases quadratically and the current of PMOS transistor decreases linearly. Since the rising time of the pass transistor circuits becomes larger than that of the transmission gate circuits below about 2V as shown in APPENDIX, we decided to use the transmission gate circuit as a basic circuit type for 4-2 adder and booth selector.

2.2 Design of A 4-2 Adder and A Booth Selector

We designed the 32-bit multiplication and accumulation(MAC) unit which can be adopted in the digital signal processing system using transmission gate circuits. Fourth Wallace tree in MAC unit is used for the accumulation of the previous multiplication result and the

current multiplication result in calculation. Table 1 shows the number of 4-2 adders and the number of Booth selectors in the 32-bit MAC unit. As shown in Table 1, it is crucial to reduce the number of transistors in 4-2 adders and Booth selectors for low power consumption except 64-bit parallel adder. We designed a new 4-2

Table 1: Required 4-2 adders and booth selectors for a 32-bit MAC unit

Block	Required Number
4-2 adders	369
Booth selector	512

adder with lowest number of transistors, and these newly designed 4-2 adders are used in Wallace tree of the multiplier. We generated the truth table of 4-2 adder and drew the logic diagram as shown Figure 1. To minimize the number of transistors, we simplified the initial gate level and used transmission gate circuits in the complicated logic gate and finally stabilized the carry-out and sum signals. The circuits of shaded area in Figure 1 are made by transmission gates because transmission gate logic is most effective in terms of the number of MOS transistors and delay time at low supply voltage. The final 4-2 adder circuit is shown in Figure 2. In

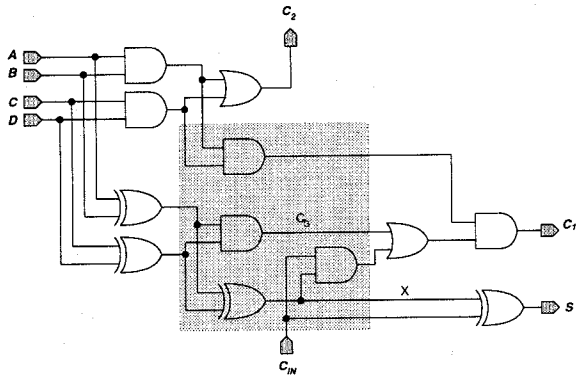


Figure 1: Logic Diagram of New 4-2 Adder Concept

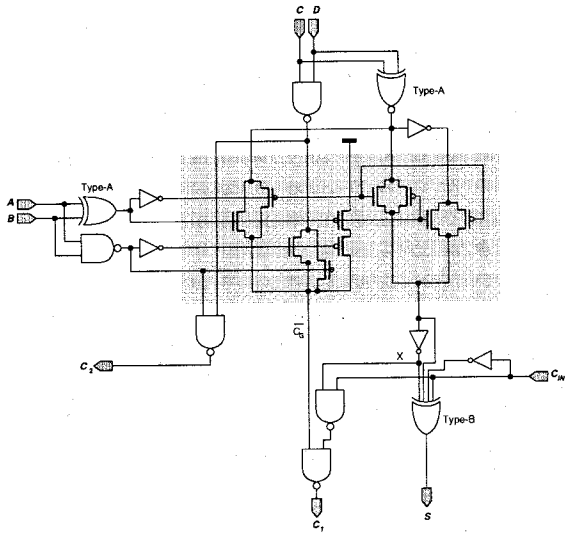


Figure 2: Circuit Diagram of New 4-2 Adder

Figure 2, there are three XOR(including XNOR†) circuits. We decided to use XOR circuits appropriate for our circuits to minimize the power dissipation and the area. We used two type of XOR(or XNOR) circuits as shown in Figure 3. Type B is used for large load capacitance when the complement input signal is provided and the driving capability of the previous circuits is weak. We fixed the width of NMOS transistors at $2\mu m$ and simulated delay times with respect to the widths of PMOS in the transmission gate with different load capacitances. The results show that 6-transistor type XOR is the best for lower capacitive load with $4\mu m$ PMOS width. The simulation results of XOR circuits(Type A) are shown in Figure 4. To minimize the number of MOS transistors and the area, complement signals can be provided from previous circuits. Thus, Table 2 shows that the proposed 4-2 adder circuits have lower number of transistors and reduce the power consumption by 16% compared to the previous 4-2 adder[2]. Figure 5(b) shows the proposed 4-2

Table 2: Comparison of Two 4-2 adder circuits

	Conventional Circuits	The proposed Circuits
Number of Transistors	68	58
Power Dissipation $[\mu W]$	172	140
Time delay $[nsec]$	1.9	1.7

adder consumes less power than the conventional circuits for the supply voltages from 3.0 to 1.8 volt. And, the proposed 4-2 adder is a little faster than the conventional static CMOS 4-2 adder. The area of transmission gate region marked with shaded area in Figure 2 is only about 11% of the the total area as shown in Figure 6. The same circuits are used in the second Wallace tree as the register type to get high bandwidth of MAC unit. 4-2 adders in the boundary of the Wallace tree have 2 or 3 inputs. Table 3 show the distribution of 4-2 adders depending on the number of inputs. Thus, we can save the area and power consumption by careful inspections. The number of transistors is reduced by adopting the modified four circuit types of 4-2 adders as shown in Table 3. For the Booth selector,

Table 3: Number of modified 4-2 adders

4-2 Adder	Number	No. of Transistors
2-inputs with carry	7	31
2-inputs without carry	46	15
3-inputs with carry	40	43
3-inputs without carry	38	27
4-inputs with carry	235	58

only 14 transistors are used for small area and low power operation without performance degradation by adapting the transmission circuit concept. The proposed circuit of Booth selector is drawn in Figure 7. Since M and 2M signals are not set in the same time, we

† XNOR circuits can be obtained easily by exchanging A and $\overline{A}$ in the Figure 3.

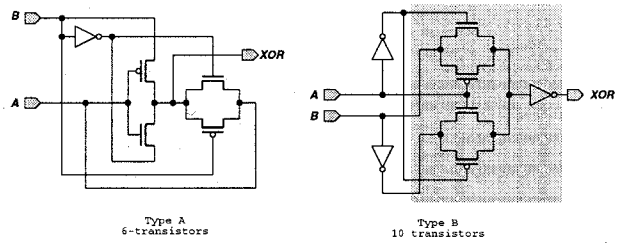


Figure 3: Two type of XOR Circuits

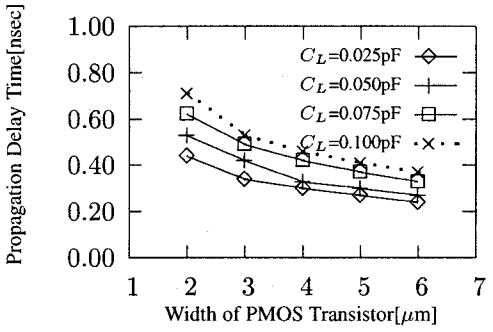


Figure 4: Delay Time of 6-Transistor XOR Circuits(Type-A)

could simplify the circuits. The proposed Booth selector dissipates smaller power than the conventional booth selector, which consists of 22 transistors, by 21%. The comparisons of two Booth selectors are shown in Figure 9. We used CLA type parallel adder for 64-bit addition to meet the clock speed. The effects from the reduction in the newly designed 4-2 adder and booth selector by our design approach are shown in the Figure 8.

3 CONCLUSION

We designed new MAC unit by full custom design. The simulation results show that the newly designed 4-2 adder in the Wallace tree dissipates lower power than the previously reported result[2] by 16% without increasing time delay. By designing a new 4-2 adder and a Booth selector we reduced the power dissipation, and we reduced total number of MOS transistors by 28% as shown in Figure 8. SPICE simulation results of each block are summarized in Table 4. The MAC unit can be operated at 100MHz with 2V V_{CC} by inserting a pipeline register in the second Wallace tree. The area of 32-bit MAC unit is approximately 1.3mm×2.4mm with 0.35μm design rule with 4-layer metal.

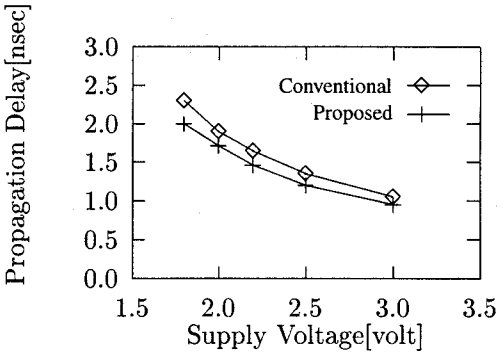
APPENDIX

For NMOS pass transistor circuits, the time which is required to charge the output node from $V_{CC} - V_{TN} - 0.5$ to $V_{CC} - V_{TN}$ is

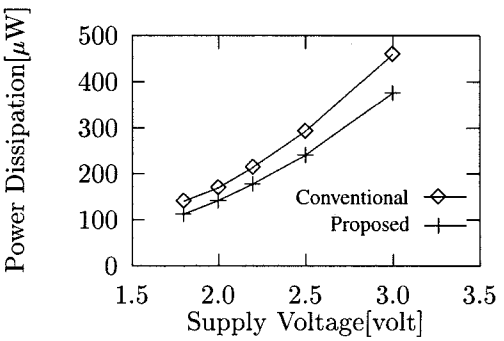
$$\Delta T = \frac{2C_{LN}}{\mu_n C_{ox} \frac{W_N}{L_N}} \frac{0.5}{(V_{CC} - 2V_{TN})(V_{CC} - 2V_{TN} - 0.5)} \quad (2)$$

However, in transmission transistor circuits, the time required to charge the output node from $V_{CC} - V_{TN} - 0.5$ to V_{CC} by PMOS only is approximately calculated as (3).

$$\Delta T = \frac{2C_{LP}}{\mu_p C_{ox} \frac{W_P}{L_P}} \frac{1}{(V_{CC} - \frac{1}{2}V_{TN} - 0.25 - V_{TP})(V_{TN} + 0.5)} \quad (3)$$



(a) Propagation Delay



(b) Power Dissipation

Figure 5: Comparison of Two 4-2 Adders

From the above two equations (2) and (3), we can calculate an example as follows. Assuming that $\frac{\mu_n}{\mu_p} = 3, W_P = 3W_N, L_P = L_N$, and $V_{TN} = |V_{TP}| = 0.5$ volt, the supply voltage at which the above two delay times in (2) and (3) are equal is given as (4).

$$V_{CC} = 1.5 + \frac{1}{3}\frac{C_{LN}}{C_{LP}} \quad (4)$$

Since the body-effect is not considered in the threshold voltage in (2) and the turn-on effect of NMOS in transmission gates, the result in (4) is underestimated. We can estimate that as the supply voltage decreases, the rising time is significantly increased in the pass transistor circuits. But, the transmission gate suffers from the time delay in the circuits with large load capacitance. Thus, we mixed the static full CMOS circuits and transmission gate circuits for the

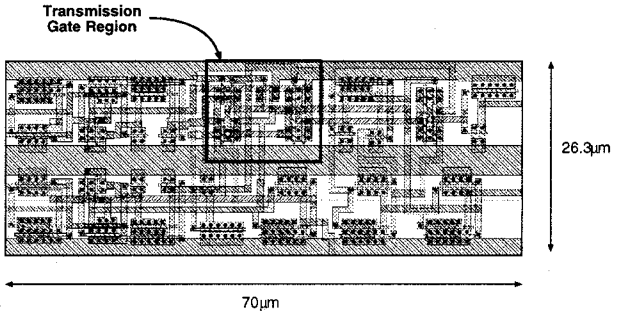


Figure 6: Layout of New 4-2 Adder

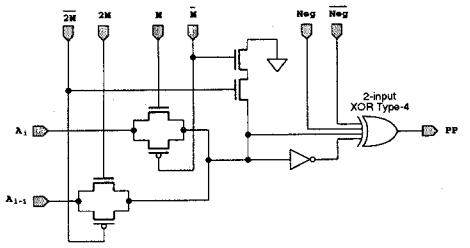


Figure 7: The proposed circuits of the booth selector

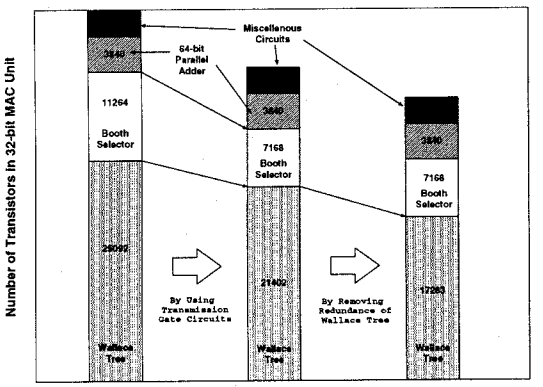


Figure 8: Reduction of the number of transistors

trade-off of the propagation delay and the power dissipations.

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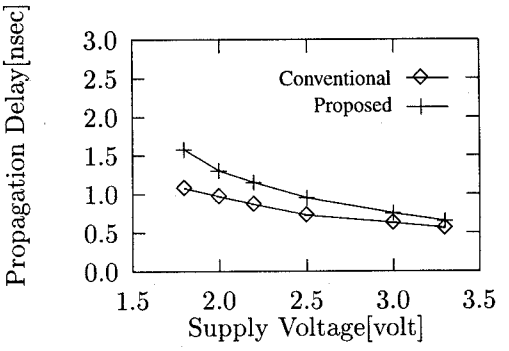
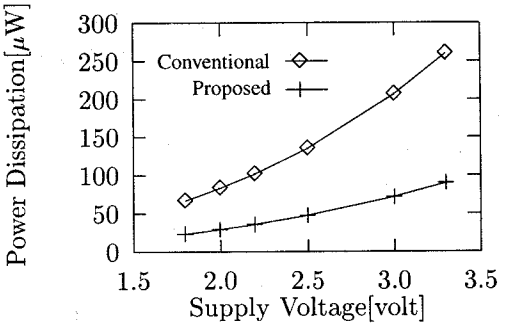
Table 4: Delay time and Power Dissipation of Each Circuit Block

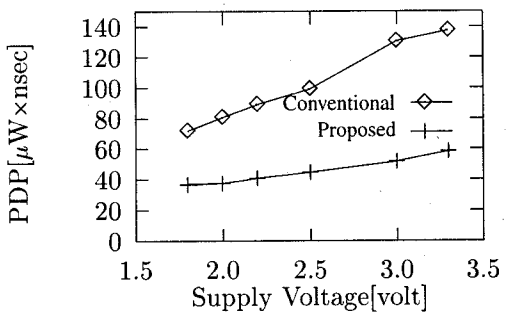
Circuit Block	Delay Time [nsec]	Power Dissipation [mW]
Booth Circuits	2.2	19.36
Wallace Tree	8.0	82.32
64-bit Adder	4.5	21.5



(a) Propagation Delay



(b) Power Dissipation



(c) Power Delay Product

Figure 9: Comparison of Booth Selector