A capacitor-based D/A converter with continuous time output for low-power applications.

Lapoe Lynn, Paul Ferguson Jr.

Analog Devices, Inc.

Abstract

A digital to analog converter has been developed using switched capacitors as the basic DAC elements. The use of switching capacitors provides excellent matching without sacrificing die area, and allows for very low-power operation. However, the architecture provides significant challenges when used in a continuous-time application requiring a “smooth” output. A realization of this architecture in a standard 0.6um CMOS process achieved 10 bits of linearity while consuming less than 200uA of current.

Introduction

A general trend in the integrated circuit industry is towards higher integration. Particularly in consumer markets such as portable communications, computer products, etc... higher levels of integration result in a smaller bill of materials, and therefore, power, area and cost savings. The performance parameters of circuits targeted for a high integration ASIC can be very different from those of a general purpose circuit with the same function. Therefore, the design of such circuits should be approached differently. In the design of general purpose digital to analog converters (DACs), switched-capacitor charge redistribution structures have largely been avoided for a variety of reasons including the need for a clock and the desire to avoid switching noise on the continuous time output of the DAC. Instead, attention has focused more heavily on switched-current or resistive ladder techniques.

In today’s standard mixed signal IC technology, polysilicon capacitors provide the best component matching per unit of area. It makes sense, therefore, to use poly-poly capacitors as the basic unit element in a high resolution converter. Especially in highly integrated mixed signal chips where a clock is readily available, a capacitor based DAC can save area and power over structures which rely on matching currents or voltages in transistors and/or resistors.

This paper will describe a technique for implementing capacitor based charge-redistribution DACs suitable for small area, low power, and high accuracy implementations. The proposed architecture incorporates a capacitor array which implements the D/A function, a zeroth order sample and hold, and an output amplifier all into a single compact structure.

Basic Topology

The basic architecture of a switched-capacitor based charge redistribution DAC is shown in Fig. 1. Samples of charge proportional to the unit capacitor value **C**, the reference voltage **Vref**, and the digital input word are sampled onto the array of input capacitors during phase Φ_2. During phase Φ_1, charge from the input capacitors are integrated onto the integrating capacitor, $\mathbf{C_i}$, to generate an output proportional to the input code. The switch in parallel with $\mathbf{C_i}$ has a dual purpose: it removes charge on a sample-by-sample basis from the integrating capacitor, and at the same time, it auto-zeros the amplifier, preventing the offset of the amplifier from appearing at the output. Unfortunately, any charge redistribution converter will require the removal of each charge sample from the integrating capacitor in order for the following sample to be processed. This means that a sample and hold -- more specifically, a zeroth order sample and hold -- is required in order to avoid producing the reset voltage on the output every cycle.

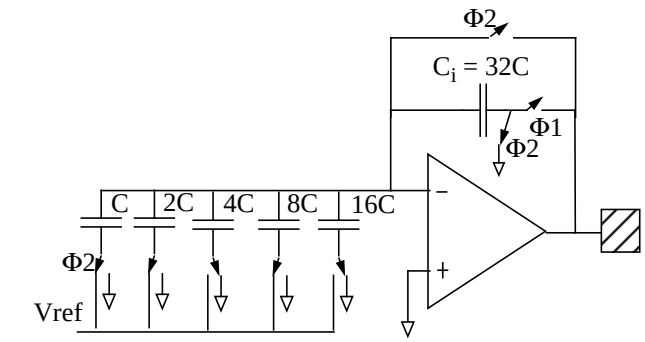
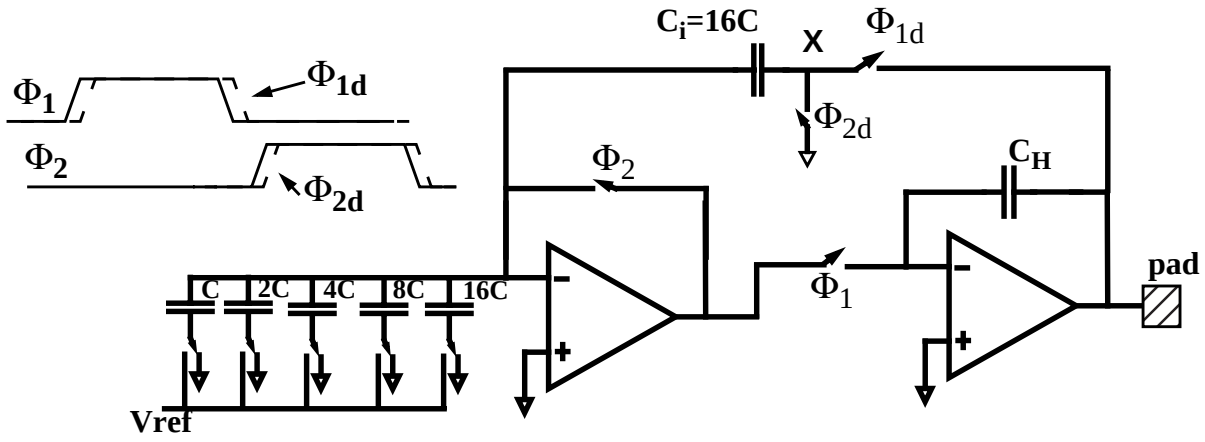


Fig. 1. Basic charge redistribution DAC

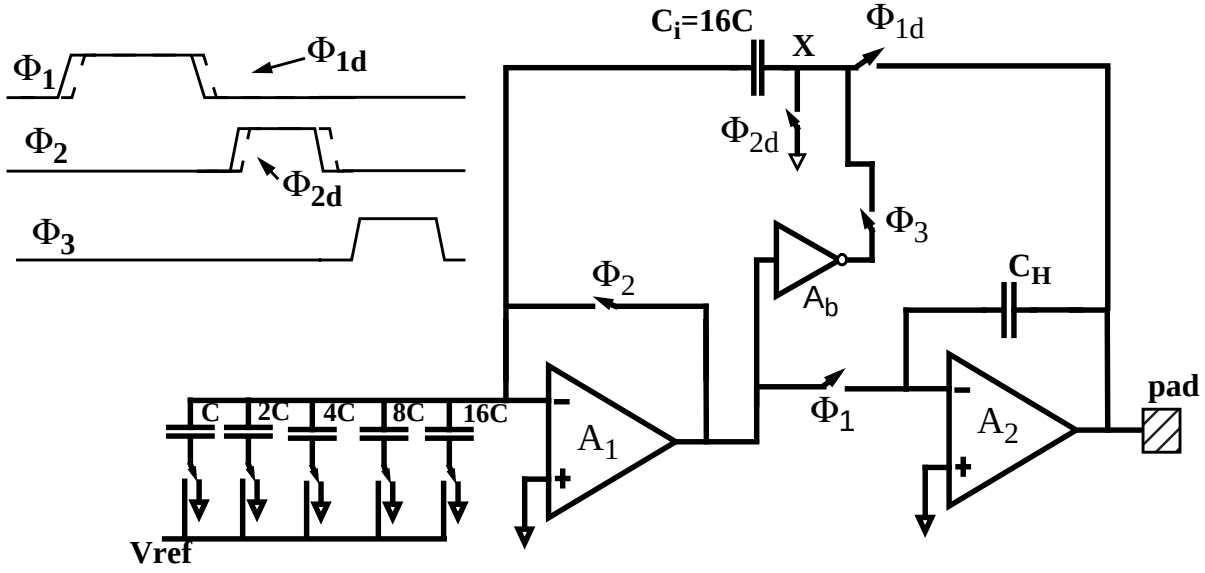
Proposed Architecture

Fig. 2. shows a modification to the basic structure which allows the output to be held at its previous value while the integrating capacitor is being reset. In this case, the amplifier has been split into two independent amplifiers. During Φ_2, when the previous output value is being re-



- **Idea is to hold output on C_H while S/H resets (offset of first stage only cancelled)**
- **Small pedestal occurs on output during transition between Φ_1 and Φ_2 (charge injection from Φ_1 switch)**

Fig. 2. Zeroth order S/H operation combined with DAC



- **Idea is to use small amplifier A_b to precharge the parasitic at node X to the next output during extra phase Φ_3.**
- **When Φ_{1d} connects node X to the output, the output will settle to next value without glitching.**

Fig. 3. Bootstrapping technique used to precharge parasitic on C_i

moved from the integrating capacitor $\mathbf{C_i}$, the output is held constant on capacitor $\mathbf{C_H}$. When a new word is to be evaluated during Φ_1, the two amplifiers are cascaded together into a two stage amplifier, and $\mathbf{C_H}$ effectively becomes the compensation capacitor for a single op amp. In other words, during Φ_1, the new structure looks just like Fig. 1., and during Φ_2, the first half of the amplifier is used to autozero the DAC, while the second half of the amplifier is used to hold the continuous time output stable at the previous value. The auto-zero function removes the offset of the first amplifier; the offset of the second amplifier gets divided by the gain of the first stage when referred to the input. This auto-zeroing also serves to remove low frequency (1/f) noise of the amplifier -- since it essentially amounts to a correlated double-sampling of the input referred noise of the first amp. Furthermore, this structure can also be used to drive the output directly, removing the need for an extra output amplifier altogether. Since the switched capacitor DAC itself consumes no static power, the power consumption of this architecture is determined solely by the output driver; whereas other architectures would have power dissipated in the DAC core as well as in the driver. In the example of Fig. 2., the integrating capacitor has been sized to include a gain of 2x in the DAC function as well. The final implementation included this gain of 2 and also used the integrating capacitor as a sampling capacitor for the most significant bit of the DAC -- saving a significant percentage of the capacitor array area.

In order to minimize the effects of charge injection, non overlapping clocks Φ_1 and Φ_2 (shown in Fig. 2.) are used to control the switches performing the sampling operation, and delayed versions of Φ_1 and Φ_2 are use to control all other switches. Charge injection from switch Φ_2 will only affect the auto-zeroed value of amplifier $\mathbf{A_1}$, and may cause a few mV's of offset. Charge injection from opening switch Φ_1 will cause a small pedestal to appear on the output as the DAC goes into sample mode (Φ_2). A small square wave at the clock frequency will be seen on the output as the DAC switches between sample and hold modes. This switching noise is signal independent (provided the gain of the second stage amplifier is sufficiently high) and will only cause a small offset on the DC component of the output.

A more troublesome side effect of this topology is the charge sharing that occurs when switch Φ_{1d} is closed. Note that during phase Φ_{2d} the right side of $\mathbf{C_i}$ in Fig. 2. (shown as node **X**) is reset to a DC potential (in this case, ground). during this time, the output is held at it's previous value on $\mathbf{C_H}$. However, when switch Φ_{1d} is closed, charge on $\mathbf{C_i}$ and the parasitic at node **X** gets shared with the charge on the output node -- causing the output to spike before the action of the closed loop amplifier can drive the output to the next value.

To alleviate this glitching, a third phase (Φ_3) is added between phases, Φ_2 and Φ_1. During Φ_3, a small amplifier $\mathbf{A_b}$ (shown in Fig. 3.) is used to drive the parasitic capacitance at node **X** to the output value. When Φ_1 arrives, node **X** and the output node are connected through switch Φ_{1d}, but node **X** has already been driven to the correct voltage; so no glitch occurs as the large amplifier $\mathbf{A_2}$ drives the output node the correct voltage as well.

In reality, amplifier $\mathbf{A_1}$ in Fig. 3. must be a non-inverting amplifier for the feedback around the $\mathbf{A_1}$ - $\mathbf{A_2}$ and $\mathbf{A_1}$ -

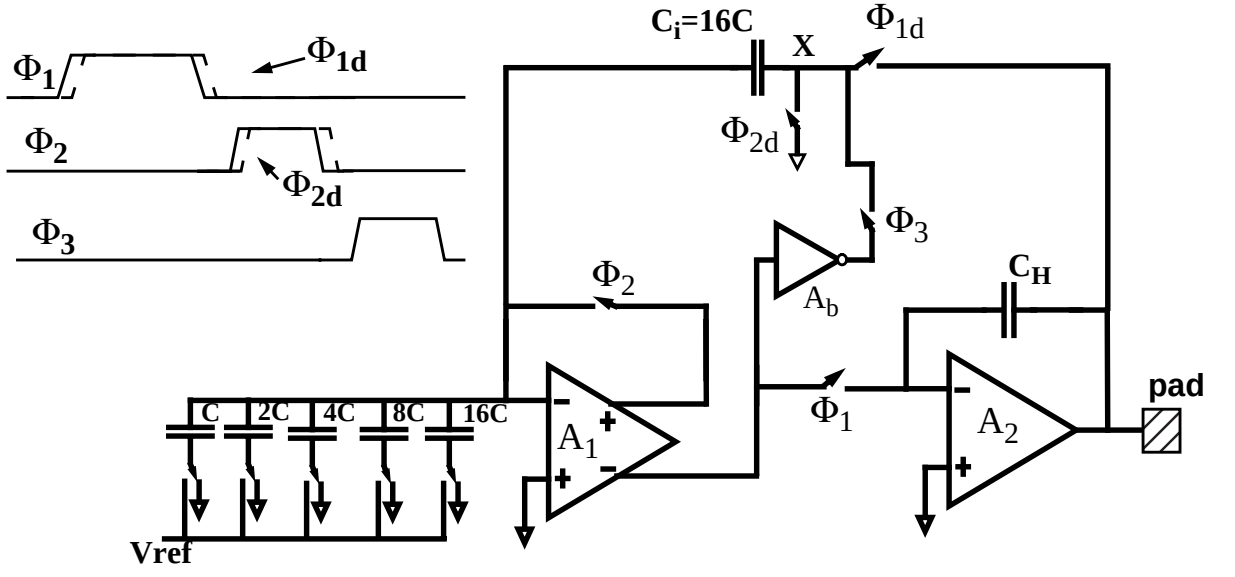


Fig. 4. Polarity of $\mathbf{A_1}$ modified for proper operation.

$\mathbf{A_b}$ cascade to be stable. Therefore, amplifier $\mathbf{A_1}$ is reconfigured as an inverting amplifier in the auto-zero phase (Φ_2), and as a non-inverting amplifier in the hold phase (Φ_1). This is illustrated in Fig. 4.

Circuit Implementation

Fig. 5. shows a simplified implementation of the zeroth-order sample and hold circuit. Amplifier $\mathbf{A_1}$ is denoted as the "reset amp", amplifier $\mathbf{A_2}$ is labelled as the "output amp", and the bootstrapping amplifier, $\mathbf{A_b}$, is shown in the light-colored lines. The polarity change on amplifier $\mathbf{A_1}$ is accomplished by switching the polarity on the active mirror load $\mathbf{M_1}$ - $\mathbf{M_2}$. Transistor $\mathbf{M_3}$ samples charge on the holding capacitor $\mathbf{C_H}$, and therefore has a charge cancellation switch associated with it. The bootstrapping amplifier is implemented as a very small, carefully sized digital inverter. Amplifier $\mathbf{A_2}$ is a standard 2-stage op-amp designed to drive a 50 kohm, 50 pF load rail to rail. Therefore, when $\mathbf{A_1}$ and $\mathbf{A_2}$ are cascaded together, a three stage amplifier is formed. Care must be taken in the choice of capacitor $\mathbf{C_H}$ since it not only holds charge during the hold phase, it also acts as the outside compensation loop of the nested-miller compensation that keeps the $\mathbf{A_1}$ - $\mathbf{A_2}$ cascade stable. $\mathbf{A_2}$ consumes a majority of the power in the entire DAC (~80%).

The capacitor arrays shown in the previous figures represent a 5-bit binary weighted DAC, but the structure can easily be extended to higher resolution by increasing the size of the input array. Fig. 6. shows a 10 bit DAC that has been segmented into two 5 bit arrays. A small amplifier and integrating capacitor has been added the LSB array to make this segment parasitic insensitive. This amplifier can be very small or can be omitted entirely if care is taken with layout parasitics.

Results

The topology shown in Fig. 2. combines the basic charge redistribution DAC function with a zeroth order sample and hold and an output amplifier. Several DACs based on this architecture have been designed and characterized. Despite using binary-weighted arrays in two 5 bit segments, 10 bit linearity (<1lsb DNL, <1lsb INL) is achieved with a compact 500µm x 600µm structure (~0.46k sq. mils). A slightly larger structure (500µm x 1000µm) included an 8 bit coarse DAC overlapped with a 10 bit fine DAC for 13 bits overall. This DAC was optimized for low power and consumed 250µA from a 3 volt supply at a 45kHz update rate. The power was reduced further (<200µA) in a low-power mode where an on-chip oscillator was used to keep the DAC refreshed without the need for an external clock.

Fig. 7. and Fig. 8. show measured DNL and INL for the 10 bit fine DAC. This DAC is being used as part of a frequency control loop in digital cellular phones. The output of the DAC regulates the frequency of the master os-

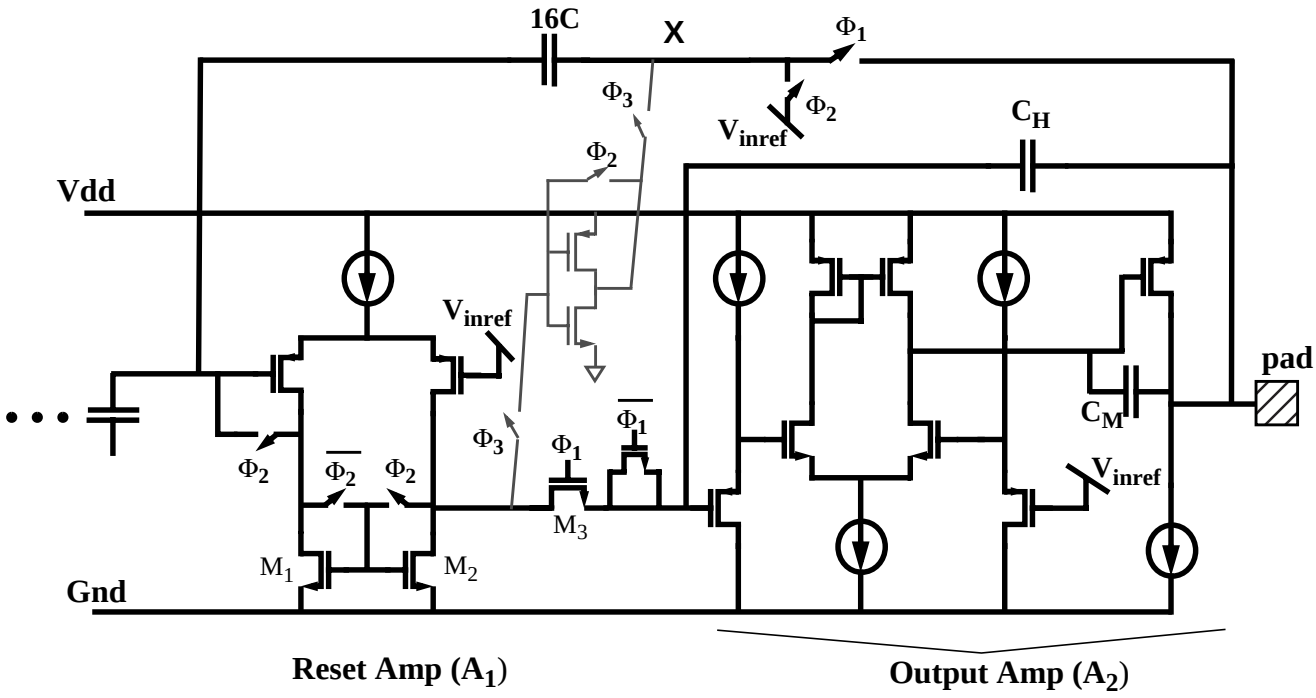


Fig. 5. Simplified schematic of amplifiers A_1, A_2, and A_b

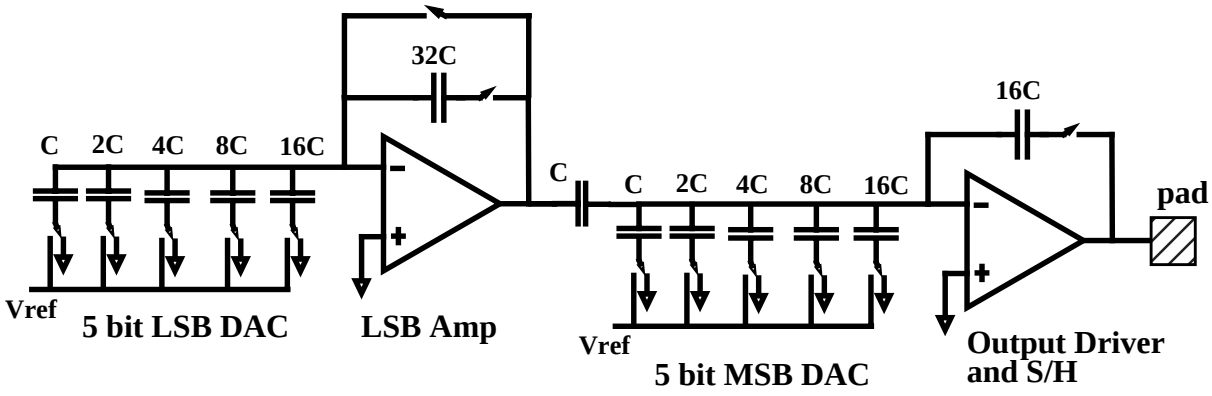


Fig. 6. Full 10 bit implementation

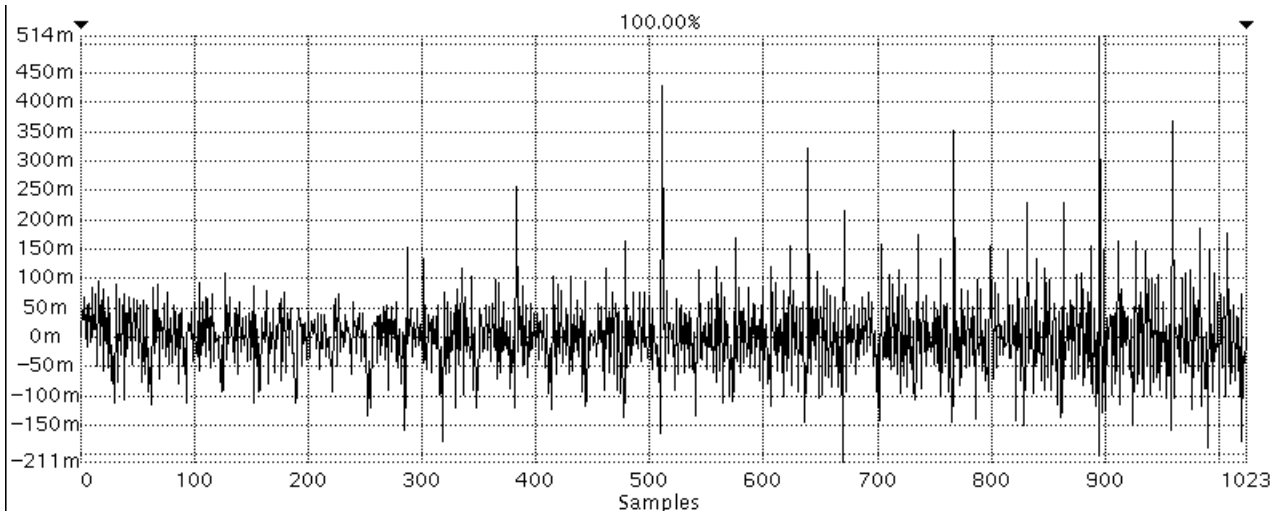


Fig. 7. measured DNL (in milli-LSB's)

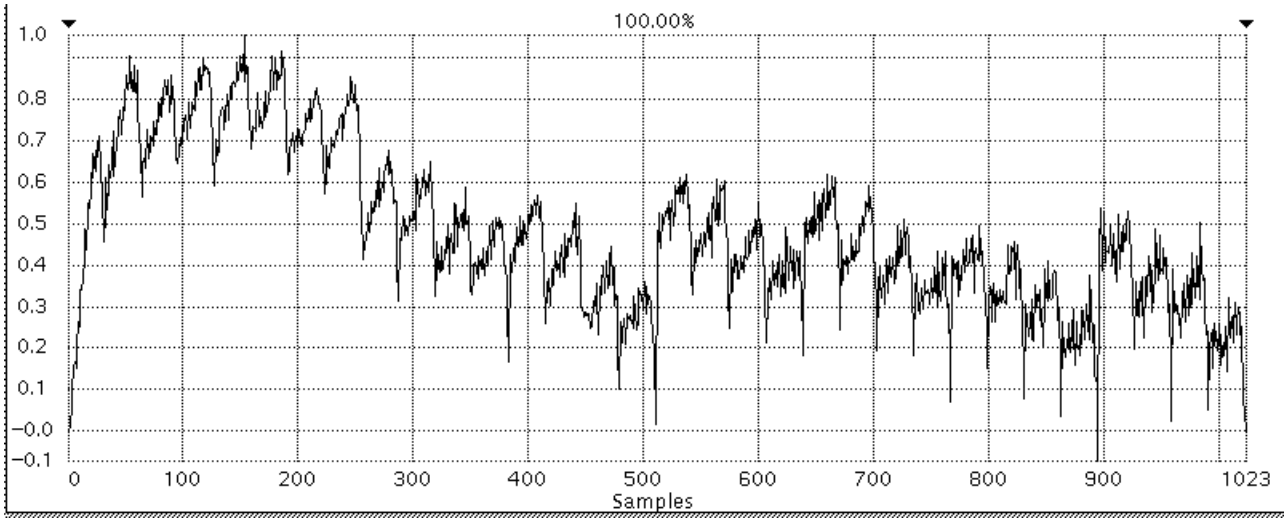


Fig. 8. measured INL (in LSB's)

cillator in the phone. Since tight control over the frequency of the master clock must be maintained even when the phone is in standby, the power consumption of this DAC is one of the key determinants of phone battery life. The use of this architecture consumed less area, and ~75% less current than the previous design, which used a weighted-current-source architecture.

Conclusions

A switched-capacitor based D/A converter has been described for use in low-power, high-integration applications. A zeroth-order sample and hold circuit uses a three-stage amplifier, correlated double sampling, and parasitic bootstrapping to produce a continuous time output. An implementation on a standard, double-poly CMOS process achieved 10 bits of linearity while consuming less than 200uA from a 3 volt supply.

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