A Low Voltage CMOS Current Source

Detlev Schmitt and Terri S. Fiez
School of EECS
Washington State University
Pullman, WA 99164-2752

ABSTRACT

A low voltage current source is described that has a minimum input voltage of less than 0.1V and a minimum output voltage swing of 0.2V. Although this current source has an output voltage range equivalent to a simple current mirror, the output resistance is amplified by a feedback amplifier to produce an output resistance on the order of a cascode current source. The low voltage current source was fabricated in a 2 micron n-well CMOS process. The measured minimum output voltage is 0.2V and the measured output resistance is $11 M\Omega$. Using this current source, a 1.8V folded-cascode op amp was designed. The simulated open loop gain was 50dB with a nearly rail-to-rail output linear range.

1 INTRODUCTION

As integrated circuit process geometries continue to scale down, power supply voltages must often follow to ensure reliable device operation. Unfortunately, as the power supply voltage is reduced, the threshold voltage does not necessarily scale proportionally. In fact, many submicron 3-V processes have threshold voltages as high as 0.9 Volts. With such high threshold voltages, it is difficult to design high performance analog circuits. Thus, basic building blocks including current sources, gain stages, output buffers and operational amplifiers that operate with low power supply voltages are needed. In this paper, a low voltage CMOS current source is presented. The output voltage can be within 0.2 volts of the supply while maintaining an output resistance similar to a cascode current source. Using this current source, a 1.8 V folded-cascode operational amplifier is designed with an open loop gain of 50dB and a linear output range of 0.2V to 1.6V.

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2 The Low Voltage Current Source

The general schematic of the low voltage current source is shown in Fig. 1. Both M1 and M2 are biased in the linear region. The amplifier senses the drain voltages of M1 and M2 and amplifies the difference. The output of the amplifier then sets the gate voltage of M3 such that it is biased in the saturation region. By sensing the differential voltage across the drains of M1 and M2, the amplifier balances the current source, i.e., $V_{DS1} = V_{DS2}$.

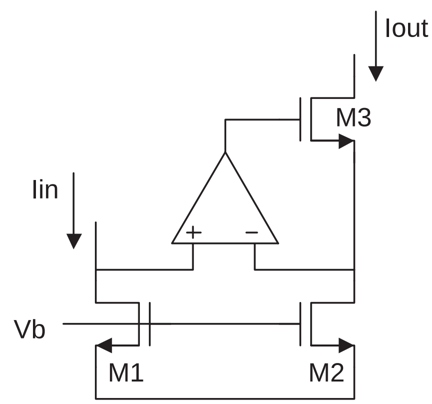

Figure 1: Schematic of the CMOS low voltage current source. M1 and M2 are biased in the linear region while the rest of the devices are biased in the saturation region.

To illustrate the merits of this current source, we will examine the input and output characteristics. Ideally, a current source has zero input resistance and infinite output resistance. While the input resistance of this current source is not zero, it is relatively low since the input transistor M1 is biased in the linear region. Thus, the input resistance is simply:

$$R_{in} = \frac{1}{\beta(V_{GS1} - V_T)} \tag{1}$$

where $\beta = K'(W/L)$. Typically the input resistance will be in the range of kΩ. Because M1 is biased in the linear region, the input voltage is very low, typically less than 0.1V.

The output resistance of this current source is amplified by the feedback amplifier and it is approximately:

$$R_{out} \approx A r_{ds3} \tag{2}$$

Type	$V_{o(min)}$	R_{out}	V_{in}	R_{in}
Simple	$V_{DS(sat)}$	$1/g_{ds}$	V_{GS}	$1/g_m$
H.S. Cascode	$2V_{DS(sat)}$	g_m/g_{ds}^2	$2V_{GS}$	$2g_m$
Low Voltage	$V_{DS(sat)}$	A/g_{ds}	0.1V	$\frac{1}{\beta(V_{GS}-V_T)}$

Table 1: Comparison of simple current mirror, high-swing cascode current mirror and the low voltage current mirror.

where A is the gain of the differential amplifier. Notice that the resistance of M2 does not contribute to the output resistance significantly since it is a relatively low value.

The minimum output voltage of the current source is determined by the saturation voltage of M3, i.e.,:

$$V_{out(min)} \approx V_{DS(sat)3} \tag{3}$$

The voltage across M2 also contributes, but in this case it is typically less than 0.1V and therefore negligible.

This current source is compared to the simple current source and the high-swing cascode current source in Table 1. The input voltage of the low voltage current source is much lower than both the simple and the high-swing cascode current sources. The output voltage requirement is of the same order as the simple current source. However, the output resistance is similar to the cascode current source.

The schematic shown in Fig. 1 is similar to the regulated-gate cascode (RGC) current source [1,2]. The primary difference between this low voltage current source and the RGC current source is that instead of a differential feedback amplifier, a single-ended feedback amplifier is used. Additionally, all the devices in the RGC current source are biased in saturation.

3 Implementation Issues

The actual implementation of this current source is shown in Fig. 2. The current mirror is made up of transistors M1-M3 and the amplifier consists of the remaining transistors. The amplifier is preceded by a p-channel level shifting circuit. This adjusts the dc voltage into the differential amplifier so that the devices can be biased in saturation. In the design of this current source, the input differential pair transistors were designed with a low excess gate voltage to reduce the offset. To reduce the mismatch, M1 and M2 were interdigitated in the layout. The circuit was implemented in a 2μ CMOS n-well process. The die photograph of two current mirrors is shown in Fig. 3. The measured I-V characteristics are shown in Fig. 4. The minimum output voltage swing is 0.2V. The measured output resistance is $11M\Omega$ and the measured input resistance is $1k\Omega$.

The feedback amplifier will be unstable unless it is compensated. Unfortunately the required compensation capacitance can be very large. In this design, it is placed from the gate of M3 to ground. By replacing the one-stage amplifier with a two-stage amplifier, the amplifier gain can be increased which increases the output resistance and a miller capacitance can be employed. The schematic of the current mirror with a two-stage amplifier is shown in Fig. 5. Designing this current mirror for the same current level, the output resistance increases from 11MΩ to 20MΩ.

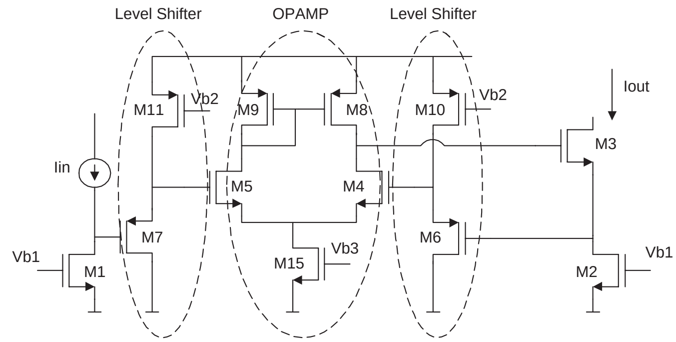

Figure 2: Schematic of the low voltage current source. M1 and M2 are biased in the linear region. M6 and M7 level shift V_{DS1} and V_{DS2} so that the differential input voltage is high enough for the amplifier transistors to be biased in saturation.

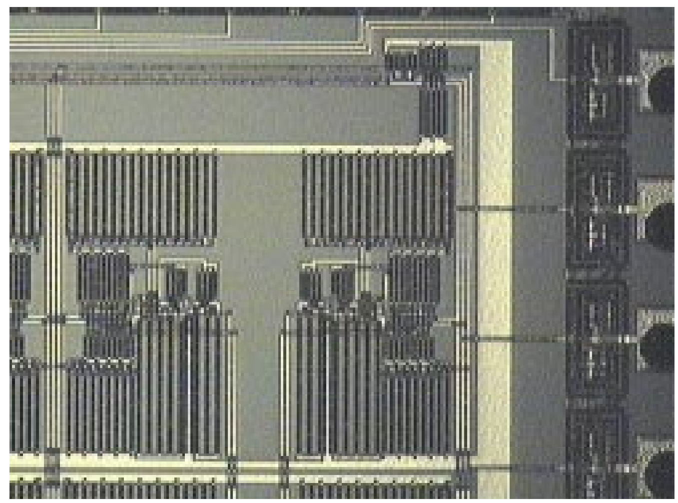

Figure 3: Die photograph of two CMOS low-voltage current mirrors. Each current mirror is designed for an input current of 80μA.

4 Design Example

To illustrate the merits of this low-voltage current source, a 1.8V folded-cascode operational amplifier has been designed, Fig. 6. The drains of the input transistors, M1 and M2, are connected to (or fold into) the drains of M3 and M4, respectively. The NMOS current mirror consisting of M7-M9 and A1 converts the differential signal into a single-ended output. The low-voltage current source is also used to generate the tail current. It increases the common-mode rejection ratio while still allowing for a wide common-mode input range. The biasing of the transistors in the linear region (M3, M4 and M13) is provided by transistors M14 and M15. A similar circuit is used for generating Vbp.

Simulations in HSPICE verify that with a 1.8V power supply, the linear output swing of the amplifier is 0.2V to 1.6V, Fig. 7. The open loop gain of the amplifier is 50dB in a 2μ CMOS process, Fig. 8.

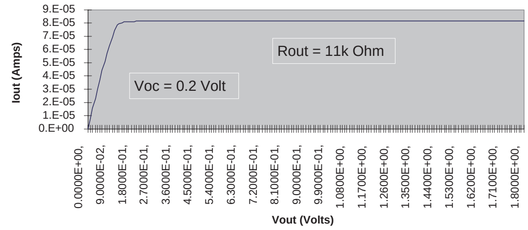

Figure 4: Measured I-V characteristics of the low voltage current mirror. The minimum output voltage is 0.2V and the measured output resistance is 11kΩ.

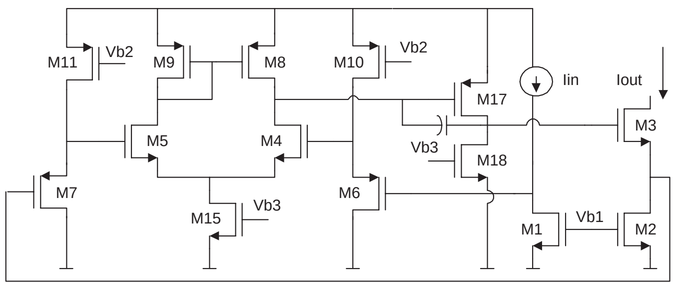

Figure 5: Schematic of the low-voltage current mirror (M1-M3) with a two-stage feedback amplifier.

5 Conclusion

A low voltage current source with an output resistance approaching that of a cascode current source has been designed, fabricated and tested. It has a minimum input voltage range of approximately 0.1V and a minimum output voltage range down to 0.2V. Its use has been demonstrated by designing a 1.8V folded-cascode operational amplifier that has an open loop gain of 50dB.

REFERENCES

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[2] E. Sachinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 289-298, Feb. 1990.

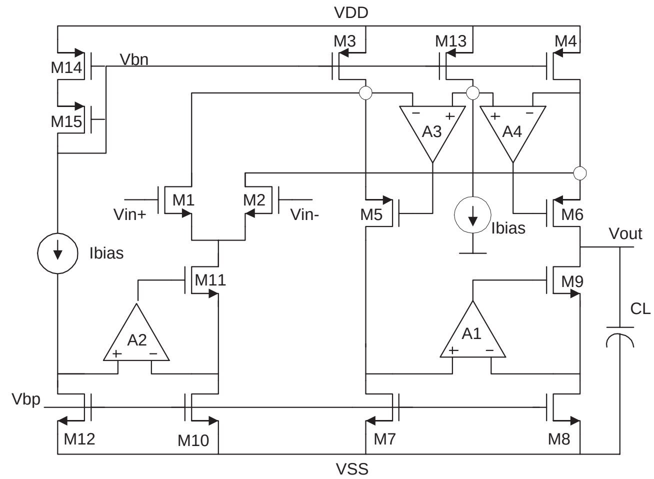

Figure 6: Folded-cascode operational amplifier using the low voltage current mirror. The amplifier operates with a single 1.8V power supply.

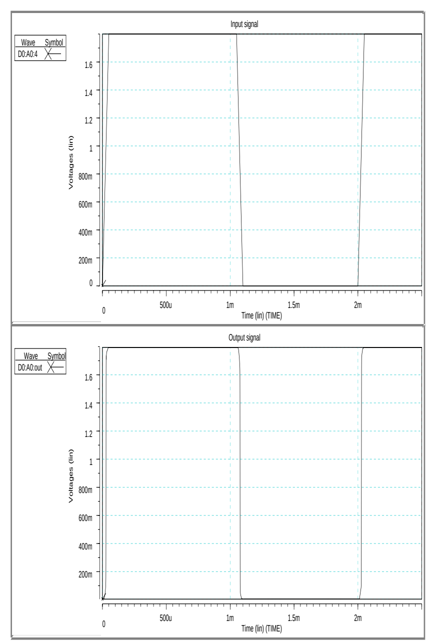

Figure 7: Input voltage and output voltage swing for the low voltage folded-cascode operational amplifier.

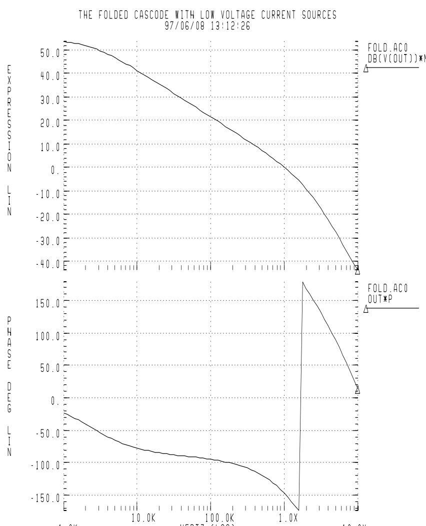

Figure 8: AC response for the low voltage folded-cascode operational amplifier.