Charge-Pump Assisted Low-Power/Low-Voltage CMOS Opamp Design

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I. Abstract

Low-voltage/low-power requirements have become essential considerations in modern mixed-signal designs. In this paper, we present a 1.8 V multi-stage opamp designed using a standard 0.6 μm N-well CMOS process. The opamp designs include a new high efficiency DC-DC converter used in a low-voltage frequency compensation configuration that tracks process, temperature, and supply voltage variations and enables accurate pole-zero cancellation. Low-power operation in comparing passive and active g_m feedforward compensation techniques. An automatic threshold calibration scheme is also described.

II. Introduction

It is difficult to design low-voltage cascoded amplifiers using standard high-V_T CMOS technology. Two- and multi-stage amplifier configurations employing Miller compensation are now considered in many low-voltage designs. Such amplifiers often employ process-tracking RC frequency compensation wherein a MOS transistor with a high gate bias voltage is used to implement the compensation resistance [3]. In low-voltage designs, its required gate bias voltage often exceeds the opamp supply voltage [4]. In the next section, we highlight strategies to achieve the required gate bias voltage through the use of high-efficiency DC-DC converters in a two-stage opamp. In Section 4, the design of a low-voltage low-power four-stage nested Miller opamp is described.

III. DC/DC Converter

The Dickson charge-pump DC-DC converter [1] is shown in Fig. 1(a), and a recently reported version with improved conversion efficiency [2] is shown in Fig. 1(b). In Fig. 1(c), we show our new design which according to HSPICE simulations has higher conversion efficiency and lower clock feedthrough voltage ripple than previous implementations. To provide first-order clock-feedthrough cancellation, we use a dual version of the three-stage charge pump circuit of Fig. 1(c) to drive the MOS transistors in the RC compensation networks. Fig. 2 shows a simple single-ended two-stage opamp incorporating this technique wherein the required resistor gate voltage ($2V_{GS}$) is obtained from a replica diode voltage increased using the dual charge pump.

A novel voltage calibration circuit has been designed to maximize opamp input common-mode range in the presence of threshold voltage variations. As shown in Fig. 3, the idea is to utilize a negative feedback control loop to

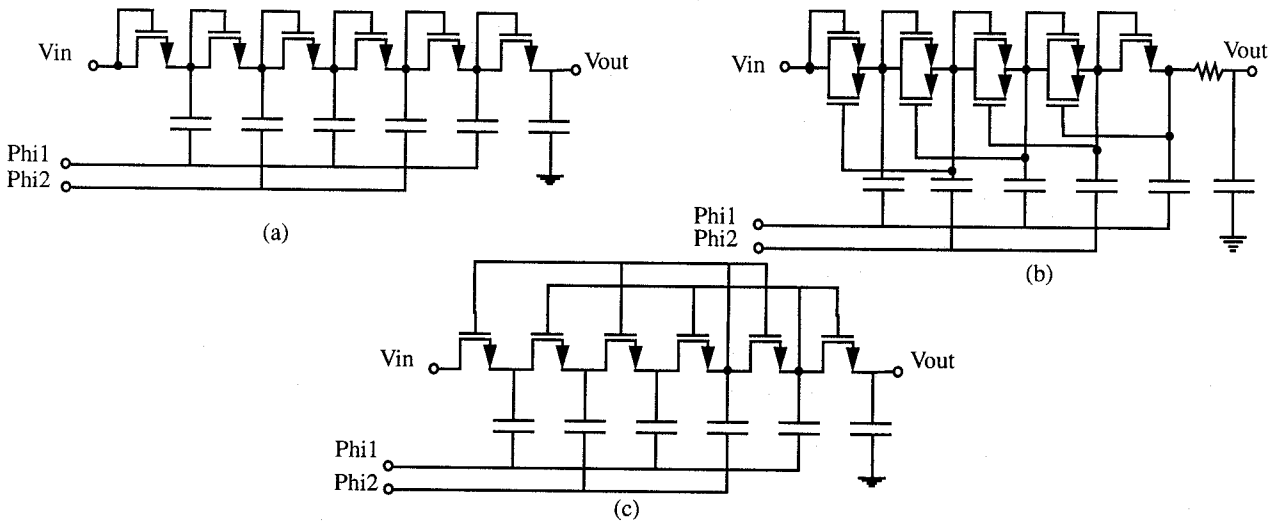

Fig. 1. (a) Dickson, (b) Wu, and (c) new charge-pump DC-DC converter circuits.

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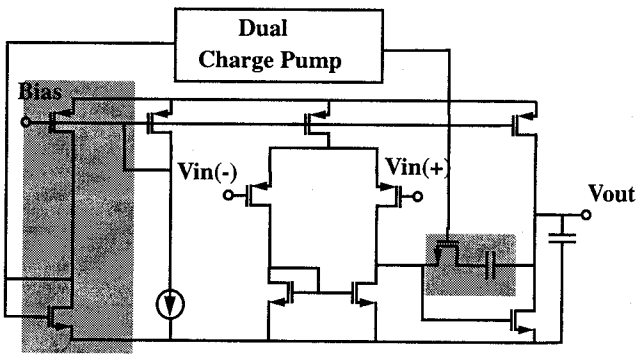

Fig. 2. Two-stage opamp with tracking compensation.

adjust the input-pair backgate voltage to minimize the threshold voltage while being careful to avoid latch-up. Using this scheme, HSPICE simulation results show a 145 mV increase in the input common-mode range with a 1.2 V power supply voltage. In reducing the threshold voltages electronically, the PMOS V_{SB} is controlled to be less than 400 mV to avoid strongly forward-biased junctions. The complete schematic for the single-ended two-stage opamp is shown in Fig. 3.

IV. Multi-Stage Nested-Miller Opamps

In low-voltage environments, multi-stage cascades of low-gain stages is one way to obtain high gain opamps as indicated in Fig. 4 [5][6][7]. One possible design uses a four-stage configuration with a fully-differential input stage followed by three pairs of common source amplifiers as shown in Fig. 5. In this topology, multi-stage capacitance compensation is needed to obtain a stable operational amplifier; zeros must be introduced to cancel non-dominant poles near the unity-gain frequency. Rather than using conventional active g_m feedforward compensation, power dissipation is reduced by introducing active resistors in series with the Miller compensation capacitors. The active resistors are biased using the technique described above to assure accurate pole-zero cancellation in the presence of process, temperature and supply voltage variations. We have achieved 110 dB dc gain, a 21 MHz unity-gain bandwidth, a unity-gain phase margin of 68 degrees, and a high slew rate of 40V/μs. Power dissipation is 19mW at 2V with a load capacitance of 10pF.

V. References

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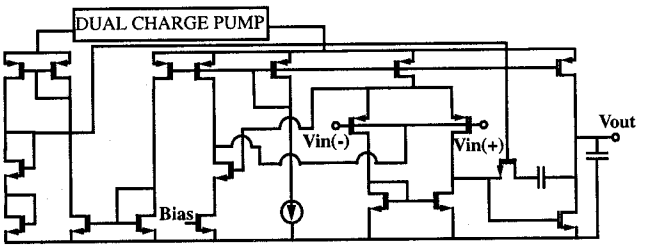

Fig. 3. Two-stage opamp with an alternative charge-pump compensation scheme..

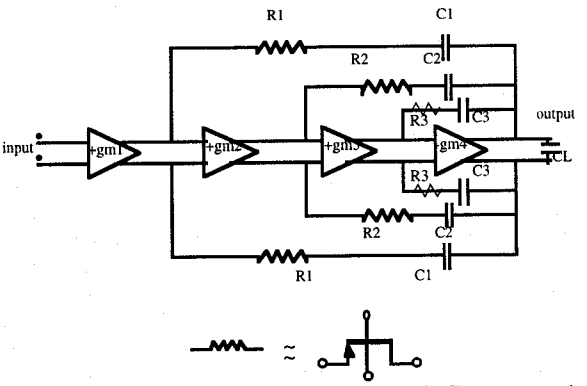

Fig. 4. Four-stage opamp with nested Miller R-C compensation network

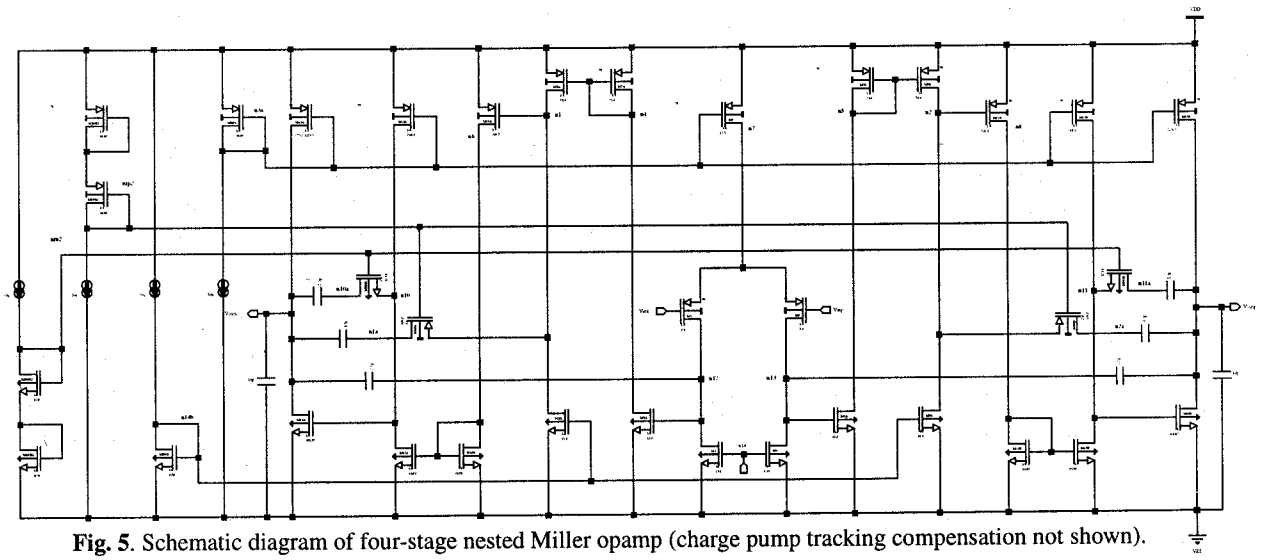

Fig. 5. Schematic diagram of four-stage nested Miller opamp (charge pump tracking compensation not shown).