Test Generation for Comprehensive Testing of Linear Analog Circuits Using Transient Response Sampling

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Abstract

The problem of testing analog components continues to be the bottleneck in reducing the time-to-market of mixed-signal ICs. In this paper, we present a test generation algorithm for implicit functional testing of linear analog circuits using transient response sampling. Each specification of the circuit under test (CUT) imposes bounds on individual parametric deviations under the single fault assumption. These bounds are mapped on to "acceptable" ranges of measurements of the transient response of the CUT at various sample points using time domain sensitivity calculations. Any circuit that "passes" the applied test is also guaranteed to meet its specifications. The simplicity of the test waveform, reduced test generation time and test time show that this testing method is a good alternative to existing testing schemes.

1. Introduction

With recent advancements in DSP and wireless communication, mixed-signal ICs are being used aggressively in industry. Nevertheless, testing continues to be the bottleneck in reducing time-to-market of mixed-signal ICs. The current practice in industry is to measure the circuit specifications and pass or fail the CUT based on the results of the tests. This test process is inherently expensive. In this paper we present an implicit test generation algorithm assisted by fast sensitivity computation which ensures that if the CUT "passes" the generated tests, then it implicitly satisfies all its specifications. Thereby, a large reduction in test cost is achieved.

In [1] the authors discuss an algorithm for efficient *functional testing* of analog ICs. In [2-4], it has been shown that many catastrophic faults can be detected by DC testing. Sinusoidal testing has been addressed by many researchers [5-7] and involves evaluating the steady state response of the CUT for fault detection. The transient testing schemes presented in [8-11] are more efficient in comparison to sinusoidal testing schemes. In [12], a set of DC and low frequency sinusoids are used for *implicit functional* testing. Pan and Cheng in [13], propose an innovative testing scheme for linear analog circuits using transient response measurements. However, their algorithm needs to be trained on large sets of failure data requiring many circuit simulation steps. The implicit functional testing scheme we present in this paper uses sensitivities to derive efficient transient tests. The test generator is assisted by a fast fault simulator, FLYER [14] which further speeds up the test generation process. Moreover, the proposed testing scheme is easily amenable to low-cost BIST [15]. In the following, we first give an overview of the test generator and then present details of the proposed algorithm.

2. Overview of the test generator

We first state the problem to be solved. Given the netlist of the circuit and its specifications, we desire to compute the optimal test stimulus and the times at which the transient response of the CUT is to be sampled for highest fault detectability and yield. This has to be done in such a way so as to ensure, as best as possible, that if the CUT "passes" the tests, then all its specifications are also implicitly met and vice versa. We also want to minimize the test time and the number of times the output is sampled. Figure 1 shows an overview of the proposed test generator. First, the circuit specifications are related to the maximum allowed deviations of circuit parameters under fault using the MIST PROFIT [16] software. The circuit netlist is preprocessed to form the adjoint circuit [17, 18]. In order to simulate the CUT and its adjoint using FLYER [14], we extract the state matrix of the circuit from its netlist. Methods for computing the state matrices from tree link [19] analysis and nodal analysis techniques [20,21] have been investigated in the past. In this work we use a simple method based on element stamps to construct the state matrices from the nodal admittance matrix. Stated concisely, specific row elimination operations are applied to a modified nodal admittance matrix of the CUT, to obtain its state variable representation. Using the respective state matrices, FLYER can simulate the CUT and its adjoint very fast and compute the time domain sensitivities of the parameters to the circuit output using the adjoint method [18]. The optimizer in the test generation program uses the sensitivities to determine the optimum test stimulus waveform and sample points for transient testing. The test generation algorithm is described in detail in the next section.

3. Test generation algorithm

For mapping the specifications to the worst case deviations (see Figure 1) in the circuit parameters, consider a circuit with q specifications, $P = [p_1, p_2, ..., p_q]$. Assume that the acceptable values of specifications p_k, $1 \le k \le q$, lie in the range p_k-Δp_k and p_k+Δp_k. The vector $\Delta \boldsymbol{P} = [\Delta p_1 \ \Delta p_2 ..... \Delta p_q]$ is specified by the circuit designer or design customer. If the measured

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value of p_k is outside the above range, then p_k is said to be *violated*.

Now consider the l circuit parameters, $C = [c_1, c_2, ..., c_l]$. We want to compute the smallest deviation Δc_j in the value of the parameter c_j, $1 \le j \le l$, that is always guaranteed to violate at least one of the specifications p_k, $1 \le k \le q$. However, while performing this calculation, one must take into account the fact that due to manufacturing process variations, the value of c_j is not exact and can only be predicted to lie in the range $(c_j - \delta c_j, c_j + \delta c_j)$. δc_j is said to be the *tolerance* in the value of c_j. Let $s_{c_j}^{p_k}$, $1 \le k \le q$, $1 \le j \le l$, be the first order sensitivity of the specification p_k to the parameter c_j. Let ε_{jk} be the deviation in the value of parameter c_j from the nominal that is guaranteed to violate specification p_k in the presence of tolerances in other parameters. This is computed using Equation 1. In order to compute Δc_j we need to calculate the minimum of the allowed deviations (ε_{jk}) over all specifications. This is computed using Equation 2.

$$|\varepsilon_{jk}| = \frac{\sum_{\substack{i=1 \\ i \ne j}}^{l} \left| \delta c_i \cdot S_{c_i}^{p_k} \right| + |\Delta p_k|}{\left| S_{c_j}^{p_k} \right|} \quad (1)$$

$$|\Delta c_j| = minimum(|\varepsilon_{j1}|, ..., |\varepsilon_{jq}|) \quad (2)$$

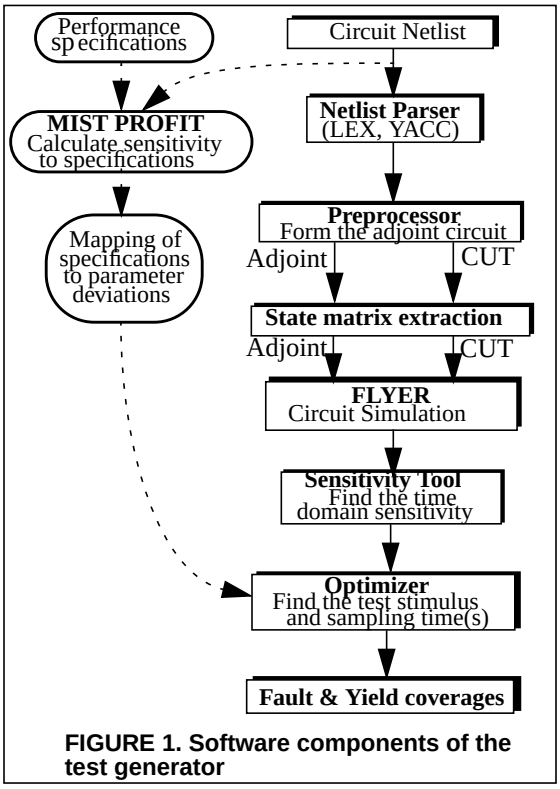

FIGURE 1. Software components of the test generator

3.1 Formulation of cost function for optimization

Assume that a test stimulus is given and our goal is to evaluate how good the supplied stimulus performs as a test for the CUT. We will use the following analysis to formulate a cost function for test generation and then later show how this cost function is used to drive the search for the optimal test stimulus and sample times (see optimizer in Figure 1).

Let the measurement of the transient response of the CUT at time t_k for the nominal value of c_j be given by M_{jk} (note that M_{jk} can be a voltage or current value). In the presence of tolerances in all the components c_i, $i \ne j, 1 \le i \le l$, and in the presence of the deviation Δc_j in the value of component c_j that is guaranteed to violate at least one specification of the CUT, we desire to compute $|\Delta M_{jk}|$, the largest possible change in the measurement M_{jk}. Equation 3 describes how $|\Delta M_{jk}|$ is computed. The range of "acceptable" measurements $(M_{jk} - |\gamma_k|, M_{jk} + |\gamma_k|)$ is determined by $|\gamma_k|$ which is computed as given in Equation 4.

$$|\Delta M_{jk}| = \sum_{\substack{i=1 \\ i \ne j}}^{l} \left| s_{c_i}^{M_{jk}} \cdot \delta c_i \right| + \left| s_{c_j}^{M_{jk}} \cdot \Delta c_j \right| \quad (3)$$

$$|\gamma_k| = maximum(|\Delta M_{1k}|, ..., |\Delta M_{lk}|) \quad (4)$$

Note that the nominal values of the measurement M_{jk} for all $1 \le j \le l$, are identical and correspond to the fault-free measurement value defined as Mff_k. Let the measured value of the response at time t_k during test be given by $Mtest_k$. If $Mtest_k < Mff_k - |\gamma_k|$ or $Mtest_k > Mff_k + |\gamma_k|$, then under the single fault assumption, it is implicitly guaranteed that there exists a faulty parameter value c_1 or c_2 or.... or c_l that causes a circuit specification to be violated. Let the value of c_j under fault be given by c_j'. With every sample time t_k and every parameter c_j, $1 \le j \le l$, we associate a deviation $|\Delta ctest_{jk}|$ such that whenever

$$c_j' < c_j - |\Delta ctest_{jk}| \text{ or } c_j' > (c_j + |\Delta ctest_{jk}|),$$
$$Mtest_k < Mff_k - |\gamma_k| \text{ or } Mtest_k > (Mff_k + |\gamma_k|).$$

Simply stated, any deviation of c_j larger than $|\Delta ctest_{jk}|$ is *guaranteed* to cause $Mtest_k$ to "fail". Note that this must hold in the presence of tolerances in all the components $c_i, 1 \le i \le l, i \ne j$. Such a value of $|\Delta ctest_{jk}|$ is computed using Equation 5. Suppose we have r sample points. Then the smallest $|\Delta ctest_{jk}|$ that will cause one of the r measurements $Mtest_k$, $1 \le k \le r$ to fail ($|\Delta ctest_j|$) is given by Equation 6. The test waveform and sampling points need to be selected in such a way so as to minimize the difference between the detectable worst case deviation in components due to the derived test set and those derived from the specifications. For generating the test we define a normalized cost function as given in Equation 7. The test waveform parameters (pulse

width for a rectangular pulse, rise time for a ramp input etc.) can be optimized using the cost function in (7). The test generation procedure is illustrated with pulse input waveforms.

$$|\Delta ctest_{jk}| = \frac{\sum_{i=1,\, i \neq j}^{l} \left|\delta c_i \cdot s_{c_i}^{Mff_k}\right| + |\gamma_k|}{\left|s_{c_j}^{Mff_k}\right|} \quad (5)$$

$$|\Delta ctest_j| = minimum(|\Delta ctest_{j1}|, \ldots, |\Delta ctest_{jr}|) \quad (6)$$

$$Cost = \sum_{j=1}^{l} \frac{(c_j)^2}{(|\Delta c_j| - |\Delta c_{testj}|)^2} \quad (7)$$

Figure 2 shows the pulse waveform. The test generation algorithm selects an optimum pulse width PW_i and a sampling time t_i through exhaustive search over the range $0 \le PW_i \le Tmax_1, 0 \le t_i \le Tmax_2$ where $Tmax_1$ and $Tmax_2$ are the limits imposed by the simulator FLYER [14]. The algorithm for test generation is given in Algorithm *FindOptimumTest* shown below. The two inner *while* loops find the optimum PW_i and t_i. The outer *while* loop adds the pulse and sampling time to the generated test set.

Input: Maximum test time
Procedure *FindOptimumTest*
total test time = 0, cost = 0, Set of pulses and sample times={Φ}
while *((total test time < Maximum test time) or (no significant improvement in cost)*
  while *(PW_i < $Tmax_1$)*
    while *(SampleTime < $Tmax_2$)*
      Calculate Cost using Equation 7
      if *(there is significant improvement in cost)*
        Store PW_i and t_i
      end if
    end while
  end while
  Add PW_i and t_i to the set of pulses and sample times
end while
Print test waveform, Sample time points, thresholds.

Algorithm FindOptimumTest

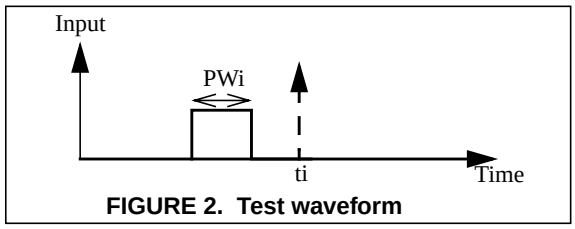

FIGURE 2. Test waveform

3.2 How good is the generated test?

The quality of the generated test is measured by fault and yield coverages. Yield coverage is defined as the ratio of the number of good circuits that pass the test to the actual number of good circuits. In our approach we are testing for worst case parameter deviations, hence we will never be rejecting a good circuit. Thus we always get 100% yield coverage. Fault coverage is defined as the ratio of the number of faulty circuits detected by the test to the total number of faulty circuits. In order to estimate the fault coverage of the generated test, we divide the faults into two categories. 1) catastrophic faults 2) parametric faults. As we detect all the faults which cause a deviation of more than $|\Delta ctest_j|$, we have 100% fault coverage of catastrophic faults. The fault coverage of parametric faults is computed by injecting a large number of random parameter variations (assuming independent normal distribution of the parameters) into the CUT and checking whether the test detects the fault.

4. Test generation results

We discuss the results of test generation on a biquadratic low pass filter (Figure 3). Tolerances of the components were taken as 1%. The nominal values of a set of specifications of the filter and their allowed deviations from the nominal are shown in Table 1. Maximum allowed deviations of the circuit components imposed by the specifications are shown in Table 2. The generated test stimulus and the CUT response for the biquadratic filter are shown in Figure 4. The sampling points, nominal output of the fault free circuit and the maximum allowed deviations of the output for passing/failing the CUT are shown in Table 3. The values of $|\Delta ctest_j|$ for various parameters are listed along with that of $|\Delta c_j|$ in Table 2. All the faults which cause R1 to deviate more than 17.3% from its nominal value are detected by the test. However, if R1 deviates more than 11.05%, the circuit is faulty. Since the test generation algorithm is driven by the worst case situation we loose fault coverage for the deviation in R1 in the range [11.05%, 17.3%].

The parametric fault coverage of the derived test was estimated by simulating 1000 circuit instances (described in Section 3.2). The 3σ value for the parameters were taken as 1%. The estimated fault coverage was around 80% for parametric faults. Thus the overall fault coverage with catastrophic faults also taken into consideration, is greater than 80%. The overall test time for the sinusoidal testing scheme presented in [5] is approximately 60ms while our approach samples the output 4 times over a total test time of 5.29ms to achieve an overall coverage (yield + fault coverage) of 1.8. The impulse sampling technique presented in [13], takes 30 samples over a test time of 25ms to achieve an overall coverage of 1.9. The analysis presented here results in a reduced cpu time for test generation of around 200s compared to the method presented in [13] which takes 1400s of cpu time just for the Monte Carlo simulations alone.

5. Conclusion

We have presented a comprehensive test generation algorithm which derives the faults from the specifications and design tolerances of the CUT and generates very efficient tests. The simplified analysis approach presented reduces the overall test generation time as well as the testing time considerably over existing testing schemes. The next steps will involve incorporation of more realistic multiple fault models and extension of the test generation algorithm to handle practical non linear circuits as well.

Specifications	Nominal Value (P_j)	Allowed deviation (ΔP_j)
Bandwidth (Hz)	202.4	20.2
Maximum Gain	1.154	0.12
DC gain	1.0	0.1
Gain @ 150Hz	1.05	0.1
Fall Time (ms)	0.15	0.01

TABLE 1. Specifications of the filter

Parameter	$\|\Delta c test\|_j$ (%)	$\|\Delta c_j\|$(%)	Parameter	$\|\Delta c test\|_j$ (%)	$\|\Delta c_j\|$(%)
R1	17.3	11.05	R5	20.1	14
R2	36.5	14.4	R6	20.1	11
R3	20.7	14.0	C1	31	20.2
R4	20.1	14.0	C2	20.7	14

TABLE 2. Allowed deviations of the parameters

Test ID	Sampling Time (ms)	Nominal Output (mV)	$\|\gamma_k\|$ (mV)	Cost
1	0.82	-131.6	22.35	695
2	2.69	-551.15	79.51	913
3	4.13	-600.92	105.60	1353
4	5.29	-663.79	114.57	1470

TABLE 3. Test for biquadratic filter

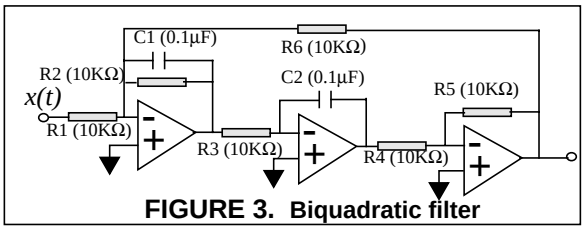

FIGURE 3. Biquadratic filter

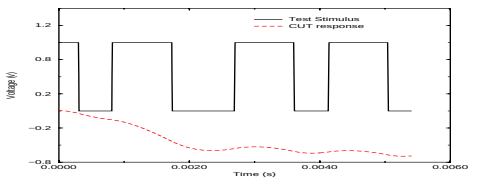

FIGURE 4. Test for biquadratic filter

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