Shaping A VLSI Wire to Minimize Elmore Delay

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Abstract

Euler's differential equation of the calculus of variations is used to determine the shape of a VLSI wire that minimizes Elmore delay. The solution is given as a power series whose coefficients are formulas involving the load-end wire width, the load capacitance, the capacitance per unit area, and the capacitance per unit perimeter. In contrast to an optimal-width rectangular wire, the RC Elmore delay of the optimally tapered wire goes to zero as the driver resistance goes to zero. The optimal taper is immune, to first order, to process variations affecting wire width.

1 Introduction

In a previous work [12] [13] Euler's differential equation of the calculus of variations was used to determine that, among all possible shapes, an exponential taper was optimal for minimizing the Elmore delay of a distributed-RC wire. This result was also discovered independently [4] using direct methods. In these works zero perimeter capacitance was assumed, so that the wire capacitance was due entirely to area capacitance. This assumption is justifiable for multichip modules, where wire width is much greater than wire thickness. However, minimum feature size has continually decreased in VLSI, to the point where minimum wire width is now smaller than wire thickness, and thus area capacitance is considerably less than perimeter capacitance for a minimum-width wire. At the same time, the smaller geometries yield transistors with greater drive current and less gate and source/drain capacitance, so that proper wire design becomes even more important. In this work we investigate the wire shaping problem under the assumption of positive perimeter capacitance.

2 Elmore delay

The Elmore delay of a linear network is defined [10] to be the first moment of the network impulse response. For example, if a unit impulse is applied to the input V_1 of Figure 1 at $t = 0$, the Elmore delay is defined as $\int_0^\infty tV_2(t)dt$, which is the t-coordinate of the center of gravity of the region under the impulse response $V_2(t)$. In the case of an RC ladder, it has been shown [17] that this is equal to the sum, over all the resistors, of that resistance times all its downstream capacitance. In Figure 1,

$$ED \equiv \int_0^\infty tV_2(t)dt = R_1(C_1 + ... + C_n) + R_2(C_2 + ... + C_n) + ... + R_nC_n. \quad (1)$$

For a given voltage threshold, the Elmore delay can be multiplied by appropriate constants to give upper and lower bounds [14] for the time that it takes an RC ladder output to cross the threshold, in response to a step input. Elmore delay has been shown [20] to be identical with group delay at zero frequency. It has been found empirically that if the input and output are at opposite ends of the network, the 50% step response delay is usually within 3% of 0.7533 times Elmore delay [20]. Another empirical study [3] found that optimization of interconnect according to an Elmore delay objective function leads to more nearly-optimal actual delay, than would be expected merely on the basis of the Elmore model accuracy. For these reasons, Elmore delay has been widely used to estimate delays in VLSI logic gates and interconnect [7] [21] [19] [15] [1] [22]. Whenever we use the term "delay" in this paper, we mean Elmore delay.

3 Euler's Differential Equation

A basic formulation of a calculus of variations problem is as follows [8]: We are given a real-valued function $F(x, y, z)$ of three real-valued arguments. When

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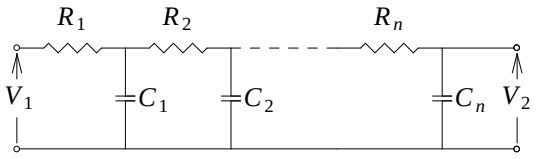

Figure 1: RC-Ladder.

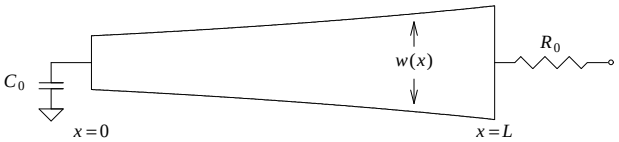

Figure 2: Distributed-RC Line.

y is replaced by a particular function of x, $u(x)$, and z by $u'(x)$, F becomes a function of x, and the integral

$$I = \int_{x_0}^{x_1} F(x, u(x), u'(x))dx$$

is equal to a particular real number.

The problem that the calculus of variations addresses is the following: Out of all functions $u(x)$ defined in the interval $[x_0, x_1]$ that have continuous first and second derivatives, find the one that yields the least possible value for I. In the elementary theory of maxima and minima of a differentiable function $f(x)$, the familiar necessary condition for the occurrence of a maximum or minimum at an interior point x of the domain of f is $f'(x) = 0$. In the calculus of variations an analogous necessary condition [11] was discovered by Leonhard Euler in 1736: If $u(x)$ is a function that yields a minimum for I, then u must necessarily satisfy *Euler's Differential Equation*:

$$F_u(x, u(x), u'(x)) = \frac{d}{dx} F_{u'}(x, u(x), u'(x)). \qquad (2)$$

4 Shaping a VLSI wire to Minimize Elmore Delay

It is assumed that a planar wire of length L is driven with resistance R_0, and drives a capacitance to ground of C_0 (Figure 2). The resistance per square is R_S and capacitance to ground is composed of two parts, area capacitance and perimeter capacitance. Capacitance per unit area is denoted by C_S. It is assumed that the wire taper is gradual enough that perimeter capacitance can be modeled as proportional to wire length. We will denote the proportionality constant by C_P. Since this constant includes both sides of the wire, it is 2 times what is usually referred to as perimeter capacitance. If the wire width at x is given by $w(x)$, the Elmore delay (1) is then

$$ED = R_0 \left(C_0 + C_P L + \int_0^L C_S w(x) dx \right) + \int_0^L \frac{R_S \left(C_0 + C_P x + \int_0^x C_S w(l) dl \right)}{w(x)} dx$$

or

$$ED = R_0(C_0 + C_P L) + \int_0^L R_0 C_S w(x) + \frac{R_S \left(C_0 + C_P x + C_S \int_0^x w(l) dl \right)}{w(x)} dx. \qquad (3)$$

If we define $u(x) \equiv \int_0^x w(l)dl$, then $u'(x) = w(x)$, and Euler's equation (2) for minimizing (3) is

$$0 = 2C_S(u'(x))^2 + C_P u'(x) - 2u''(x)(C_0 + C_P x + C_S u(x)). \qquad (4)$$

This differential equation can be solved with a power series as follows: Suppose that

$$u(x) = \sum_{n=0}^{\infty} a_n x^n. \qquad (5)$$

Due to the definition of $u(x)$, $a_0 = u(0) = 0$. a_1 is the width of the wire at $x = 0$, which we denote by the special name W_0. Substituting (5) into equation (4), we obtain the power series (6).

Since this series is identically zero for all x, each one of its coefficients must also be zero. Hence we can derive closed-form expressions for all of the a_n in terms of $W_0 = a_1$ as follows: The first coefficient is zero, which allows a_2 to be expressed in terms of $W_0 = a_1$. If we have closed form expressions for a_1 thru a_n, we can substitute them into the coefficient of x^{n-1}, then solve for a_{n+1}. In this way we can find the power series coefficients for $u(x)$. Differentiating this power series gives the power series (7) for $w(x)$.

We will denote by

$$E(W_0, C_0, C_P, C_S, x), \qquad (8)$$

or the *Elmore taper function*, the derivative $u'(x)$ of the solution $u(x)$ of (4) satisfying $u(0) = 0$ and $u'(0) = W_0$, whose power series is given by (7).

The ratio test stipulates that the radius of convergence of (5) is $\lim_{n\to\infty} |a_n/a_{n+1}|$. When $C_P = 0$, (7) becomes the power series of an exponential function ae^{bx} [13] [4], which converges for all x. For non-zero C_P, the term in a_n containing C_P^n is

$$\frac{(-1)(-3)(-5)\cdots(3-2n)C_P^n}{2^n n! C_0^n}$$

$$
\begin{aligned}
0 \;=\;& 2C_S{W_0}^2 + C_P W_0 - 4C_0 a_2 \\
&+\; 2(-C_P a_2 + 2C_S W_0 a_2 - 6C_0 a_3)x \\
&+\; (4{a_2}^2 C_S - 24C_0 a_4 - 9C_P a_3)x^2 \\
&-\; 4(-2C_S a_2 a_3 + 10C_0 a_5 + 5C_P a_4 + 2C_S W_0 a_4)x^3 \\
&-\; (20C_S W_0 a_5 - 4C_S a_2 a_4 - 6C_S {a_3}^2 + 35C_P a_5 + 60C_0 a_6)x^4 \\
&-\; 2(27C_P a_6 + 18C_S W_0 a_6 + 2C_S a_2 a_5 - 6C_S a_3 a_4 + 42C_0 a_7)x^5 \\
&+\; \ldots
\end{aligned}
\tag{6}
$$

$$
\begin{aligned}
w(x) \equiv u'(x) = \;& W_0 \\
&+ \tfrac{W_0(2C_S W_0 + C_P)}{2C_0}x \\
&+ \tfrac{W_0(4{C_S}^2{W_0}^2 - {C_P}^2)}{8{C_0}^2}x^2 \\
&+ \tfrac{W_0(8{C_S}^3{W_0}^3 - 4{C_S}^2{W_0}^2 C_P + 2C_S W_0 {C_P}^2 + 3{C_P}^3)}{48{C_0}^3}x^3 \\
&+ \tfrac{W_0(16{C_S}^4{W_0}^4 - 16{C_S}^3{W_0}^3 C_P + 8{C_P}^2{C_S}^2{W_0}^2 - 20C_S W_0 {C_P}^3 - 15{C_P}^4)}{384{C_0}^4}x^4 \\
&+ \tfrac{W_0(32{C_S}^5{W_0}^5 - 48{C_S}^4{W_0}^4 C_P + 48{C_S}^3{W_0}^3{C_P}^2 + 40{C_S}^2{W_0}^2{C_P}^3 + 210C_S W_0 {C_P}^4 + 105{C_P}^5)}{3840{C_0}^5}x^5 \\
&+ \ldots
\end{aligned}
\tag{7}
$$

and it is this term that seems to determine convergence: The power series converges for x in the region $[0, C_0/C_P]$. This is an intuitively satisfying result, since C_0 "outweighs" the perimeter capacitance only for x inside this interval. This region of convergence has also been observed empirically.

The power series for $w(x)$ has one parameter, W_0, that is not given by the original problem. The total Elmore delay, ED, can be expressed as a function of W_0 by substituting the power series for $u(x)$ and $w(x)$ into (3) and symbolically or numerically integrating. A golden section search [16] then finds the value of W_0 that results in minimum delay.

In the following examples, unless specified otherwise, parameters take on the values in Table 1. The values for C_S, C_P, and R_S are for the first metal layer of a 0.35-micron process. L is one-half the perimeter of a typical microprocessor [9]. R_0 and C_0 have been chosen to be approximately equal to the driving resistance and gate capacitance of a single 100x buffer. As we will see, the delay of an optimally tapered wire can be made arbitrarily small by making the driving buffer large and/or the load buffer small, but this is not realistic for quickly sending a combinational logic signal across a chip, since additional amplifying stages would then be necessary at one or both ends of the wire.

Figure 3 shows the wire converging to its optimal

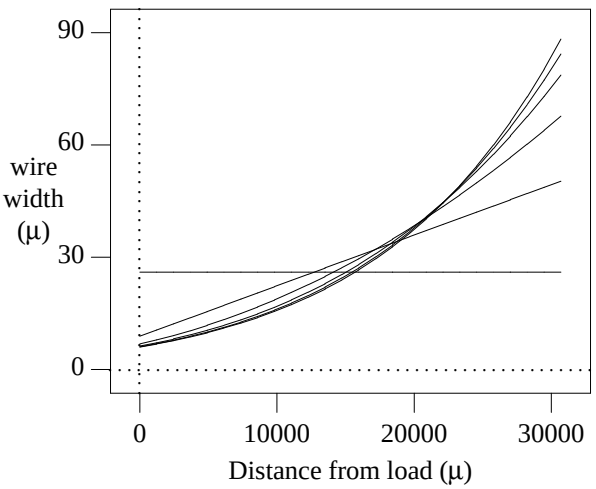

Figure 3: An Nth-order polynomial approximation of the power series of the optimal wire, for $N = 0, \ldots, 5$.

Param.	Value	Description
C_0	4×10^{-12} F	load cap.
C_S	$6.2 \times 10^{-17}\mathrm{F} \cdot \mu^{-2}$	area cap.
C_P	$11.9 \times 10^{-17}\mathrm{F} \cdot \mu^{-1}$	perimeter cap.
R_S	$0.09\Omega/\square$	sheet res.
R_0	12.5 Ω	driver res.
L	30700 μ	line length

Table 1: Wire parameters.

shape as the order N of the polynomial approximation increases from 0 to 5. For each value of N, W_0 is set to the value that minimizes delay. Thus when $N = 0$, W_0 is set to the optimal width for a rectangular-width wire.

Figure 4 shows the decrease in delay as the order N of the polynomial approximating the power series for $w(x)$ increases. $N = 0$ (optimal-width rectangular wire) is significantly slower than the others, but there is no significant decrease for order greater than 3.

Figure 5 shows the effect on the optimal taper as C_P grows in equal increments from zero to the value in Table 1. When $C_P = 0$, the optimal taper is exponential, so the taper is a straight line on this log scale. When $C_P > 0$, the width at the load end grows faster than the original exponential curve. But as the wire becomes wider toward the driver end, area capacitance once again dominates over perimeter capacitance, and the wire grows in an exponential manner.

Figure 6 compares the delay of an optimal-width rectangular wire and the optimal taper as R_0 ranges from 2.5 to 80 Ω. As R_0 gets smaller, the savings of the optimal taper over the optimal-width rectangular wire grows in absolute magnitude as well as in percentage.

The data for Figure 7 were also generated by varying R_0 from 2.5 to 80 Ω, but the total capacitance of each wire is plotted, instead of R_0. This graph thus shows the delay vs. power tradeoff that is offered by the optimal taper, as contrasted with the optimal-width rectangular wire. We can see that all the points on the curve for the optimal-width rectangular wire are *inferior* — At a given power, the optimal Elmore taper can always achieve less delay, and for a given delay can achieve less power.

5 Reducing RC Elmore Delay Below Any Given Amount by Tapering

The laws of physics dictate that signal velocity in a conductor, which is due to distributed inductance and capacitance, cannot be greater than the speed of light

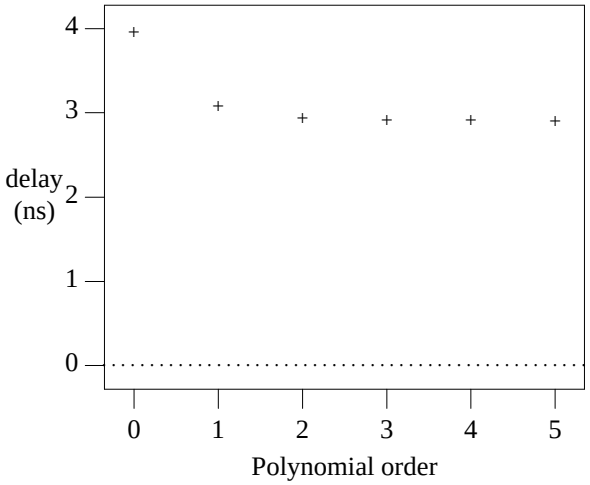

Figure 4: Delays for the 6 wires of the previous figure.

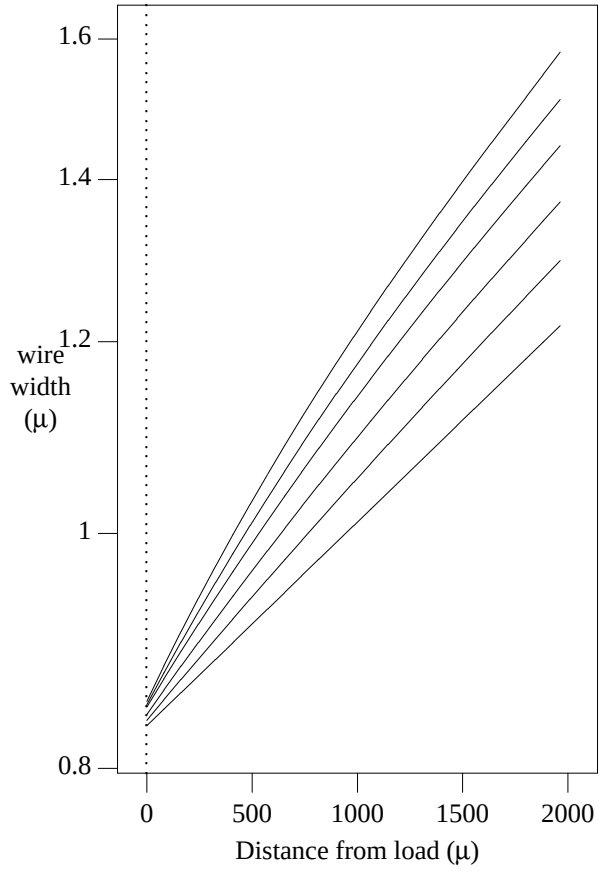

Figure 5: Plotted on a log scale, the shapes of optimal wires as C_P grows in equal increments from zero (straight line) to its value in a representative 0.35-micron process. To accentuate the non-exponential growth when $C_P > 0$, this example departs from the values of Table 1 as follows: $C_0 = 0.26 \times 10^{-12}$F, $L = 2000\mu$, and $R_0 = 375\Omega$

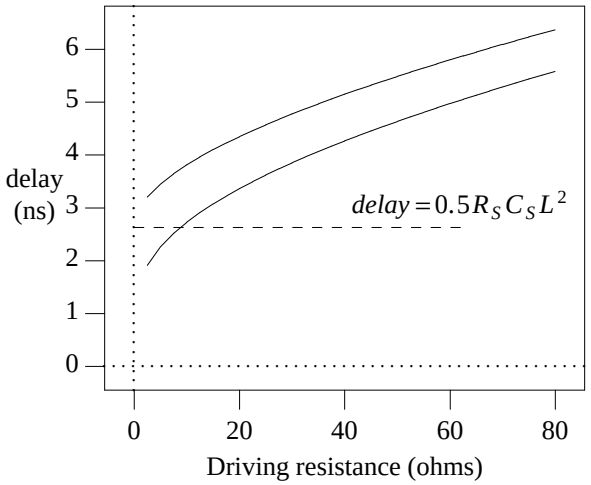

Figure 6: Delay as a function of R_0 for optimal-width rectangular wire (top line) and optimally-tapered wire (bottom line). The delay of the optimal-width rectangular wire cannot be less than $\frac{1}{2}R_SC_SL^2$.

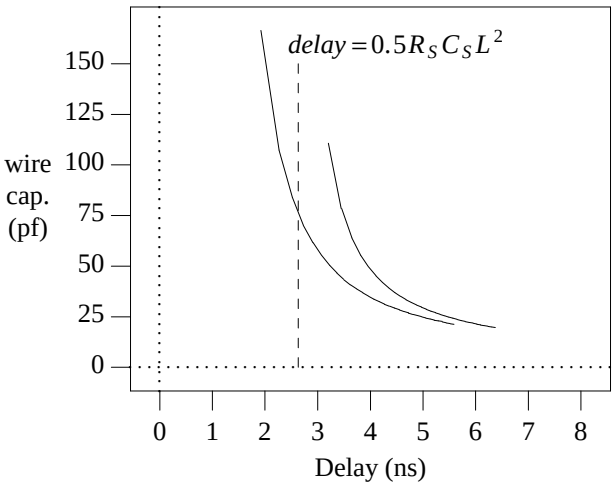

Figure 7: Delay-capacitance curves for optimal-width rectangular wire (right line), which approaches the $\frac{1}{2}R_SC_SL^2$ asymptote and optimally-tapered wire (left line).

divided by $\sqrt{\epsilon}$, where ϵ is the dielectric constant of the surrounding material. Aluminum wires in VLSI, however, are so thin that their RC delay far exceeds their LC delay. Therefore we have much room for decrease of delay within the RC model before LC considerations invalidate the assumptions made in that model. We will prove that in contrast to the rectangular wire, which has an intrinsic RC delay that cannot be reduced, no matter how much R_0 is reduced, the RC delay of an optimally tapered wire can be reduced below any given positive threshold, by driving it with a sufficiently low R_0 (while keeping C_0 fixed) and tapering accordingly. Of course this is not free; We must use more power for the larger wire and the smaller R_0. Also, as we have seen, this is not necessarily a practical method for send combinational signals, since it requires enlarging the transmitting buffer relative to the receiving buffer. But in cases where we might be willing to employ a large transmitting buffer, such as in a clock driver, the delay might be reduced so as to approach the LC limit. Microprocessor clock drivers [9] have had values of R_0 lower than 0.1Ω.

It has been demonstrated [18] that the performance of multi-chip module transmission lines can be improved by tapering. By using "just enough" tapering, the delay is reduced nearly to its LC time-of-flight minimum, while at the same time retaining enough resistance to effectively damp ringing.

In order to demonstrate that RC Elmore delay can be reduced below any given amount by tapering we will first consider the case $C_P = 0$, then use this to prove the same result when $C_P > 0$.

5.1 $C_P = 0$

In [13] it was demonstrated that when perimeter capacitance is zero, the optimal taper is

$$w(x) = \frac{2C_0}{C_SL}W\left(\frac{L}{2}\sqrt{\frac{R_SC_S}{R_0C_0}}\right)e^{2W\left(\frac{L}{2}\sqrt{\frac{R_SC_S}{R_0C_0}}\right)x/L}. \tag{9}$$

This can be written in terms of the Elmore taper function as

$$w(x) = E\left(\frac{2C_0}{C_SL}W\left(\frac{L}{2}\sqrt{\frac{R_SC_S}{R_0C_0}}\right), C_0, 0, C_S, x\right).$$

In these expressions W is the inverse of the function $f(x) = xe^x$. W satisfies the equations $W(x)e^{W(x)} = x$, $W(xe^x) = x$, $W(0) = 0$, and $W'(0) = 1$. $W(x)$ grows like $\log(x)$ as x goes to infinity. The delay for

the optimal shape (9) is

$$\frac{R_S C_S L^2 \left(1 + 2W\left(\frac{L}{2}\sqrt{\frac{R_S C_S}{R_0 C_0}}\right)\right)}{4W^2\left(\frac{L}{2}\sqrt{\frac{R_S C_S}{R_0 C_0}}\right)}. \qquad (10)$$

Note that as R_0 goes to zero, (10) goes to zero, and the capacitance of the optimally-tapered wire goes to infinity.

By contrast, if the wire has constant width K, the delay is

$$R_0 C_0 + KLR_0 C_S + \frac{L}{K} R_S C_0 + \frac{1}{2} R_S C_S L^2.$$

Setting $K = \sqrt{\frac{R_S C_0}{R_0 C_S}}$ in this expression gives the minimum delay that can be achieved by adjusting the width of a constant-width wire:

$$R_0 C_0 + 2L\sqrt{R_0 C_0 R_S C_S} + \frac{1}{2} R_S C_S L^2.$$

Notice that no matter how hard we drive the rectangular wire, its delay is always greater than $\frac{1}{2} R_S C_S L^2$.

5.2 $C_P > 0$

In the case $C_P > 0$, we can prove that the RC delay can be reduced below any given positive value ϵ, no matter how small, by reducing to the case $C_P = 0$ as follows: Remove all the perimeter capacitance from the sides of the wire, and add it at the load end. Now we have a problem with zero perimeter capacitance and a fixed load capacitance (now equal to $C_0 + C_P L$), which is the problem form addressable by the previous section. Thus there is an exponential taper which reduces the delay for this configuration below ϵ. Keeping this exponential taper fixed, we redistribute the $C_P L$ part of the load back to the sides of the wire. This can only reduce the delay. Finally we change the taper from exponential to the optimal Elmore taper function that minimizes the delay with consideration of the perimeter capacitance. Since this is the optimal taper, its delay must be less than the previous exponential taper, and thus is less than ϵ. This is illustrated in Figures 6 and 7, where the delay of the optimally-tapered wire, but not the rectangular wire, can be made less than $\frac{1}{2} R_S C_S L^2$.

6 Optimal Taper Delay is First-Order Immune to Wire Width Variations

Fundamental to the derivation of Euler's equation is the condition that the integral being minimized must be stationary with respect to variations in the candidate function $u(x)$. (Thus the name *calculus of variations*. In this case we might call it the calculus of *process* variations.) In other words, we suppose that the optimal function $u(x)$ is perturbed by an error function $\eta(x)$, scaled by ϵ to produce $u(x) + \epsilon\eta(x)$. If we then regard the functions u and η as fixed, and ϵ as variable, the value of the functional

$$I = \int_{x_0}^{x_1} F(x, u(x) + \epsilon\eta(x), u(x)' + \epsilon\eta'(x))dx$$

becomes a function of ϵ, and the fact that $u(x)$ gives a minimum for I implies that the perturbed function $u(x) + \epsilon\eta(x)$ must have a minimum at $\epsilon = 0$. Therefore it must be the case that

$$\frac{dI}{d\epsilon} = 0. \qquad (11)$$

Equation (11) is the starting point from which Euler's differential equation is derived, and in our case expresses the condition that at the optimal wire shape, the first-order variation of delay with respect to any wire-width variation is zero. In more practical terms, this means that if the optimal wire shape acquires a small bump (or narrowing) within any section along its length, then the extra delay caused by the bump capacitance, times the upstream resistance, is almost exactly cancelled by the decrease in delay due to the lowered resistance of that section, times all the downstream capacitance. Another practical consequence is that the discretization of the optimal wire taper, which is a continuous function, to multiples of the basic lithography quantum (which is 0.02 micron in the case of the representative 0.35-micron process) will have insignificant affect on delay.

7 Future Directions

The present work gives a power series solution with one undetermined coefficient (W_0) for the optimal wire width function that minimizes Elmore delay under a model that includes perimeter capacitance. Recently, using similar formulations, closed form solutions with two undetermined coefficients have been discovered for the optimal width function [5] and for its inverse [2]. These solutions reveal an interesting property of the optimal taper: If perimeter capacitance grows large relative to area capacitance at the load end of the wire, then the optimal shape converges to a square root function.

Although we have found the optimum, we have not answered the question of how much better the optimum is, compared to current typical practice. The improvement needs to be quantified for various conditions in current and foreseeable technologies, especially when optimally tapered wires are used in conjunction with other methods for performance enhancement. In a VLSI chip, the availability of repeater buffers may lessen the need for tapering. On the other hand, tapered wires might prove instrumental in new applications, such as we saw in their use for avoiding both dispersion and ringing in MCM traces [18].

There are many directions in which the current work might be generalized. First of all it should be possible to handle multiple-segment wires, in which each segment is on a different level, and so has different capacitance and resistance parameters. A minimum and maximum width for each level [4] can also be incorporated. Another generalization would allow networks that are trees [6], as opposed to the point-to-point connections of the current work. All of these problems are greatly simplified by the fact that the optimal taper of a given subsegment is affected by its upstream and downstream taper only insofar as these tapers affect the total upstream resistance and the total downstream capacitance, respectively. The calculus of variations is able to handle, with Lagrange multipliers, multiple-criterion optimization. It should be possible, for example, to jointly minimize both delay and power by placing a constraint on one and minimizing the other. Also, wire tapering should be combined with other kinds of optimization, such as transistor sizing, retiming, clock skew, logic optimization, placement and routing to obtain better results than can be had by performing these optimizations separately.

Appendix

This appendix gives more detail on the derivation in [13] of the formula for the optimal exponential taper when $C_P = 0$. In that paper, in the first column of page 1021, setting $ED'(c) = 0$ gives

$$L/2 - \frac{2R_0C_0R_SC_SLe^{2R_SC_SL/c}}{c^2} = 0,$$

which can be manipulated into the form

$$\frac{L}{2}\sqrt{\frac{R_SC_S}{R_0C_0}} = \frac{LR_SC_S}{c}e^{LR_SC_S/c}.$$

Now note that the right-hand side is of the form xe^x. Thus we can apply W() to both sides, and use $W(xe^x) = x$, giving

$$W\Big(\frac{L}{2}\sqrt{\frac{R_SC_S}{R_0C_0}}\Big) = R_SC_SL/c,$$

or

$$c = \frac{R_SC_SL}{W\Big(\frac{L}{2}\sqrt{\frac{R_SC_S}{R_0C_0}}\Big)},$$

as stated in [13].

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