# A CMOS Low-Voltage, High-Gain Op-Amp

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## Abstract

*A CMOS, self-biasing, single-supply op-amp is presented. It is designed with regulated cascode transistors for gain enhancement and a common-mode feedback technique for bias stabilisation of complementary regulated cascodes. It enables supply voltage lowering to about $2|V_T| + 2|V_{ds,sat}|$ with the maintain of high-gain operation. At $V_{dd}$ = 1.8 V, the measured dc gain of the op-amp is 115 dB, with a unity-gain frequency of 8.6 MHz for a capacitive load of 20 pF.*

## I. Introduction

The op-amp is one of the most widely used functional block for high-level analogue and mixed mode design. One design issue of many circuits or systems has revealed that their overall achievable performances are conditioned by that of the used op-amps. This situation has led to, especially for low-power, low-voltage, linear and A/D data conversion applications, strong demands for new or improved op-amps providing higher performances.

In this paper we present a low-voltage, high-gain op-amp which can operate with a single sub-2 V supply. It is a CMOS, two-stage structure. The input differential stage is composed of a folded cascode topology and a regulated-cascode building block acting as composite load. The very high output resistance of the building block allows a large dc gain (< 85 dB) for a single stage. The building block is built with complementary regulated cascode devices to enhance the output resistance, and a common-mode feedback technique to stabilise the output biasing point. The high-gain operation of the stage can be maintained for a supply voltage down to about $2|V_T| + 2|V_{ds,sat}|$. To obtain rail-to-rail output swing and to improve the current driving capability, a push-pull output stage is added.

## II. Regulated cascode

Regulated cascode circuits [1,2] contain very attractive features. In particular, extra high output resistance can be obtained, allowing the dc gain enhancement of an amplifier without needing to add additional stages [3]. A major advantage of this design approach for high-gain achievement is that Miller compensation is not needed to ensure stability, thus providing higher frequency performance [4]. Another interesting aspect of regulated cascode which is important for low-voltage applications is its low compliance voltage, compared with those having comparable output resistances such as triple cascode.

However, to form a high resistance node (output), complementary regulated cascodes are required. Due to the enhanced output resistance, the output biasing point is unstable and highly sensitive to supply voltage variations and complementary device mismatches. It results in dc biasing deviation and unwanted ac coupling.

To overcome this drawback, we employ a technique consisting of replica regulated cascode for bias sensing and common-mode feedback for bias stabilisation. A building block has been built to be used as composite load of the input stage.

## III. Bias-stabilising building block

The schematic diagram of the building block is shown in Fig. 1. It contains a pair of differential current inputs and a high-resistance output. A transimpedance $A_r$ is defined as its transfer function.

It makes use of regulated cascode transistors [1] and regulated cascode current mirrors (RCCMs) [2]. The upper part consists of 3 regulated cascode current mirrors (RCCMs), realising differential-to-single-ended conversion. A giga-ohm-range output is formed with n- and p-type regulated cascode current sources (RCCM2 and RCCM3). The input current $I_o + \Delta I$ is mirrored by RCCM1 to drive n-type RCCM3. With unity current ratio,

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and at low frequencies, the transimpedance $A_r$ is simply equal to the output resistance

$$A_r = \Delta V_{out} / 2\Delta I = r_{out} = r_{out,n}\, r_{out,p} / (r_{out,n} + r_{out,p}) \qquad (1)$$

where $$r_{out,n} = \frac{gm_{12} gm_{13}}{gds_{11} gds_{12} (gds_{13} + gds_{24})}$$

and $$r_{out,p} = \frac{gm_8 gm_9}{gds_7 gds_8 (gds_9 + gds_{27})} .$$

Such a high output resistance is obtained when all the transistors operate in the saturation region. We can thus estimate the required minimum supply voltage. Since the output signal of the building block will still be amplified by an output stage, an output swing of a few ten millivolts is enough for this building block. If we neglect this dynamic range, the minimum supply voltage for small-signal operation can be determined by the sum of both output compliance voltages of RCCM2 and RCCM3. Approximately, it is given by

$$V_{dd,min} \approx V_{tn} - V_{tp} + 2\,|V_{ds,sat}| \approx 2\,|V_T| + 2\,|V_{ds,sat}| . \qquad (2)$$

This means that regulated cascode circuits can operate at a supply voltage $V_{dd} < 2V$ or even much lower when using low threshold voltage processes.

To stabilise the biasing point, the lower part is added to perform bias sensing and feedback regulation. It includes two replica regulated cascode current mirrors RCCM2' and RCCM3' to obtain the same biasing point as the output. They are driven by the same input current $I_o + \Delta I$ through connections to nodes A and B. It is a common-mode drive and thus there is no dynamic change at node C. The static V(C) is then fed to the gates of $M_{20}$ and $M_{21}$. These two transistors drive respectively current mirrors ($M_{25}$ - $M_{27}$) and ($M_{22}$ - $M_{24}$) for feedback regulation. The bias currents $I_{b1}'$ and $I_{b2}'$ are adjusted, until V(C) = $V_t(M_{20},M_{21})$, which is the input threshold level of $M_{20}$ and $M_{21}$:

$$V_t(M_{20}, M_{21}) = \frac{V_{dd} + V_{tn} + V_{tp}\sqrt{\beta_n / \beta_p}}{1 + \sqrt{\beta_n / \beta_p}} . \qquad (3)$$

Since the main current mirrors RCCM2 and RCCM3 in the upper part are also controlled by identical currents $I_{b1}$(= $I_{b1}'$) and $I_{b2}$(= $I_{b2}'$), the dc output voltage has the same stabilised level as V(C). They can be set to $V_{dd}/2$ by sizing $M_{20}$ and $M_{21}$ with $(W/L)_{20} = 2.5\,(W/L)_{21}$.

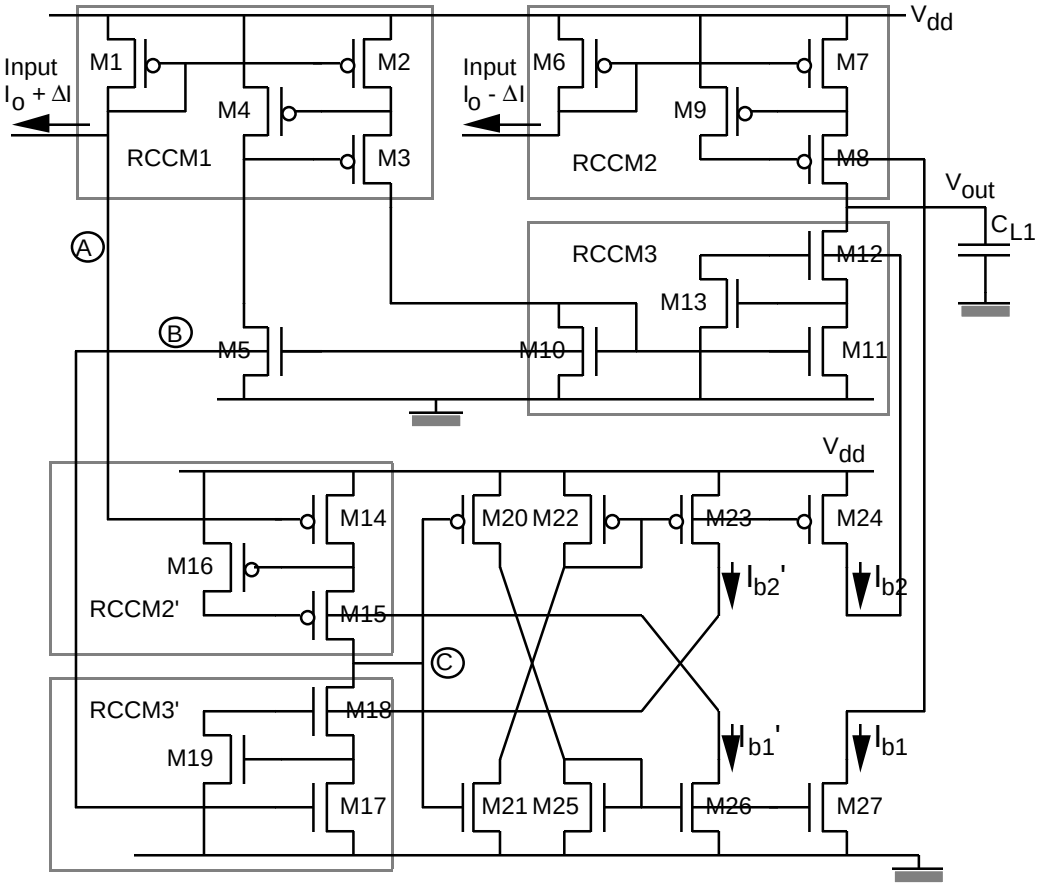


**Fig. 1: Transimpedance building block built with regulated cascode mirrors and common-mode feedback using replica devices**

The stabilised voltage V(C) determined by (3) is insensitive to mismatches of complementary regulated cascodes. This is the result of feedback regulation. Provided that main and replica devices are identical, the output biasing point is equal to V(C). However, slight random mismatches between main and replica devices may exist, and the feedback regulation is not effective for eliminating or reducing their effect. These mismatches, arising from fabrication imperfections, might lead to a dc potential deviation of output biasing point from V(C). For example, in worst cases, a 0.1 % geometrical mismatch between main and replica devices may cause a shift of about 0.18 V. Consequently, if the output biasing point is shifted out of the high-impedance range, the overall dc gain of the op-amp will drop. To minimise this effect, special care should be taken for matched devices in physical layout.

By neglecting this effect, it can be seen that $V_{out}$ differs from V(C) only if there are differential current signals applied between the two inputs. As V(C) is fixed by the feedback, a pure common-mode drive will not cause output voltage to change. This common-mode rejection can significantly improve the CMRR of the differential stage.

The frequency response of the building-block can be described with pole-zero locations. The low-frequency dominant pole is obviously determined by the high output resistance and the capacitive load. Node C has virtually no effect on frequency performances since V(C) is quasi-static. Other nodes have much lower resistance values and the related non-dominant poles and zeros are found at frequencies over 40 MHz. Real poles are created on current mirror's inputs. Complex poles are generated by regulated cascodes. Pole-zero doublets are formed resulting from mismatches between the differential current paths. Most non-dominant poles have gm dependence. Increasing bias currents can push them towards higher frequencies, thereby improving the phase margin.

## IV. Input differential stage

Fig. 2 shows the input stage which consists of a differential folded cascode amplifier and the regulated cascode building block acting as an active load. The dc gain of the stage is expressed as

$$A_{do} = V_{out} /(V_{in2} - V_{in1}) = - gm_{30} r_{out} . \quad (4)$$

The folded cascode amplifier driving the building block does not introduce low-frequency poles: as the current-driven input terminals of the building block are low-resistance nodes, the related input resistances of the folded cascode transistors ($M_{35}$, $M_{36}$) at nodes D and E have also small values. Accordingly, Miller effect on the input capacitances of the stage is reduced. It can be found that poles related to these nodes have frequencies at least 3 to 4 times higher than that of the non-dominant poles of the building block. Therefore, the ac behaviour of the stage is determined by that of the building block.

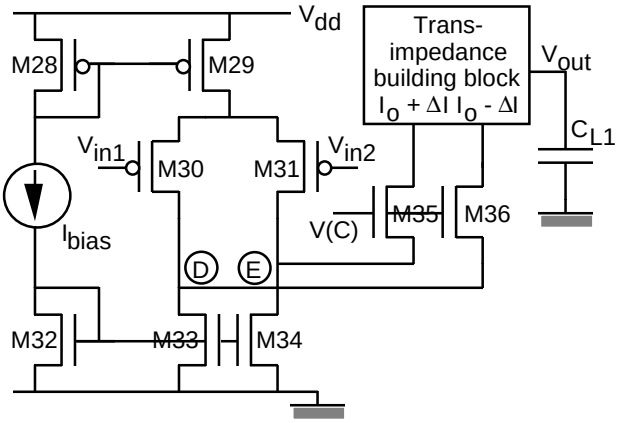


**Fig. 2: Differential stage using a folded-cascode amplifier and the transimpedance building block acting as a composite load**

The folded cascode amplifier has the same expression of the minimum supplied voltage as given by (2). The power consumption of the stage can be easily controlled through a bias current $I_{bias}$. $I_{bias}$ determines both input bias currents of the building block which have the same value

$$I_o = I_{ds34} + \frac{I_{ds29}}{2} = \left[ \frac{(W/L)_{34}}{(W/L)_{32}} - \frac{(W/L)_{29}}{2(W/L)_{28}} \right] I_{bias} \quad (5)$$

For large-signal operation, the maximum input current variation of the building block $|\Delta I|$ can reach $I_o$, and the achievable dynamic current for each input of the building block is $2|\Delta I| = 2 I_o$. It is equal to the output current of the stage charging and discharging the capacitive load. Thus the slew rate of the stage is given by

$$S_R = \frac{2|\Delta I|}{C_{L1}} = \frac{2I_o}{C_{L1}} . \quad (6)$$

It should be noted that input current swings of the building block correspond to the output current swings of the differential amplifier ($M_{29}$ - $M_{34}$), and this dynamic range is limited by the bias current $I_{ds29}$, i.e., $2|\Delta I|_{max} = |I_{ds29}|$. Therefore, when $2 I_o > |I_{ds29}|$, the slew rate can not be improved by simply increasing $I_o$. Only the power dissipation of the building block will be increased. But if too small values for $I_o$ are set, and $2 I_o < |I_{ds29}|$, as can be seen from (6), decreasing $I_o$ means smaller slew rate. Thus, we can consider $I_o = |I_{ds29}|/2$ as an optimum point, and use the following relationship deduced from (5):

$$\frac{(W/L)_{34}}{(W/L)_{32}} = \frac{(W/L)_{29}}{(W/L)_{28}} . \quad (7)$$

In this case, the current $I_o$ is written as

$$I_o = -\frac{I_{ds29}}{2} = \left[\frac{(W/L)_{29}}{2(W/L)_{28}}\right] I_{bias} . \quad (8)$$

Since the input stage is self-biased, $I_{bias}$ can be properly chosen for the trade-off between slew rate and power consumption, and $V_{dd}$ can be modified for supply voltage adaptation.

## V. Output stage

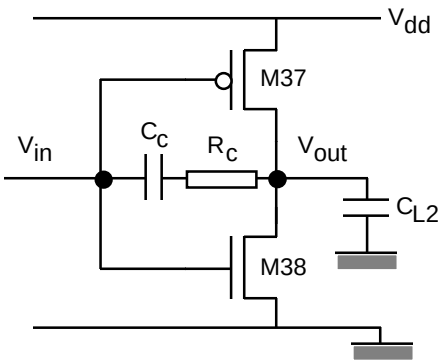


**Fig. 3: Push-pull output stage of the op-amp**

The output stage is shown in Fig. 3. At low supply voltages (e.g., $V_{dd}$ < 2V), a simple CMOS inverter can be used as a push-pull amplifier without causing excessive dc bias current for the stage. The low-frequency gain of the stage is

$$A_o = -\frac{gm_{37} + gm_{38}}{gds_{37} + gds_{38}} . \quad (9)$$

The input terminal node of the output stage connected to the precedent stage determines the only low-frequency dominant pole of the op-amp. To improve the stability, compensating components $C_c$ and $R_c$ are added. The capacitor $C_c$ becomes a key factor determining the unity-gain frequency $f_T = gm_{30}/(2\pi C_c)$ and the slew rate of the op-amp. The slew rate can be estimated using the expression (6) with $C_{L1} \approx C_c$, because the dynamic output current of the input stage is much smaller than that of the output stage, and the slew rate limitation depends mainly on the input stage charging and discharging $C_c$. The output capacitive load $C_{L2}$ has no effect on the bandwidth, but it may reduce the phase margin when it becomes large enough ($C_{L2}$ > 10 pF).

## VI. Simulated and measured results

Using Spice simulation, the dc gain dependence of the input stage on the supply voltage $V_{dd}$ and the bias current $I_{bias}$ was evaluated. From Fig. 4, it can be seen that high-gains are almost saturated for $V_{dd} \geq 1.9$ V. Around $V_{dd}$ = 1.7 V, the stage can still provide a gain larger than 85 dB. When decreasing further $V_{dd}$, some transistors which are regulated cascode components begin to enter in the ohmic region, resulting in a fast drop of voltage gain.

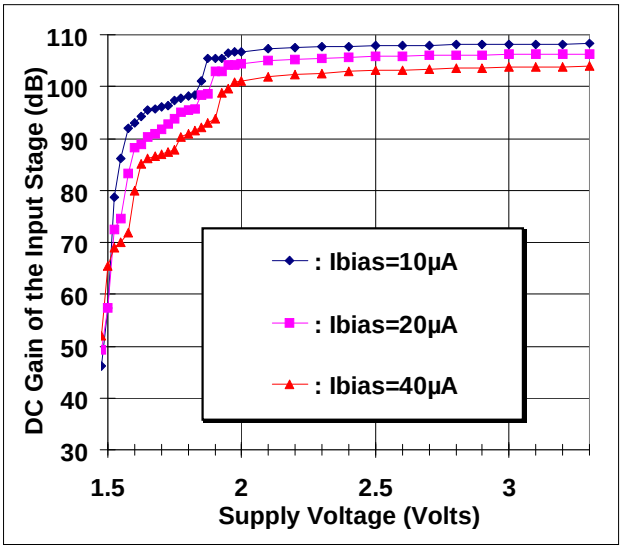


**Fig. 4: Simulated dc gain of the input stage versus supply voltage $V_{dd}$ with different values of bias current $I_{bias}$**

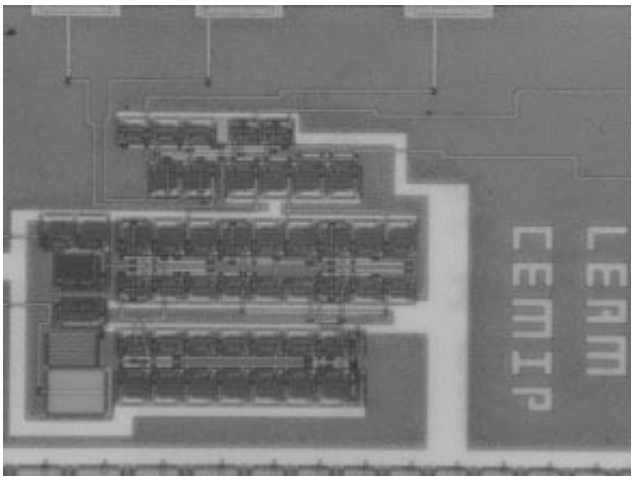


**Fig. 5: Photomicrograph of the op-amp realised on a test chip**

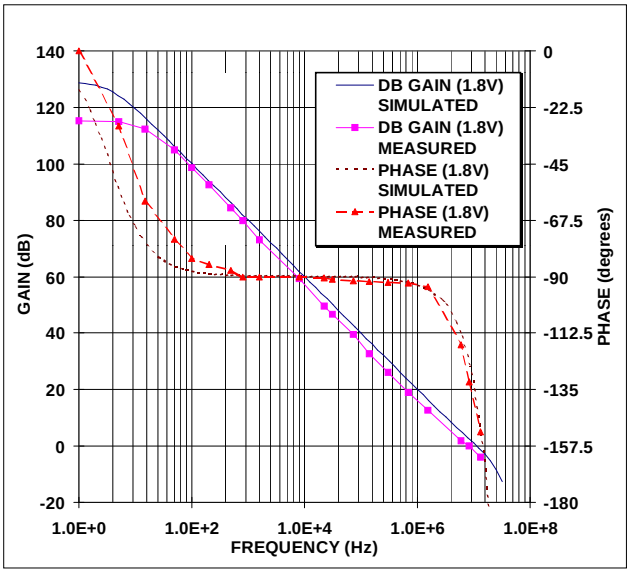


**Fig. 6: Frequency response of the op-amp**

| | Simulated | Measured |
|---|---|---|
| Supply voltage | 1.8 V | 1.8 V |
| DC gain | 128 dB | 115 dB |
| Unity-gain freq. | 11 MHz | 9 MHz |
| Phase margin | 50 degrees | 48 degrees |
| Power diss. | 0.5 mW | 0.55 mW |
| CMRR | > 150 dB | - |
| PSRR | > 150 dB | - |
| Slew rate | 7.5 V/µs | 8 V/µs |
| Settling time | 300 ns | 300 ns |
| Offset voltage | - | 25 mV |
| Capacitive load | 20 pF | 20 pF |
| Noise (100-10MHz) | 130 µVrms | - |
| Output swing | rail-to-rail | rail-to-rail |
| CM input range | 0-0.9 V | 0-0.9 V |

**Tab. 1: Main characteristics of the op-amp**

The op-amp was designed with a 1.2-µm, double-poly, double-metal CMOS process, and was realised on a test chip (Fig.5), together with other parts to be tested. It has a die area of 0.2 $mm^2$. Fig. 6 shows the frequency response of the op-amp obtained with $V_{dd}$ = 1.8 V, $I_{bias}$ = 20 µA and $C_{L2}$ = 20 pF. The measured dc gain is 115 dB, instead of being 128 dB predicted by simulation. At $V_{dd}$ = 2 V, the measured and simulated values are respectively 127 dB and 140 dB. This difference between measurement and simulation may be explained by the slight mismatches between main and replica devices, as previously mentioned. Other characteristics are summarised in Tab. 1.

## VII. Conclusions

With regulated cascode composite load, the dc gain of a single stage can substantially be enhanced. By using replica device for bias sensing and common-mode feedback, sensitivity problems associated with a high-resistance node are solved. The output biasing point of complementary regulated cascodes is so stabilised in the high-impedance range that the supply voltage $V_{dd}$ can be reduced to about $2|V_T| + 2|V_{ds,sat}|$. This makes it possible to design high-gain op-amps operating at such a low supply voltage.

## References

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