SWITTEST: Automatic Switch-level Fault Simulation and Test Evaluation of Switched-Capacitor Systems[1]

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ABSTRACT

A tool for the switch-level fault simulation and test evaluation of switched-capacitor systems is presented. Time or frequency-domain fault simulations with SWITCAP and time-domain fault simulations with HSPICE can be performed. Adequate fault models are presented for both simulators. The tool has proven to be very useful in the early evaluation of test strategies, providing similar results to those obtained at the transistor-level.

INTRODUCTION

Fault simulation is a widely applied technique to analyze the testability of integrated circuits and to optimize a test approach. For analog and mixed-signal circuits, fault simulations are traditionally performed at the transistor-level using circuit simulators such as HSPICE [1]. Unfortunately, analog fault simulation is a very time consuming task and, even for rather simple circuits, a comprehensive transistor-level fault simulation is normally unfeasible. Macromodels of circuit components are conveniently used to decrease the extremely long computation times. Fault simulation approaches using high level simulators, which can simulate above the circuit level approach based on differential equations, are usually avoided due to the lack of adequate fault models.

In this work, we propose an automatic tool called SWITTEST for the switch-level fault simulation and test evaluation of switched-capacitor and mixed switched-capacitor/digital circuits. These circuits are widely used for integrating many signal processing functionalities in MOS technologies. Examples include filters, data converters, PCM codecs, PLLs and neural netwoks. The advantage of the switch-level fault simulation approach is that it facilitates the integration of test as early as possible in the design of these systems. The evaluation of a test strategy can be performed with simulation times which are orders of magnitude lower than for transistor-level fault simulations, even when macromodels are considered for some components, and the results are sufficiently significative to decide to reject a test approach or to carry on with it.

SWITTEST can use both SWITCAP2 [2], with a discrete-time fault model, and HSPICE, with a continuous-time fault model, as core simulators. SWITCAP2 (from now on SWITCAP) is an special purpose simulator which, taking advantage of the algebraic nature of the charge-based equations of switched-capacitor networks, provides simulation algorithms extremely useful both for linear and mixed analog/digital switched-capacitor circuits. Therefore, SWITCAP is preferred over HSPICE in the early design stages.

For fault simulation, second-order effects such as non-zero ON resistance of switches or finite output resistance of voltage sources and operational amplifiers play a significant role once faults are present in a switched-capacitor system. These fault modeling issues are addressed in this paper, and the feasibility of switch-level fault simulation is demonstrated by using adequate fault models. We have found convenient both SWITCAP and HSPICE switch-level fault simulations. For example, CPU times for a time-domain SWITCAP fault simulation taking into account secondary effects may be longer than for an equivalent HSPICE simulation due to the need of simulating second-order resistances by means of additional switched-capacitor resistors. On the other hand, the effect of faults in the frequency domain for switched-capacitor linear circuits can be readily analysed by means of SWITCAP.

RELATED WORK

Fault simulation plays a central role in the validation and optimization of a test approach. A typical test goal is to achieve a fault coverage as close as possible to 100%. To reach an optimal fault coverage, an iterative process over the test strategy and the circuit design [3], as shown in Figure 1, is required. If the fault coverage figure is too low it may be because of: (a) test stimuli which are not good enough; (b) test parameters which are not fault sensitive enough; (c) accessibility and observability problems of fault sensitive parameters; or (d) redundancy in circuit components. The term *redundant component* is used in the sense that circuit functionality is practically unaltered regardless of the value or state of the component. For example, if a faulty switch is stuck-open (stuck-on), and the functionality of the circuit is practically unaltered, the switch is redundant in this circuit.

Several analog fault simulation tools have been presented using HSPICE as the core simulator [4, 5]. An inconvenience of these tools for linear switched-capacitor circuits is that a frequency-domain fault simulation cannot be directly performed and this is important, for example, for the determination of the test stimuli [6]. A fast fault simulation approach has been presented in [7], but this

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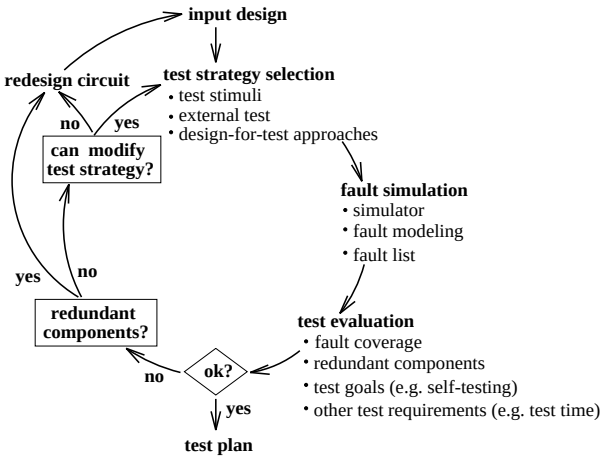

Figure 1: Optimization of circuit testing.

only addresses continuous-time linear analog circuits.

The lack of adequate fault models and realistic fault lists is a main reason preventing an early evaluation of testability in the analog design flow. For the extraction of realistic fault sets, useful techniques such as Inductive Fault Analysis (IFA) [8] can only be used after layout which is towards the end of the design process. Thus, analog test engineers often consider *hard or catastrophic faults* (i.e. an open or short circuit) and *soft or parametric faults* (i.e. a component deviation from its nominal value without reaching its extreme bounds). Hopefully, an early estimation of testability can be performed considering these classical faults at the device level. In recent results [3], mixed-signal fault simulations based on fault lists generated from IFA are compared with simulations based on a transistor-level open/short fault model. The comparison showed that both approaches lead qualitatively to the same results, indicating the circuit parts with undetectable faults and giving a clear indication on how to improve the test approach.

A problem that arises is how to model these faults at design stages above the transistor-level and for special-purpose simulators. For example, fault modeling for SWITCAP has been avoided in the past due to the lack of adequate fault models [9]. Instead, the discrete-time circuit has been modeled as an equivalent continuous-time circuit for HSPICE fault simulation [10, 9]. However, it is known that those models are not correct for all faults that can occur in circuit switches.

SWITCH-LEVEL FAULT SIMULATION

Our fault simulation approach is based on modifying a fault-free netlist of the input design into a netlist with an injected fault. A single fault assumption is made. After the execution of the nominal design, analog fault simulation is performed in a repetitive cycle of three main phases: preprocessing of the original input file and fault injection, run of the circuit simulator, and a phase of postprocessing that compares results and extracts statistics.

Description of the tool

Switch-level fault simulation with SWITTEST is performed as shown in Figure 2. At the starting point of any fault simulation, a fault-free SWITCAP description of the circuit is required. This is because fault injection is only performed in a SWITCAP specification. The SWITCAP description can be edited manually or prepared by means of a design environment as shown in Figure 2(a). The schematic captured by means of a computer-aided design environment can normally be represented as an HSPICE output file, and this file converted into a SWITCAP representation by means of a translator available in SWITTEST. In the case that transistor-level subcircuits exist in the HSPICE design (such as switches, logic gates, amplifiers, comparators, etc.), the translator can be told to replace them by equivalent SWITCAP primitives or subcircuits (in this case, the input design must be hierarchical).

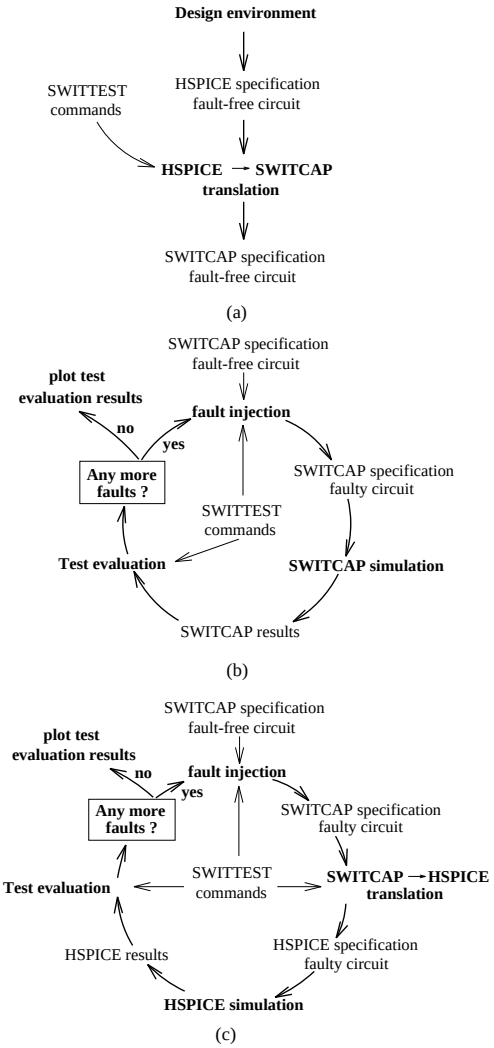

Figure 2: Automatic fault simulation: (a) preparation of a SWITCAP description, (b) fault simulation with SWITCAP, and (c) fault simulation with HSPICE.

For hierarchical designs, the injection of a fault is performed by flattening the design hierarchy where the faulty component is embedded. This fault injection approach based on circuit flattening is required for SWITCAP fault simulation, and it also provides the most efficient way of fault simulation with HSPICE since a minimum number of additional components are added to the fault-free design for fault simulation.

For its evaluation, the test approach must be adequately characterized as a set of *test variables*. In general, a test variable is formed as a combination of a number of *test measures*. A test measure is represented as a numeric expression on circuit voltages. Circuit misbehavior is observed if a test variable exceeds a certain *test threshold*. Circuit test properties such as fault coverage can then be obtained as a function of a test threshold.

Automatic switch-level fault simulation and test evaluation can be performed with SWITCAP in time- or frequency-domain, or with HSPICE in time-domain. Figure 2(b) illustrates the process of

SWITCAP fault simulation. A repetitive three-phase cycle of fault injection, SWITCAP simulation, and test evaluation is performed. A command file provides to SWITTEST the fault list, some required circuit parameters, and the test variables. The fault simulation cycle for HSPICE is shown in Figure 2(c). During each cycle a fault is injected in the input SWITCAP file and the file translated into an HSPICE file for simulation. In the SWITCAP → HSPICE translation, switches are represented as voltage-controlled resistors. Parameters such as ON and OFF switch resistances and voltage source or amplifier output resistance are given in the command file.

SWITTEST has been implemented in Prolog, with some interfacing procedures in the C language. The tool contains 7689 lines of code (with 20% comments), including HSPICE and SWITCAP parsers, and HSPICE ↔ SWITCAP translators.

Fault models

Switched-capacitor circuits and mixed switched-capacitor/digital circuits can be considered for fault simulation. A fault list including faults in switches and capacitors, and stuck-at faults in logic components is provided to SWITTEST. In a faulty circuit, second-order effects such as non-zero ON resistance of switches or finite output resistance of voltage sources (or operational amplifiers) need to be included. Other second-order effects (e.g. clock feedthrough) can easily be taken into account if necessary, although this is not so significant as shown later by the experimental results obtained. A continuous-time fault modeling approach for HSPICE is shown in Figure 3.

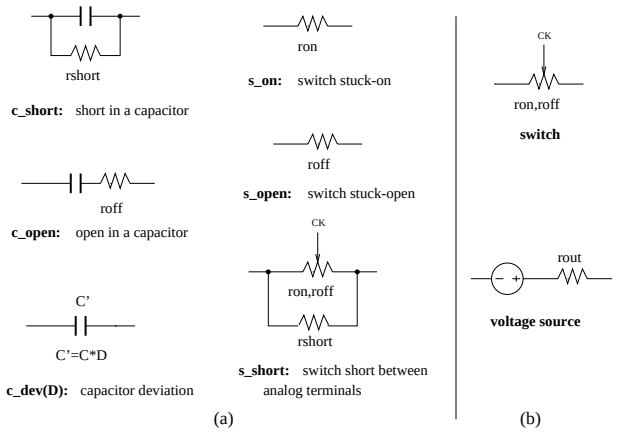

Figure 3: HSPICE fault modeling: (a) fault models, and (b) models for non-faulty components.

The two common classes of analog faults are modeled in Figure 3(a): catastrophic faults include shorts between the analog terminals of a switch or shorts in a capacitor, opens in circuit capacitors and switch stuck-on and stuck-open faults. Short faults are represented as a resistive impedance between the shorted lines. An open fault in a capacitor is modeled as a resistor in series with the capacitor. Switch stuck-on faults are modeled by substituting the faulty switch by a resistor modeling the ON resistance of the switch, and switch stuck-open faults by substituting the faulty switch by a resistor modeling the OFF resistance of the switch. Parametric faults include deviations on circuit capacitors (*c_dev(D)*, where D indicates a relative deviation of the nominal value).

To adequately model fault effects at the switch-level, non-faulty components must also be modeled as shown in Figure 3(b). Each switch in the design is modeled as a voltage-controlled resistor with its ON and OFF resistance values. An output resistance is added at the output of each voltage source (and operational amplifier) to model a resistive output impedance.

A discrete-time fault modeling approach for SWITCAP is shown in Figure 4. This is equivalent to Figure 3, considering that all resistors are now modeled by means of bilinear switched-capacitor resistors. These resistors require a two-phase clock FS of frequency f', and f' needs to be larger than the fastest clock frequency in the circuit. This is analyzed next.

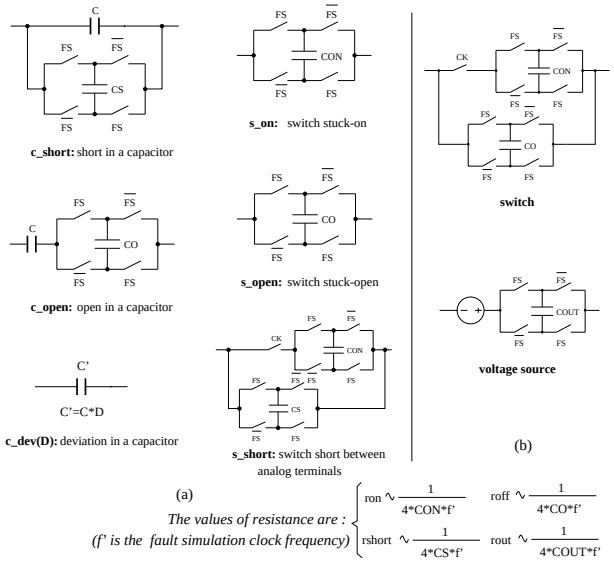

Figure 4: SWITCAP fault modeling: (a) fault models, and (b) models for non-faulty components.

SWITCAP fault modeling analysis

The results obtained for time-domain fault simulations are practically the same with HSPICE and SWITCAP, provided that attention is paid to the value of the fault simulation clock f'. This can be analyzed by means of the simple circuit of Figure 5 in which a capacitor is charged through a switched-capacitor resistor.

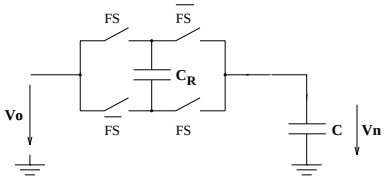

Figure 5: Charge of a capacitor through a bilinear switched-capacitor resistor.

It is easily shown that if capacitor C is initially discharged, the voltage V_n through this capacitor after n clock cycles is given by $V_n = V_o\left(1 - \left[\frac{C-C_R}{C+C_R}\right]^{2n}\right)$. The charge of a capacitor through a resistor in continuous-time is given by $V_t = V_o(1 - e^{-\frac{t}{RC}})$. Equating both equations for $t = \frac{n}{f'}$ gives

$$R = \frac{1}{2\,C\,f'\ln\left(\frac{1+\frac{C_R}{C}}{1-\frac{C_R}{C}}\right)} \qquad (1)$$

According to (1), the switched-capacitor resistor behaves as a resistor (for $C_R < C$) whose value depends on the switching frequency f', capacitor C_R and the charged capacitor C. If the switched-capacitor resistor must model an actual resistor, the resistance value should be independent of the charged capacitor C. Considering that,

for $x \ll 1$, $ln\left(\frac{1+x}{1-x}\right) \approx 2x$, for

$$\frac{C_R}{\mathrm{C}} \ll 1 \tag{2}$$

(1) becomes

$$R \approx \frac{1}{4\, f'\, C_R} \tag{3}$$

which gives a value independent of the charged capacitor C.

Since the tool does not calculate the capacitive load of each switch, which may depend on the clock phasing, (3) is used in place of (1) to define the switched-capacitor resistor which models a switch resistance or a voltage source output resistance. The relative error δ incurred when (3) is used in place of (1) is given by

$$\delta = 1 - \frac{2\frac{C_R}{C}}{ln\left(\frac{1+\frac{C_R}{C}}{1-\frac{C_R}{C}}\right)} \tag{4}$$

and the error only depends on $\frac{C_R}{C}$, and not on the switching frequency f'. Equations (1) and (3) are represented in Figure 6(a) for f'=100 MHz and C=1pF. The error δ defined by (4) is represented in Figure 6(b). From Figure 6(b), if the value of C_R is around $0.25C$ or smaller, (3) produces accurate results (and this is regardless of the value of f').

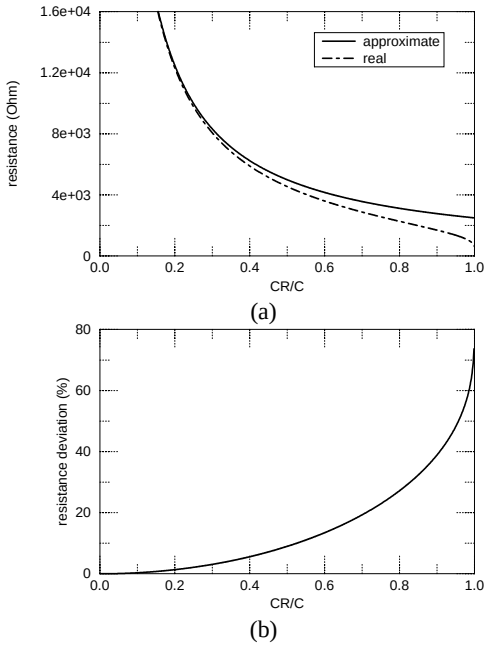

Figure 6: Bilinear switched-capacitor resistor: (a) approximate and real resistance values, and (b) resistance deviation.

Given the smallest resistor $R_{\min}$ to model and the smallest capacitor in the design $C_{\min}$, the tool can derive a frequency f' which guarantees accurate results in the worst case. This is done as follows. The capacitor of the switched-capacitor resistor model for $R_{\min}$ is given by

$$C_{R\min} = \delta_r\, C_{\min} \tag{5}$$

where a value of $\delta_r = 0.25$, according to Figure 6(b), produces accurate results even for a possible worst case time constant given by $R_{\min} * C_{\min}$. With $R_{\min}$ and $C_{R\min}$, the switching frequency f' is calculated from (3). For higher resistance values in the design, the capacitor of the switched-capacitor resistor is calculated from the value of resistance and the switching frequency f' by means of (3), and it is ensured that the condition imposed by (2) is always met (any switched-capacitor resistor verifies $C_R \leq 0.25C$, where C is its capacitive load).

It can be shown that, if f is the largest switching frequency in the design, this worst-case value of f' results in a frequency increase factor defined by FI $= \frac{f'}{f}$ in the range of 10 to 1000 for sensible designs. For practical purposes, a value for FI of 10 or 20 is normally sufficient. It must be noted that very low values of resistance may lead to excessively large switching frequencies. It is then convenient to use values of short faults around the smallest value of switch ON resistance, which normally leads to an underestimated fault coverage. Voltage source output resistances can also be neglected if they are much smaller than the smallest switch ON resistance.

EXPERIMENTAL RESULTS

The fully differential biquadratic filter of Figure 7 is considered in this section to illustrate the use of the tool. The test variable corresponds to the observation of deviations of input common-mode in the amplifiers as a result of a circuit fault [10]. The nominal common-mode at each amplifier inputs is close to analog ground. The frequency of the switched-capacitor clock is 4 MHz.

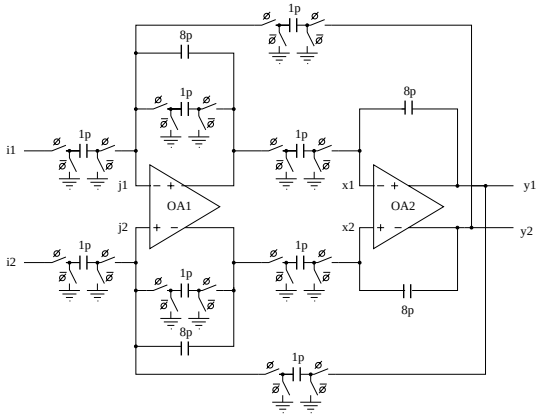

Figure 7: Fully differential biquadratic filter.

Switch-level fault simulations with SWITCAP and HSPICE are performed and the fault coverage of the test approach is given as a function of test threshold. The same results are obtained for time-domain fault simulations. These results are also compared with transistor-level fault simulations to validate the switch-level fault simulation approach. All simulations were performed on a SUN SPARC10 workstation.

Time-domain fault simulation

The SWITTEST command file of Table 1 is used to drive a time-domain fault simulation for the differential filter of Figure 7. A 2 V differential signal at 100 KHz is considered at the filter input in the design specification.

The fault list indicates that hard faults are injected in all switches and capacitors, and parametric deviations are considered for the capacitors (individual components can also be referenced in the fault list). All switches are assumed to have the same ON and OFF resistances (a switch can also be individually referenced), the output resistances of voltage sources are neglected in this example (including those sources used to model the operational amplifiers which have a differential gain of 20000), and the value of short resistance selected is equal to the ON resistance of a switch (4KΩ). The resistance of an open fault is the default value of switch OFF resistance (100MΩ). The unit of capacitance for the capacitors in the input

```
(analysis=tran).
(faults=[(switch,s_on),(switch,s_open),(capacitor,c_short),
     (capacitor,c_dev(2)),(capacitor,c_dev(0.5)),
     (capacitor,c_open),(switch,s_short)]).
(rshort=4.0e3).
(ron=[(switch,4.0e3)]).
(roff=[(switch,1.0e8)]).
(cap=1.0e-12).
(mincap=1).
(tf=10.0e-9).
(tr=10.0e-9).
(tm(1)= (v(j1)+v(j2))/2).
(tm(2)= (v(x1)+v(x2))/2).
(tv(1)=max(absmax(tm(1)),absmax(tm(2)))).
(time(T) :- T > 3.0e-6).
(th(1)=0.05).
```

Table 1: Command file for time-domain fault simulation.

SWITCAP design corresponds to picofarads (*cap=1.0e-12*) and the lowest capacitive load of a switch corresponds to 1 pF (*mincap=1*, where the value of *mincap* is given in the same capacitance units used in the SWITCAP design). The clock frequency increase for fault simulation in this design is FI=63 for the minimum values of resistance (4KΩ) and switch capacitance load (1pF). Parameters *tf* and *tr* correspond to the rise and fall times of the circuit clock signals for HSPICE fault simulation.

Two test measures are considered (*tm(1)* and *tm(2)*) which correspond to the observation of the common-mode at each amplifier inputs. After the simulation of a fault, the contents of a test measure corresponds to a list of values, where each of them is the value of the test measure at a different simulation time. Test variable *tv(1)* corresponds to the largest absolute value for test measures *tm(1)* and *tm(2)*. The times at which simulation results are acceptable for computing the test measures can be controlled by means of a *time(T)* statement. Thus, *tv(1)* corresponds to the largest input common mode in any of the two stages after 3 μs, and the printing step in the design specification is adjusted so that the common-mode is measured at the end of phase $\overline{\phi}$. A threshold for test variable *tv(1)* is also included (*th(1)=0.05*) in order to obtain some statistics on undetectable faults for this threshold value.

Fault simulations have been carried out with both SWITCAP and HSPICE for a total of 144 faults given by the fault list of Table 1. Figure 8 shows the fault coverage given by SWITTEST as a function of test variable threshold. For a threshold of 50 mV, 36 faults are undetected and these correspond to 18 switch stuck-on faults and 18 switch short faults. For a simulation time of 30 μsec, the CPU time for the SWITCAP fault simulation is 11859 seconds with FI=63 and 1476 seconds for the HSPICE simulation.

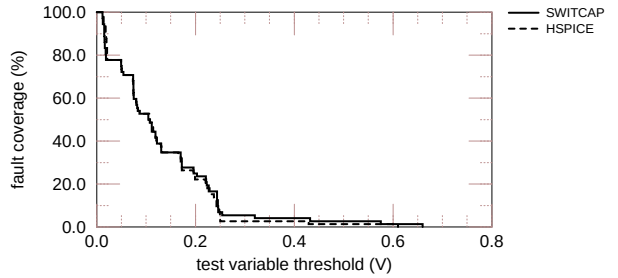

Figure 8: Fault coverage for switch-level time-domain fault simulations with SWITCAP and HSPICE.

For SWITCAP fault simulation, practically the same results are obtained with FI=13 in 2542 seconds. For this value of FI, the capacitor in the switched-capacitor resistors simulating resistances of 4KΩ is about $C_R = 1.2$ pF. Since the minimum size capacitors of 1pF in figure 7 are charged or discharged through at least two switches in series, an equivalent $C_R = 0.6$ pF results. According to figure 6b, with $\frac{C_R}{C} = 0.6$, the actual resistance may only deviate up to 13%.

Frequency-domain fault simulation

A frequency-domain fault simulation determines the best fault coverage that can be achieved with a multifrequency test. The commands in Table 2 are used to drive a fault simulation in the frequency domain for the differential filter of Figure 7. For simplicity, since both inputs of an amplifier have practically the same voltage, signals *j1* and *x1* are used as a measure of the amplifiers input common-mode. Variables *vm(j1)* and *vm(x1)* (voltage magnitude of *j1* and *x1*) must be used in the print statement of the design specification and, for example, *tm(1)* corresponds to the input common-mode in the first amplifier. Alternatively, the real and imaginary parts of signals j1 and j2 can be printed, and test measure *tm(1)* can be defined as *tm(1)=cmod(cadd(vr(j1)-vi(j1),vr(j2)-vi(j2)))/2*, where the operator *cadd* adds the two complex numbers and the operator *cmod* extracts the magnitude of a complex number.

```
(analysis=sss).
(faults=[(switch,s_on),(switch,s_open),(capacitor,c_short),
     (capacitor,c_dev(2)),(capacitor,c_dev(0.5)),
     (capacitor,c_open),(switch,s_short)]).
(rshort=4.0e3).
(ron=[(switch,4.0e3)]).
(roff=[(switch,1.0e8)]).
(cap=1.0e-12).
(mincap=1).
(tm(1)= vm(j1)).
(tm(2)= vm(x1)).
(tv(1)=max(max(tm(1)),max(tm(2)))).
(th(1)=0.05).
```

Table 2: Command file for frequency-domain fault simulation.

An input test signal of 2 V differential and 60 frequency points in the band $[1\text{KHz} - 1\text{MHz}]$ are given in the design specification. As shown in Figure 9, the fault coverage obtained in frequency-domain is better than the obtained in time-domain, since the whole frequency band is considered to determine the largest deviations. The time-domain fault coverage is quite acceptable since the 100 KHz input signal used as test stimuli is around the cut frequency of the filter where most faults are observable.

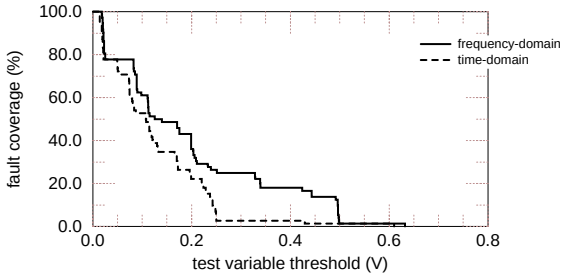

Figure 9: Fault coverage for SWITCAP frequency-domain and time-domain fault simulations.

Detection of all faults can only be achieved for the fault list and test strategy considered with a test variable threshold of 18 mV. The CPU time for the frequency-domain SWITCAP simulation is 29709.75 seconds with FI=63 (the same results are obtained with FI=13 in 6544 seconds).

Transistor-level fault simulation

One of the known limitations of switch-level simulations is the use of macromodels for circuit components which cannot take into account all secondary effects present in the actual circuit. In this paper, we have taken into account switch resistances and voltage source output resistances, but other second-order effects such as clock feedthrough and charge injection in MOS switches have not been included in order to keep the fault models simple. However, we have investigated up to which extent the results obtained with the current fault models in SWITTEST are useful for making decisions about the testability of a design. For that, transistor-level simulations have been carried out with HSPICE for the case-study considered. The fault models used are shown in figure 10. CMOS switches are used for the implementation, but a macromodel for the operational amplifier is still considered. These models allow the implementation at the transistor-level of the same type of faults considered at the switch-level.

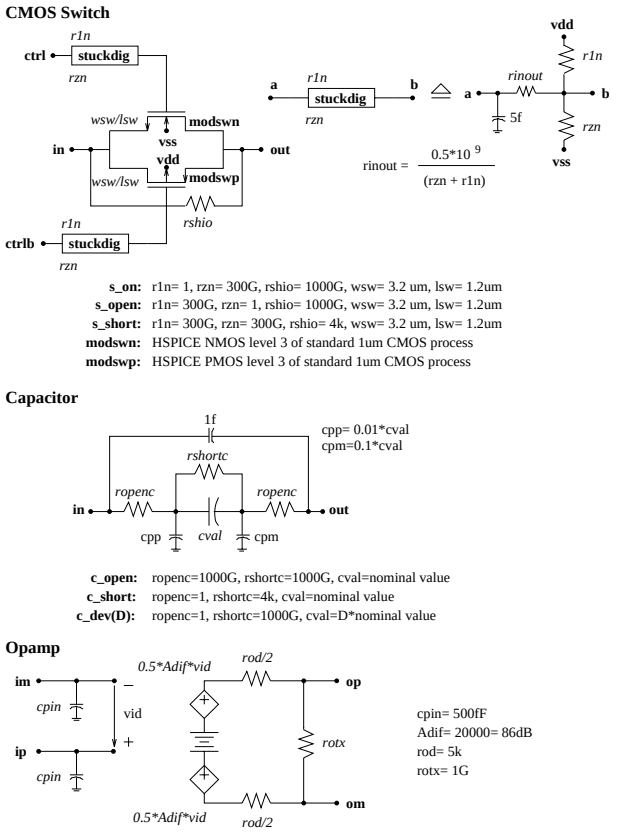

Figure 10: Transistor-level fault models.

Switch stuck-on and stuck-open faults are injected in a single switch at a time by controlling the values of the resistances in the corresponding instance of the cell called *stuckdig*. Switch and capacitor shorts are modeled with a short resistance of 4KΩ. Capacitor opens are modeled with 1000GΩ resistors in series with a capacitor. A differential gain *Adif*=20000, an input amplifier capacitance *cpin*=500fF, and a differential output resistance *Rod*=5KΩ are considered for the operational amplifiers. The ON resistance of the switch, which depends on the value of the analog signal being transferred, is around 4KΩ.

The fault coverage obtained for the transistor-level simulation of the 144 faults is compared in Figure 11 with the switch-level fault coverage. At the switch-level, the fault coverage is shown for two values of the amplifier differential output resistance in order to observe the effect of this parameter. The transistor-level fault coverage is obtained with an amplifier differential output resistance of 5KΩ. The switch and transistor-level fault coverage is very similar. The CPU time for the transistor-level HSPICE fault simulation with an operational amplifier macromodel is of 16800 seconds, about an order of magnitude larger than the switch-level fault simulations.

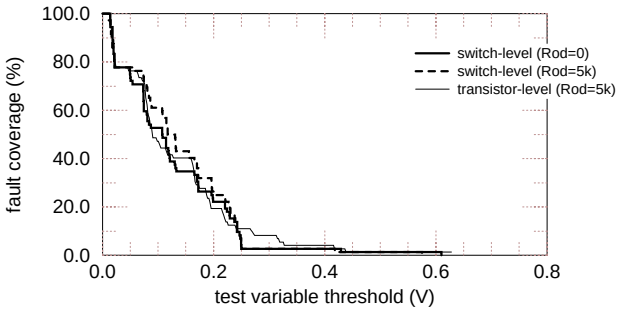

Figure 11: Fault coverage for HSPICE time-domain fault simulations at the switch and transistor levels.

CONCLUSIONS

In this paper, we have presented an automatic tool called SWITTEST for the switch-level fault simulation of switched-capacitor systems. The advantage of the approach is that it facilitates the integration of test as early as possible in the design of switched-capacitor systems, allowing the evaluation of fault effects both in the time and frequency domains. The feasibility of switch-level fault simulation, both with SWITCAP and HSPICE as core simulators, is demonstrated through the use of adequate discrete-time and continuous-time fault models. Depending on the characteristics of the circuit under test, a fault simulation approach may be faster than the other. Fault simulation in the frequency domain is performed with SWITCAP. The switch-level fault models proposed allow the consideration of the most common faults in analog and mixed-signal circuits. Their suitability has been proved by comparing results at the switch and transistor levels.

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