Micro Power “Relative Precision” 13 bits Cyclic RSD A/D Converter

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Abstract

“Relative precision” A/D and D/A converters are presented. They feature a limited signal-to-noise ratio but have a dynamic range of 13 to 14 bits. These characteristics are achieved by using a so called RSD (Redundant Signed Digit) algorithm conducting to a minimal implementation complexity. The elements of the analog part of the A/D converter and its digital control consumes less than 50 µW at 2.4 V power supply voltage, whereas the D/A converter with its track&hold circuit consumes 75 µW at the same supply voltage.

1 Introduction

Recent progress in Digital Signal Processing makes the application of digital algorithms more and more attractive in various fields. However, in battery-operating equipment which needs analog interfaces, the power consumption of the additional today’s available A/D and D/A converters restricts the use of digital signal processing.

Typical audio applications need a bandwidth above 6 kHz and a dynamic range of about 80 dB corresponding to 13 to 14 bits precision. It is clear that converters with such features consuming distinctly less than 1 mW are not standard components today.

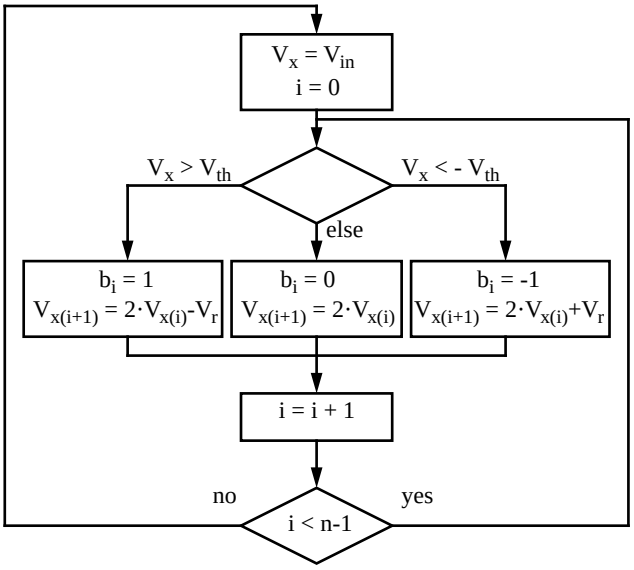
Fortunately, in many audio applications, these requirements may be loosened without loss of perceived signal quality. Numerous masking experiments [Schr79] indicate that noise at a level of 30 dB below signal components does not cause any perceptual degradation. Consequently, for such applications, the design constrains are the dynamic range and the minimal signal-to-noise ratio.

2 Related works

In [Scha92] the “relative precision” is achieved by a kind of floating point converter. The minimal signal-to-noise ratio determines the number of bits of the mantissa realised as a normal linear converter. At the front end, a variable gain pre-amplifier provides the required dynamic range (see [Gri95] and [Gri96] for an implementation).

3 “Relative precision” using RSD

An RSD (Redundant Signed Digit) converter which algorithm can be seen in figure 1, has been published in [Gin92].



V_{in}:	input voltage	V_r:	reference voltage
$V_{x(i)}$:	intermediate voltage	b_i:	output bits
V_{th}:	threshold voltage	n:	number of bits

FIGURE 1. Cyclic RSD converter algorithm

The original advantage of the RSD-algorithm over the algorithmic converter (figure 2, [Hoe94]) is to replace a very accurate comparator (precision better than 1/2 LSB) by two very simple comparators which inaccuracy can reach half the reference voltage V_r regardless of the number of bits. In [Gin92] a 13 bits absolute precision converter is described

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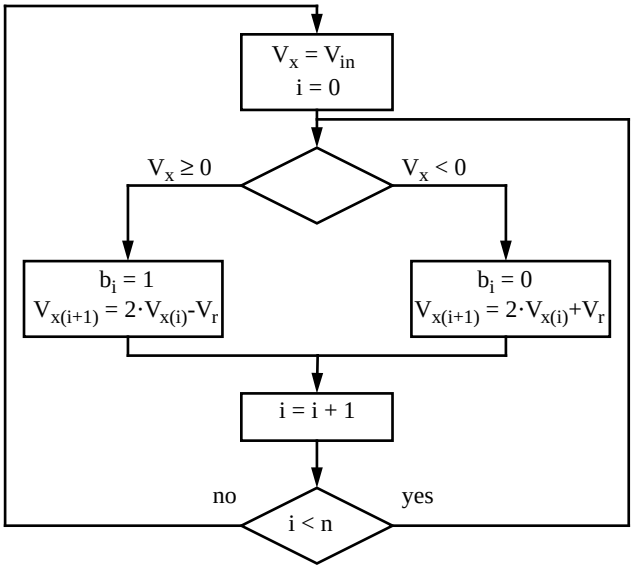

V_{in}: input voltage V_r: reference voltage

$V_{x(i)}$: intermediate voltage b_i: output bits

V_{th}: threshold voltage n: number of bits

FIGURE 2. Algorithmic converter

where the capacitor mismatch is compensated in an analog way. The stated power consumption is 45 mW at a sampling rate of 25 kHz and ± 5 V supply voltage.

With the RSD-algorithm, if a “relative precision” can be tolerated, it is not necessary to compensate the capacitor mismatch, nor to have very high gain operational amplifier and finally the reference do not have to be very accurate. The effects of these imperfections only affect the maximum achievable signal-to-noise ratio as one can see on a simulation in figure 3. The capacitor mismatch effect on the signal-to-noise ratio for a 1 kHz sinusoidal input signal and a sampling frequency of 16 kHz is plotted.

The use of RSD-algorithm has some other advantages listed below:

- active element offset gives only a digital offset (can be easily compensated if needed)
- switch charge injection has the same effect
- active element saturation causes digital saturation (no distortion for low level input signals)
- capacitors non-linearity only limits the maximal signal-to-noise ratio
- the quality of the reference has the same effect

The unique fundamental limit for the dynamic range is the noise sampled at each iteration of the algorithm.

In order to highlight the “relative precision” effect of the RSD algorithm, one can consider the effect of an inaccuracy Δ_1 introduced at the first iteration of the algorithm.

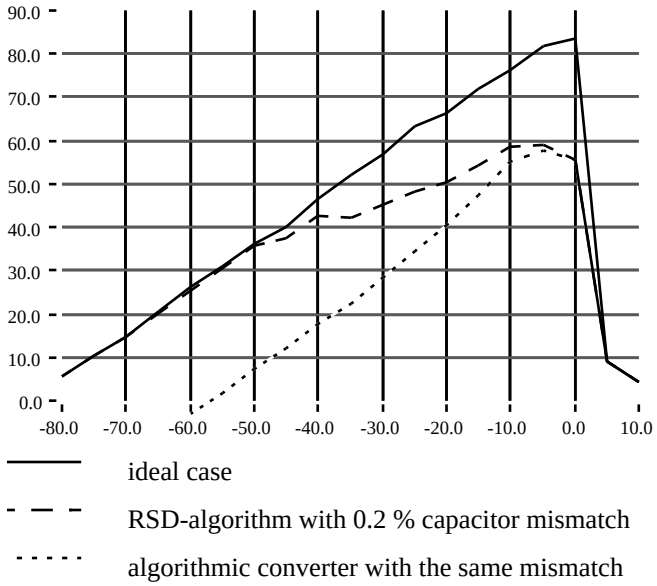

FIGURE 3. Signal-to-noise ratio as a function of the input signal level for 14 bits converters

Assuming that:

- The precision of the rest of the algorithm is perfect, the final error will be $2^{n-2} \cdot \Delta_1 / Vr$ LSBs for both converter algorithms.
- V_{in} is close to 0.
- The error Δ_1 comes from the finite gain of an amplifier, the error Δ_1 is proportional to $V_{x(1)}$.

Then for the algorithmic converter as $V_{x(1)}$ is close to $\pm V_r$ the **final error** is **proportional to V_r**.

And for the RSD-converter as $b_0 = 0$ then $V_{x(1)} = 2 \cdot V_{in}$ and the **final error** is **proportional to V_{in}**.

4 Realisation

The converter is realised in CMOS technology and the operations of the algorithm are performed with switched capacitors. It can be implemented very simply thank to the characteristics of the algorithm and the design constrains.

The input signal is sampled at the beginning of the algorithm, thus no sample and hold circuit is required in front of the circuit.

Since the comparisons have a large tolerance, these functions can be realised by simple strobed cross-coupled inverters, thus no static power is consumed by the decision circuits.

A simple shift register is sufficient to store the digital result of an algorithmic converter. Nevertheless an additional component is required to convert the redundant output of the RSD converter into a 2’complement form [Gin92]. This circuit needs about 70% more gates than a shift register.

5 Implementation

The most important design parameters listed below are adapted to fulfil typical audio applications:

- Dynamic range: 80 dB (13 to 14 bits)
- Signal-to-noise ratio: > 30 dB
- Sampling rate: 16 kHz
- Supply voltage: ± 1.25 V
- Input voltage range: ± 1.25 V - Vsat

The dynamic range determines a minimum value of the capacitors such that the sampled thermal noise kT/C remains below half an LSB. In order to reach a maximal dynamic range, the negative supply voltage is used as voltage reference. The minimal signal-to-noise ratio is achieved by keeping the amplifier's gain high enough and by a good capacitors matching. These points are not practical problems since, with a appropriate layout, a typical matching of some $^{0}/_{00}$ is easily fulfilled (leading to a signal-to-noise ratio of almost 50 dB). The amplifier's gain, expressed in dB, conducts in first approximation to the same signal-to-noise ratio limit.

The circuit is implemented in the ALP2 LV double metal, double poly, 2 µm CMOS technology from EM Microelectronic-Marin SA in Switzerland. The analog part is full custom layout and the digital part is realised using CSEL_LIB, a low power standard cell library developed at the CSEM SA, Neuchâtel, Switzerland.

The simulations exhibits a power consumption of 25 µW at 2.5V for the analog part of the A/D converter and the area is 0.06 mm^2 including the polarisation circuit.

Additional components are on the test circuit. One can find a D/A converter having the same "relative precision" as the A/D one, a track and hold output amplifier, the control logic, the serial-to-parallel and parallel-to-serial conversion circuit (figure 4 and 5).

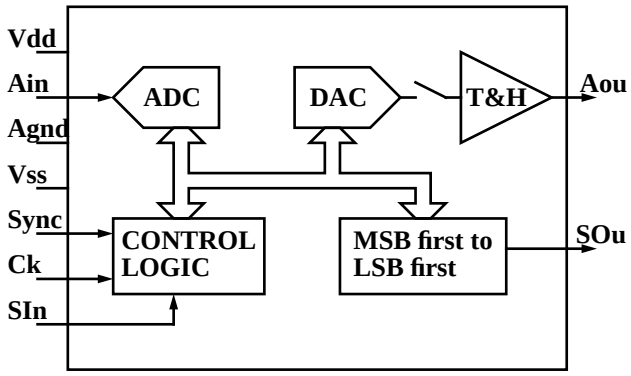

FIGURE 4. Bloc diagramm of the A/D and D/A chip

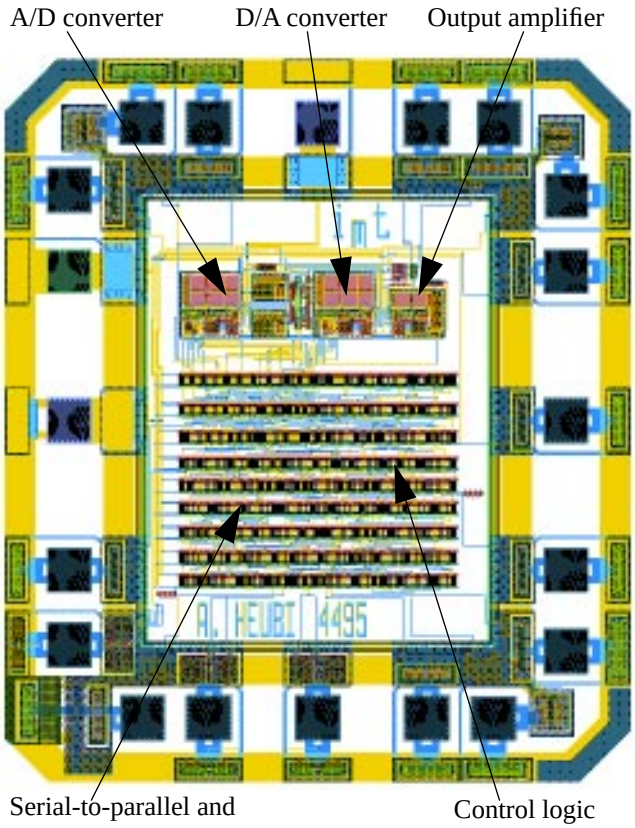

FIGURE 5. A/D and D/A chip layout

The whole circuit has an area of 4 mm^2 (≈ 5900 sq-mil) including pads and the core an area of about 0.8 mm^2.

The timing signals of the circuit are found on figure 6. The "ck" and "sync" signals controls the sampling frequency and the number of bits. The internal MSB first to LSB first registers are build to support a word length up to 15 bits. Thank to the serial ports, the number of pins can be limited to 9.

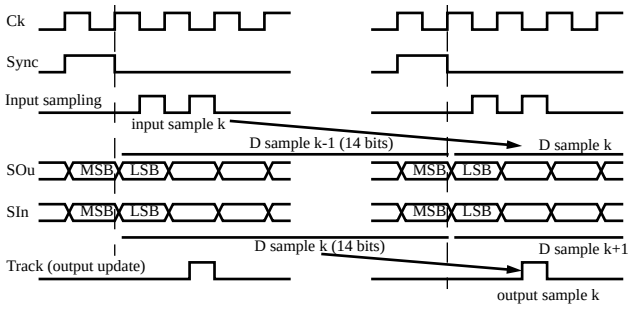

FIGURE 6. Timing of the A/D and D/A chip

Some test pads and auxiliary functions (for instance putting some parts in stand-by mode) are added.

6 Performances

The circuit is tested on a PC based environment equipped with a data acquisition card from National Instruments (AT-MIO-16E-1) driven with the LabVIEW software.

6.1 Power consumption

The circuit consumes at ± 1.2 V power supply and 16 kHz sampling frequency:

- 13 µA for the A/D converter (31 µW)
- 32 µA for the D/A converter and the track&hold circuit (75 µW)
- 7 µA for the logic part (17 µW)
- 125 µW total power dissipation
- < 1 µA in stand-by mode

The consumptions of the analog parts exceeds the simulated ones by about 20 %. This can result from technological parameter variations.

6.2 Noise floor

The noise floor of the A/D converter is measured at 16 kHz sampling frequency for reference voltages between 1 V and 2.5 V. The results are given in dB relative to the full scale (figure 7) and were measured with the input connected to ground.

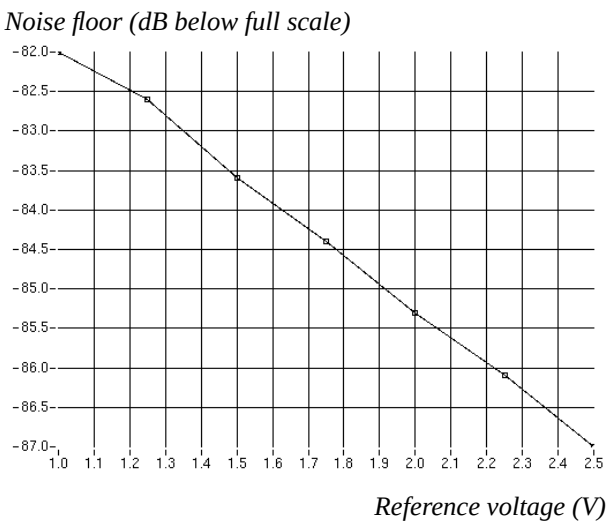

FIGURE 7. Noise floor versus reference voltage

These measures give the maximal dynamic range of the converter witch is about 13.5 bits at 1 V and 14.5 bits at 2.5 V.

6.3 Signal-to-noise ratio

The signal-to-noise ratios are measured with a 1 kHz sinusoidal input sampled at 16 kHz and ± 1.2 V power supply. The input was generated by the 12 bits D/A converter of the acquisition card, with 64 kHz sampling rate and variable reference voltage to reach the dynamic range.

The measurements (figure 8) of the Total Harmonic Distortion (THD) and THD + noise shows a saturation at about 60 dB SNR for large input levels and the same behaviour as a linear converter for low input levels as foreseen by the simulations (figure 3).

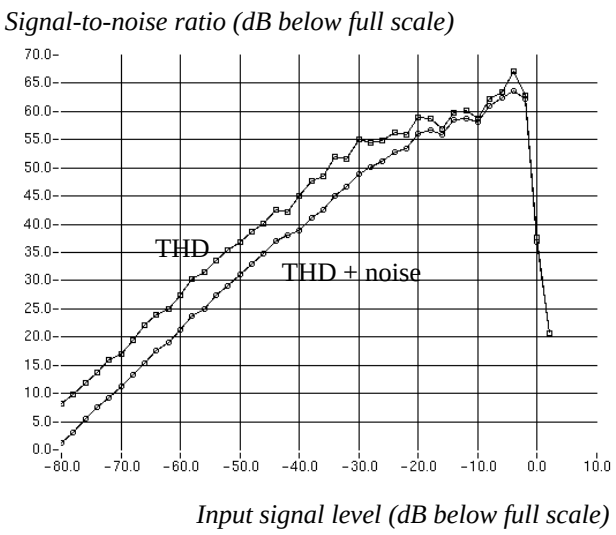

FIGURE 8. Signal to noise ratio versus input signal level

Finally figure 9 shows the AD converter's frequency response to a 1 kHz sinusoidal signal at - 25 dB below full scale.

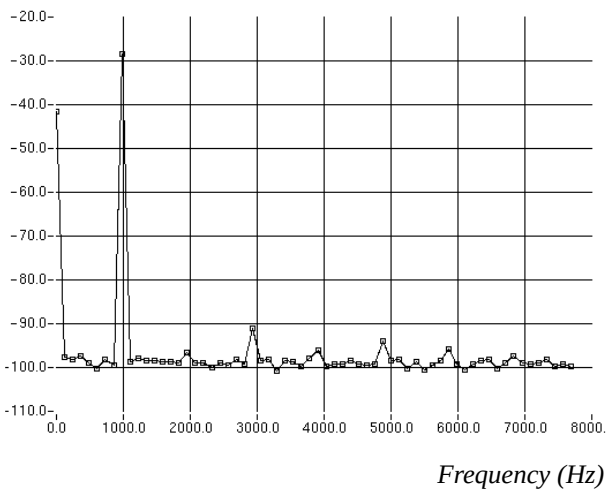

FIGURE 9. Frequency response to a 1 kHz input signal at -25 dB below full scale

It should be noticed that the measurements of this section gives worst case results due to the limitation of the sinusoidal source (12 bits DAC).

6.4 Others

a) Sampling frequency

The sampling frequency can be increased at the cost of a slight degradation of the maximal signal-to-noise ratio. The A/D converter works until 36 kHz at ± 1 V power supply and until 57 kHz at ± 2.5 V.

b) Power Supply Rejection Ratio (PSRR)

The PSRR was measured by modulating the positive supply voltage with a sinusoidal signal of 1 kHz and - 20 dBV level. The measured signal at the output of the A/D converter, supplied at ± 2 V, was equivalent to - 73 dBV, resulting in a PSRR of 53 dB at 1 kHz.

c) Temperature behaviour

The circuit has been used from - 40°C to + 100°C at ± 2.5 V power supply and worked for the whole range. The offset drift is - 32 µV/K (or a total offset change of 4.5 mV between - 40°C and + 100°C).

d) Yield

From a series of 119 chips, 113 worked correctly and were mounted in TSSOP-16 packages, resulting in a yield of about 95 %.

e) Analog ports characteristics

The analog ports have the following characteristics:

- Max input capacitance 10 pF
- Min dc input resistance 10 MΩ
- Max output impedance 200 kΩ

In many applications, the output has to be buffered due to its relative high impedance.

6.5 D/A converter

The D/A converter is not yet fully tested, but it works correctly. It has a dynamic range of at least 13 bits and a maximal signal-to-noise ratio of more than 50 dB.

7 Conclusion

The presented converters are well suited for audio applications where a large dynamic range is needed but only a relative precision is sufficient. They feature 13 to 14 bits dynamic range and a maximal signal to noise ratio of about 60 dB (≈ 10 bits).

For other applications, such as instrumentation, the offset and the non-linearity can be compensated by a digital circuit at the cost of less than 1 mm^2 extra area in a 2 µm technology and no significant increase in the power consumption.

Since the presented converter takes up very few silicon area and consumes only some µW, it becomes feasible to process signals digitally for many audio applications.

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Patent pending:

Registration number: 95 10 174

Title: “Dispositif de traitement numérique d’un signal analogique devant être restitué sous forme analogique”

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