Effects of Random MOSFET Parameter Fluctuations on Total Power Consumption[†]

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Abstract

Intrinsic fluctuations in threshold voltage, subthreshold swing, saturation drain current and subthreshold leakage of ultra-small-geometry MOSFET's due to random placement of dopant atoms in the channel are examined using novel physical models and a Monte-Carlo simulator. These fluctuations are shown to pose fundamental barriers to the scaling of supply voltage and channel length and thus, to the minimization of power dissipation in multi-billion transistor chips of the future. In particular, using the device technology and the level of integration projections of the National Technology Roadmap for Semiconductors for the next 15 years, standard-maximum deviations of threshold voltage, drive current, subthreshold swing and subthreshold leakage are shown to escalate to 40-600mV, 10-100%, 2-20mV/dec. and 10-10^8%, respectively, in the 0.07 mm, 0.9 V CMOS technology generation with 1.3-64 billion transistors on a chip. While these limits can be transcended to some degree by selecting optimal transistor width values larger than the channel length, the associated penalties in dynamic & static power, and in packing density demand novel MOSFET designs aimed at minimizing these fluctuations.

Introduction

Due to random microscopic fluctuations in the number and location of dopant atoms in the MOSFET channel region, the major device parameters, namely, threshold voltage, subthresold swing, drain current and subthresold leakage current fluctuate accordingly. This intrinsic fluctuation effect poses a fundamental barrier to further reductions of supply voltage and channel length, and thus, to the minimization of power in multi-billion transistor Gigascale Integration (GSI) chips [1,2]. Variations in threshold voltage of 0.1 mm MOSFET's due to concurrent fluctuations in the number of dopant atoms in the channel (intrinsic), oxide thickness (extrinsic) and channel length (extrinsic) have been investigated experimentally [3-5] and through numerical simulations of devices with only 10 to 30 distinct random dopant distributions [6-7].

In this paper, comprehensive analytical models for intrinsic random dopant placement-induced distributions in threshold voltage, subthreshold swing, drain current (linear and saturation) and subthreshold leakage current of sub-0.1 mm MOSFET's are presented. These models are derived from physical device analysis and validated through comparisons with device parameter distributions obtained from Monte-Carlo simulations of MOSFET's for more than 1000 distinct random dopant atom placements. The trade-offs between minimization of intrinsic random dopant fluctuation effect and power consumption (static and dynamic) are explored for the first time. The opportunity to optimize device structure to minimize the intrinsic fluctuation effect and power consumption is discussed. The limitations imposed by the fluctuation phenomena on the evolution of GSI are projected.

Device Parameter Distribution Models

The major equations of the device parameter fluctuation model are given below. Here, $F(n_a)$ is the probability density function that represents the distribution of effective channel doping concentrations among a number of "square" (equal channel width & length) bulk MOSFET's:

$$F(n_a)=\sqrt{\frac{2}{\pi^2(\alpha^2+\gamma^2)}}\left\{\frac{(\varepsilon_s\varphi_{B/q})^{1/4}}{N_a^{13/12}}\right\}\left[\exp\left\{-\frac{(p-\eta)^2}{2(\alpha^2+\gamma^2)}\right\}\right]\cdot$$

$$\left[1+\frac{\gamma(p-\eta)}{(\alpha^2+\gamma^2)}\left\{\frac{1-2p}{2L\sqrt[3]{N_a}\sqrt{p(1-p)}}\right\}\right]\left[\frac{\exp\left\{-\frac{(n_aXN_a^{-2/3}-XN_a^{1/3})^2}{2XN_a^{1/3}}\right\}}{1+\mathrm{erf}\left(\sqrt{\frac{XN_a^{1/3}}{2}}\right)}\right]$$

$$p=\frac{\mathrm{erf}\left(\frac{n_aXN_a^{-2/3}-XN_a^{1/3}}{\sqrt{2XN_a^{1/3}}}\right)+\mathrm{erf}\left(\sqrt{\frac{XN_a^{1/3}}{2}}\right)}{1+\mathrm{erf}\left(\sqrt{\frac{XN_a^{1/3}}{2}}\right)},\quad X=2\sqrt{\frac{\varepsilon_s\varphi_B}{qN_a}}$$

$$\alpha=0.149\exp(-0.0636LN_a^{1/3}),\ \eta=0.59,\ \gamma=\frac{\sqrt{p(1-p)}}{LN_a^{1/3}}$$

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I. Threshold voltage distribution function:

$$F_{V_{ts}} = \frac{W}{L}\left(1-\int_0^{n_a} F(t)dt\right)^{W/L-1} F(n_a)\times\frac{dn_a}{dV_{ts}}$$

$$V_{ts}(n_a) = V_{fb} + 2\varphi_B + \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_s n_a(\varphi_B+\varphi_f)} - \Delta V_{ts}$$

$\Delta V_{Tts}(n_a)$: from Ref.[7],

$$\varphi_f(n_a) = \frac{kT}{q}\ln\left(\frac{n_a+\sqrt{n_a^2+4n_i^2}}{2n_i}\right)$$

$$\varphi_B = \frac{kT}{q}\ln\left(\frac{N_a+\sqrt{N_a^2+4n_i^2}}{2n_i}\right)$$

II. Subthreshold swing distribution function :

$$F_S = \frac{W}{L}\left(1-\int_0^{n_a} F(t)dt\right)^{W/L-1} F(n_a)\times\frac{dn_a}{dS}$$

$$S(n_a) = \frac{kT}{q}\ln 10\left(1+\frac{t_{ox}}{\varepsilon_{ox}}\sqrt{\frac{q\varepsilon_s n_a}{2(\varphi_B+\varphi_f)}}\right)$$

III. Drain current distribution function:

$$F_{I_{ds}} = -\frac{W}{L}\left(1-\int_0^{n_a} F(t)dt\right)^{W/L-1} F(n_a)\times\frac{dn_a}{dI_{ds}}$$

$I_{ds}[\mu(n_a), V_{TS}(n_a)]$:from Ref.[9]

IV. Subthreshold leakage current distribution function:

$$F_{I_{leak}} = -\frac{W}{L}\left(1-\int_0^{n_a} F(t)dt\right)^{W/L-1} F(n_a)\times\frac{dn_a}{dI_{leak}}$$

$I_{leak}[\mu(n_a), V_{TS}(n_a), S(n_a)]$: from: Ref.[9]

n_a: variable channel doping, N_a: target channel doping

ε_s, ε_{ox}: Si & oxide permittivity, W: channel width

L: channel length, t_{ox}: gate oxide thickness

q: electronic charge, k: Boltzmann's constant

T: temperature, V_{fb}: flatband voltage, μ: mobility

n_i: intrinsic carrier concentration

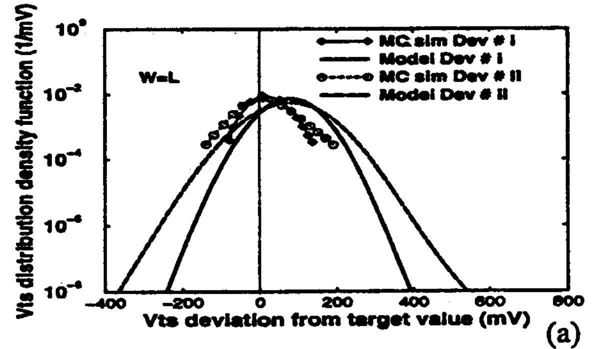
V_{ts}: threshold voltage, S: subthreshold swing

I_{ds}: drain current, I_{leak}: subthreshold leakage current.

Key features of the new analytical model equations for threshold voltage, subthreshold swing, drain current (linear and saturation) and subthreshold leakage current distributions are: 1) fluctuations of both the oxide field and the potential drop across the channel depletion region are included in the threshold voltage distribution; 2) effects of channel width on distribution characteristics are introduced; 3) the "cube approximation" introduced by Keyes [10] in a previous threshold voltage fluctuation model is eliminated and the theory of percolation in square arrays [10] is exploited; 4) fluctuations in carrier mobility are included in the drain current distribution; 5) the influence of Drain Induced Barrier Lowering (DIBL) [8] on the distribution of device parameters is incorporated, and 6) the distribution of dopant atoms among the microscopic volume elements in the channel is derived from first principles to be "Binomial" instead of "Poisson" [6,7,10]. The model predictions, *obtained without using any fitting parameters,* are in *good agreement* (Fig. 1) with parameter distributions obtained from Monte-Carlo simulations (using TMA MEDICI) of devices with more than 1000 (to yield 99% confidence level) distinct random dopant atom placements.

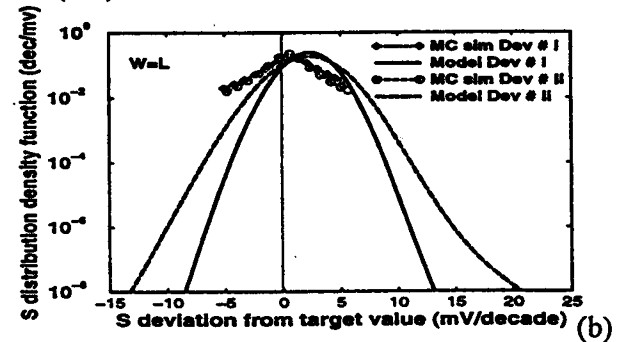
Physics of Parameter Fluctuations

Distributions of device parameters predicted by the new models and simulations (Figure 1) are shown to be predominantly asymmetric about the target values. As illustrated in Figure 2, the magnitude and nature of this asymmetry, particularly in the threshold voltage distribution, are influenced strongly by the degree of DIBL present in the target device, even in the absence of extrinsic variations in channel length or oxide thickness. For example, in target devices with negligible DIBL, the mean value of the threshold voltage deviates in the positive direction as expected from the inherent asymmetry 1) of the probability of conduction across a square array with respect to the fraction of "on" elements (as dictated by percolation theory [6]) and 2) of the "Binomial" or "Poisson" distribution of dopant atoms about the target value. However, when DIBL is dominant,



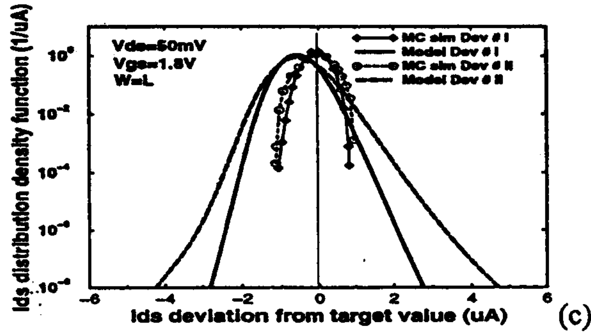
(a)

Device #	I		II		III	
	$\bar{V}_{ts}$	dV_{ts}	$\bar{V}_{ts}$	dV_{ts}	$\bar{V}_{ts}$	dV_{ts}
MC (mV)	1200	42	1147	58	945	34
Model (mV)	1165	56	1166	74	914	49



(b)

Device #	I		II		III	
	$\bar{S}$	dS	$\bar{S}$	dS	$\bar{S}$	dS
MC (mV/dec)	102	2.5	102	2.2	101	4.5
Model (mV/dec)	97	1.6	97	2	97	2

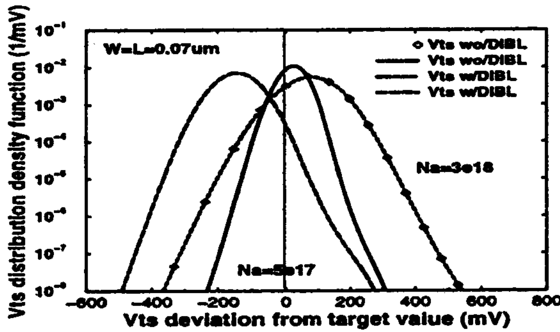


(c)

Device #	I		II		III	
	$\bar{I}_{ds}$	dI_{ds}	$\bar{I}_{ds}$	dI_{ds}	$\bar{I}_{ds}$	dI_{ds}
MC (mA)	3.8	0.28	4	0.36	4	0.38
Model (mA)	3.4	0.38	3.3	0.47	3.6	0.41

Fig. 1 Comparisons of MOSFET parameter distributions from Monte-Carlo (MC) simulations and analytical models: **(a)** threshold voltage ($\bar{V}_{ts}$: mean, dV_{ts}: standard deviation) **(b)** subthreshold swing ($\bar{S}$: mean, dS: standard deviation)**(c)** drain current ($\bar{I}_{ds}$: mean, dI_{ds}: standard deviation).

Device I: L= 0.1 mm, Na=3 X 10^{18} cm^{-3}
Device II: L= 0.07 mm, Na=3 X 10^{18} cm^{-3}
Device III: L= 0.1 mm, Na=2 X 10^{18} cm^{-3}



N_a (cm^{-3})	5 X 10^{17}		3 X 10^{18}	
L: 0.07 mm	$\bar{V}_{ts}$ shift	dV_{ts}	$\bar{V}_{ts}$ shift	dV_{ts}
with DIBL (mV)	-148	58	+81	75
without DIBL (mV)	+26	37	+81	75

Fig. 2 MOSFET threshold voltage distributions with & without DIBL effects

the mean threshold voltage shifts in the negative direction, explaining observations from previous simulations [5-6]. Furthermore, in the presence of DIBL, the device parameters are more sensitive to fluctuations in doping and more susceptible to enhanced shifts in the directions of smaller doping concentrations. Therefore *DIBL, even without dimensional variations, contributes to larger variance and asymmetry of the distributions.*

Figure 3 shows the subthreshold leakage current distribution. Even though mean of the subthreshold swing is larger than the target value, increase of the mean threshold voltage dominant which causes reduction of mean subthreshold leakage current.

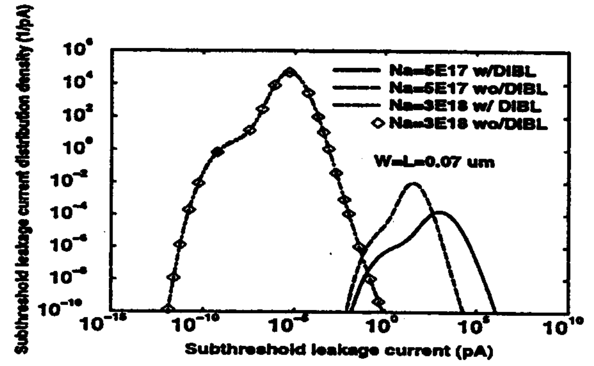
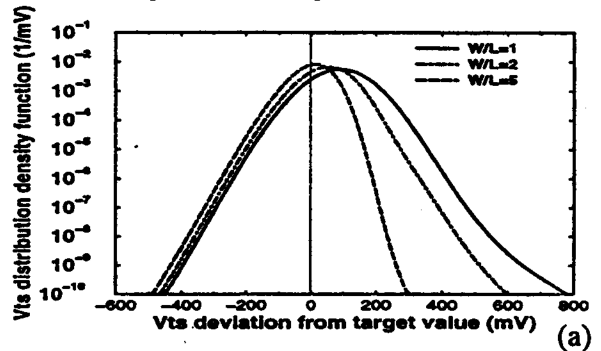
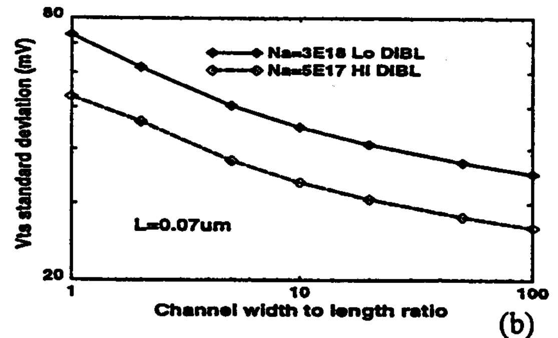


Fig. 3 Subthreshold leakage current distribution

Since this random dopant fluctuation poses a fundamental limit to supply voltage scaling [1,2], it is necessary to minimize this effect for minimum total power consumption. As shown in Figure 4, the standard deviation of threshold voltage reduces with increasing channel width since the total number of impurities in the channel volume increases. Thus, the device parameter fluctuations can be reduced to some extent by making the transistors wider. While smaller fluctuations achieved through larger device size enable further scaling of supply voltage, corresponding increases in the output load capacitance and subthreshold leakage current contribute to larger static and dynamic components of the power dissipation and to degradation of packing density. Therefore, there is an optimal value of channel width that allows the total power consumption and the fluctuation



(a)



(b)

Fig. 4 (a) Threshold voltage distribution for different aspect ratio. (b) Standard deviation of threshold voltage distribution for different aspect ratio.

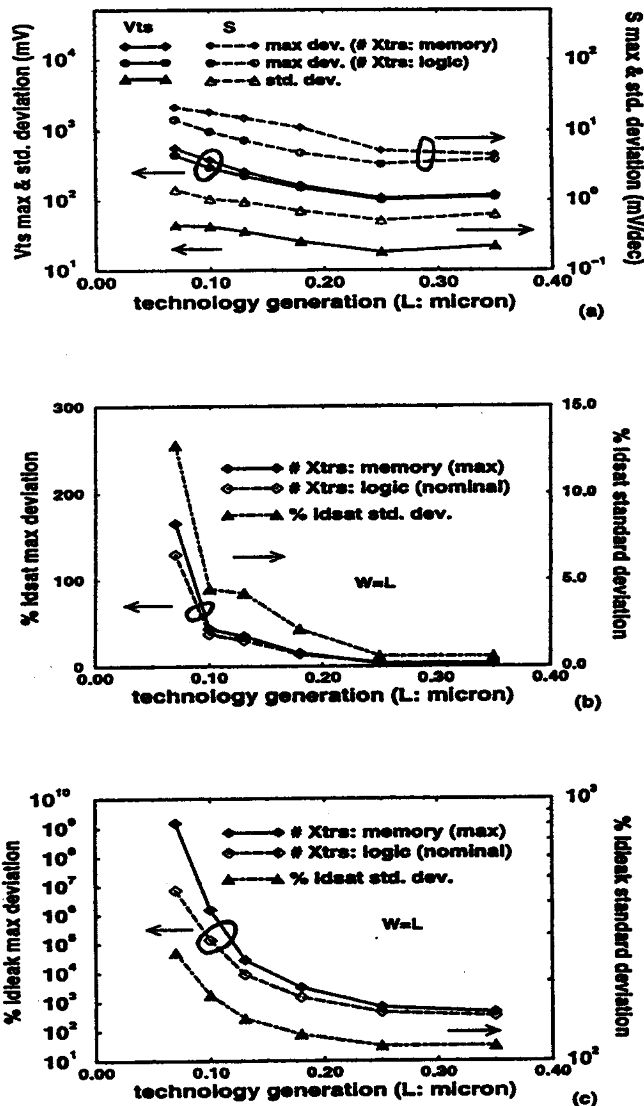


Fig. 5 Maximum and nominal MOSFET parameter fluctuations across technology generations.
(a) threshold voltage & subthreshold swing,
(b) drive current. (c) subthreshold leakage current.

Roadmap [11] below:

L: mm (Year)	0.35 (1995)	0.25 (1998)	0.18 (2001)
oxide thickness (nm)	10	5	4.5
supply voltage (V)	3.3	2.5	1.8
# Xtrs (logic-memory)	12 - 64 M	31 - 256 M	93 M - 1 G
L: mm (Year)	0.13 (2004)	0.1 (2007)	0.07 (2010)
oxide thickness (nm)	4	3.5	3
supply voltage (V)	1.5	1.2	0.9
# Xtrs (logic-memory)	225 M - 4 G	450 M - 16 G	1.3 - 64 G

of device parameters to be minimized simultaneously. In addition, reduction of the effective gate insulator thickness and selection of suitable doping profiles in the target MOSFET channel provide more promising alternatives to minimizing these fluctuations.

Using the device technology and level of integration projections from the Technology Roadmap for Semiconductors [11] for the next 15 years, random variations of threshold voltage, subthreshold swing, drive current and leakage current in bulk MOSFET's are shown to escalate to unacceptable proportions (Fig. 5) in the sub-0.1 mm GSI era, thus demanding new device designs aimed at minimizing these fluctuations and total power consumption simultaneously.

Conclusions

Novel and accurate physical models for random MOSFET parameter fluctuations are established. The models enable insightful analysis of the interactions between random dopant placement and DIBL as well as total power consumption, and allow efficient exploration of the limitations imposed on functionality, gain, delay and power of circuits using sub-0.1 mm GSI technology. While these limits can be transcended to some degree by selecting optimal transistor width values larger than the channel length, the associated penalties in dynamic & static power, and in packing density demand novel MOSFET designs aimed at minimizing these fluctuations.

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