Short Circuit Power Consumption of Glitches[1]

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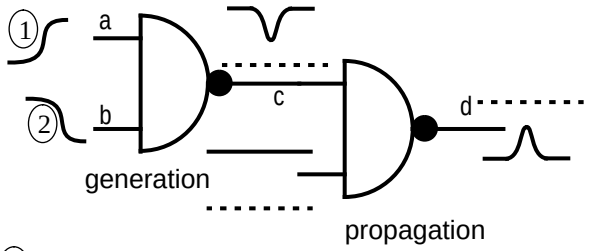
Abstract

Short circuit currents are analyzed for glitch and glitch-free cases within this paper. Within the glitch power-formulas introduced in literature short circuit power consumption is neglected. We examined that short-circuit power consumption contributes more significantly to a gate-transition's total power consumption for glitches than for common complete transitions. Simulation results are presented which exemplify that generated and propagated glitches can lead to excessive power consumption (between 10% and 60% of its total power consumption for typical cases). These examinations can be used for accurate glitch power modelling and circuit optimization on gate level, which is particularly important for arithmetic and DSP circuits.

1 Introduction

Recently the conventional two dimensional design-space (area;time) has been enlarged to handle submicron and deep submicron designs by a third dimension: *Power consumption* [1,5].

Within design for low power the power consumption of a certain design solution needs to be evaluated. The power consumption of currently used static CMOS-technologies is dominated by dynamic power consumption (except for very low-voltage technologies), i.e. the circuit activities need to be analysed. Precise simulation tools on circuit level (like SPICE) can not handle the complexity of large circuits and huge number of possible stimuli. For this reason the power calculation is based on circuit activity analysis at logic level. Good surveys on power estimation are given in [2,3]. In order to precisely calculate energy consumption the logic node transitions must be examined carefully. It is important to note that multiple transitions within one clock cycle and glitches significantly influence power consumption [8,9] (typically around 15-20% but in arithmetic units up to 65%[13]). This influence strongly depends on the architecture. Within this paper a glitch is defined as a pair of two or more colliding output waveforms which are so close together that the corresponding voltage waveform neither reaches V_{SS} nor V_{DD} in between (cf. fig. 1). A glitch might



(1) this slope is called the glitch setting input-slope

(2) this slope is called the glitch resetting input-slope

Fig. 1: Glitch generation and propagation

even have a peak-voltage which is less than the common logic threshold-voltage (typically around 50% V_{DD}). The energy consumption of a glitch is not identical to that of the underlying complete transitions and hence must be calculated differently. For power modelling the main focus is put on dynamic charging of capacitors [1,10,11,12]. Within this paper we will show that for glitch power modelling this approximation does not hold.

In the next section the calculation of power consumption of static CMOS circuits on gate level is reviewed and its limitations are pointed out. Simulation results are presented in section 3. In section 4 conclusions are drawn.

2 Power-Calculation of static CMOS

The power consumed by a gate is generally defined as the amount of power drawn from the power supply. The average power consumption of a single CMOS gate can be divided into three parts:

$$P = P_{leakage} + P_{SC} + P_{Cap} \quad (1)$$

The power consumption due to leakage currents is much smaller than the other two dynamic components and hence is often neglected within power calculation. This is true except for very low voltage-technologies and as a consequence for very low threshold voltages [5]. During switching a conducting path through the pullup- and pulldown-network of a gate is present and as a consequence a short-

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circuit current is occurring. The third component is the capacitive power consumption which takes into account the capacitive charging of switched capacitors.

The calculation of the short-circuit power consumption is done by $\overline{I_{SC}} \cdot V_{DD}$. Primarily $\overline{I_{SC}}$ depends on the input-slope(s) of the transition causing input-pin(s). The capacitive charging and discharging current waveform through the block, which is turning on, limits the short circuit current. For this reason the short-circuit current is hard to determine within a simple expression[6,7]. If capacitive effects are considered, according to [7] the short circuit power is only 30% compared to not considering these effects for typical cases (i.e. equal input and output slopes). Within this paper we will therefore investigate this component by means of circuit level simulations (cf. section 3).

Due to two complete transitions (one from 0→1 and one from 1→0) the capacitive energy $C_L \cdot V_{DD}^2$ is drawn from the power supply. The energy $1/2 \cdot C_L \cdot V_{DD}^2$ is associated with each transition. However it should be noted that fanin-capacities, which significantly contribute to C_L, vary by approximately 20-25% due to gate-internal and other terminal-voltages [15].

If incomplete transitions occur instead of complete transitions the energy, which is drawn from the power supply by each incomplete transition, is:

$$E_{Glitch\_Cap} = \frac{1}{2} \cdot V_{DD} \cdot |Q_{Cap}| = \frac{1}{2} \cdot V_{DD} \cdot C_L \cdot |\Delta V| \quad (2)$$

Equation 2 also holds for complete transitions with $\Delta V = V_{DD}$. Capacitive power calculation is straight forward:

$$P_{Cap} = \frac{1}{2} \cdot V_{DD} \cdot C_L \cdot \lim_{T \to \infty} \frac{\sum_i |\Delta V_i|}{T} \quad (3)$$

The sum $\sum \Delta V_i$ can be obtained by logic simulation over a *sufficient* time-interval [14] using the glitch model presented in [1]. Equation 3 holds for all kinds of glitches (i.e. also for glitches which consist of more than 2 incomplete trans.).

3 Simulation results

As a typical example for simulation purposes we focus on a NAND2-gate of an industrial 3.3V-library within this paper. Using special testbenches and procedures, short-circuit power consumption was extracted for glitch free cases, glitch generation and glitch propagation. The results are presented and discussed in the following subsections.The behaviour of other single stage CMOS gates is similar, because in case of output transitions a pair of n- and p-channel transistors switches. Any other transistor in parallel (series) will have higher (lower) impedances during switching.

3.1 Glitch free cases

Generally the time a short circuit path is present through the pullup- and pulldown network is proportional to the input-slope's steepness. On the other hand the charge and discharge of fanout-capacitor C_{FO} and internal capacitors limits the short-circuit charge Q_{SC}. I.e. for a fixed input-slope the short-circuit charge decreases with an increasing fanout capacitor C_{FO}. The short-circuit charge's contribution to the total charge, which indicates the error if the short-circuit power consumption is neglected within power calculation, has been investigated. For this comparison we divided the capacitor C_{FO} into 2 equal parts: one towards V_{DD} and one towards V_{SS}, which is more realistic than lumping the whole capacitor towards V_{SS}. Hence only half of C_{FO} is charged during a falling respectively a rising output-slope. The short-circuit's charge-contribution ranges from 90% for slow input-slopes and C_{FO}=0 to approximately 0% for fast input-slopes and/or high values of C_{FO}.The cases with equal input-rise and output-fall times result in contributions of about 3% of the total charge. These results are in agreement with [6,7]. Hence the short-circuit power consumption is negligible for *well designed* cases with equal input- and output- rise and fall times. However, it should be noted, that in combinational circuits it is impossible to always ensure such well designed cases due to different fall- and rise-times of a gate, different input-slopes at different input-pins and so on. Hence short-circuit power consumption may not always be neglected.

3.2 Glitch generation

For generated glitches the influence of the short-circuit behaviour dramatically depends on the glitch peak voltage and the resetting input-slope (cf. fig. 1). We will discuss the characteristic short-circuit behaviour on the basis of the simulation results (fig. 3) of the testbench (fig. 2). The case

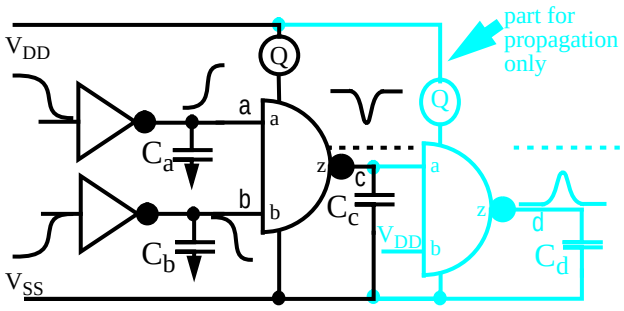

Fig. 2: Testbench for glitch generation and propagation

C_a=100fF, C_b=300fF and C_c=150fF would result in approximately equal input-rise (input-fall) and output-fall (output-rise) times if no collision occurs.

The basic difference of the short-circuit behaviour between the glitch- and glitch-free case is the role of the capacitive charging current. For glitches the resetting input-slope is in the *short-circuit region* ($V_{thn} < V_b < V_{DD} + V_{thp}$) while no significant charging-/discharging current of the output load C_{FO} is occurring, i.e. the output-voltage does not significantly change (cf. time interval τ in fig. 4). Hence during this time the short-circuit current is not limited by any charging/discharging current. For this reason the short-

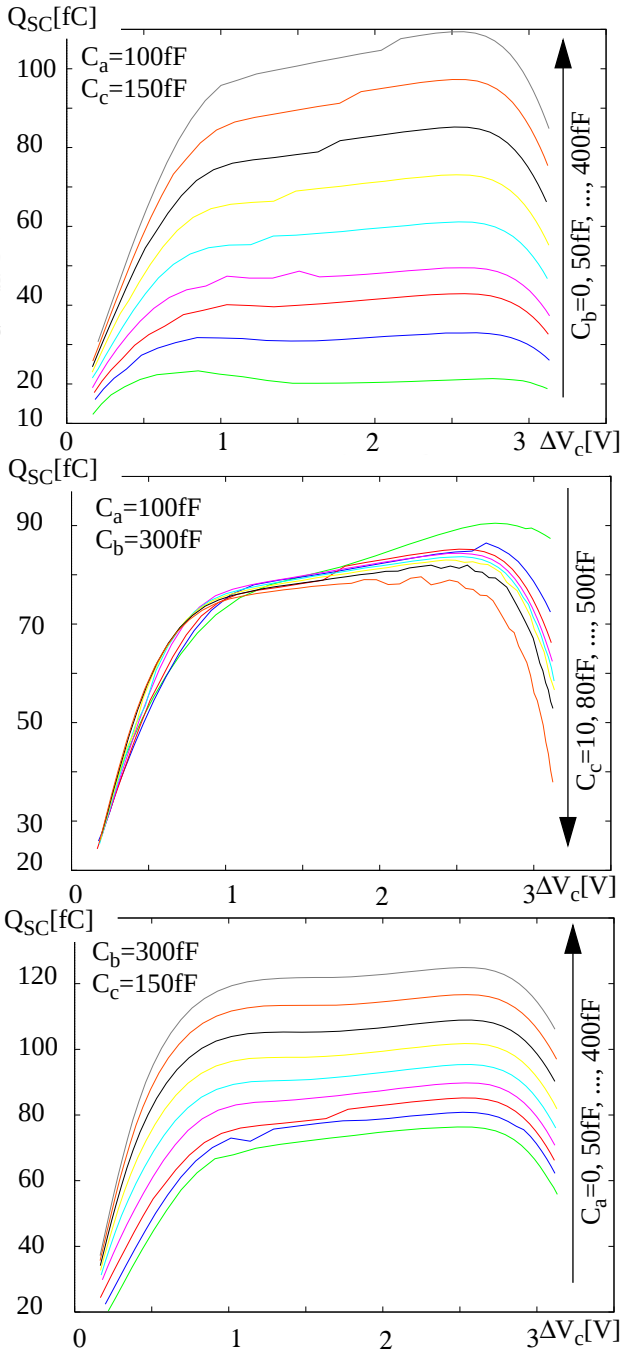

Fig. 3: Short circuit charge as a function of generated glitch peak voltage

circuit-current is even higher for glitches than for the two respective non-colliding input-transitions.

This basic behaviour can also be observed from the plots in fig. 3. The middle plot shows that short-circuit power consumption almost doesn't depend on the capacitive load for glitches with glitch-peak voltages lower than 2.5 V. The great impact of the resetting input slope can be observed from the upper plot. The impact of the setting input-slope is much lower (cf. lower plot). Within all plots

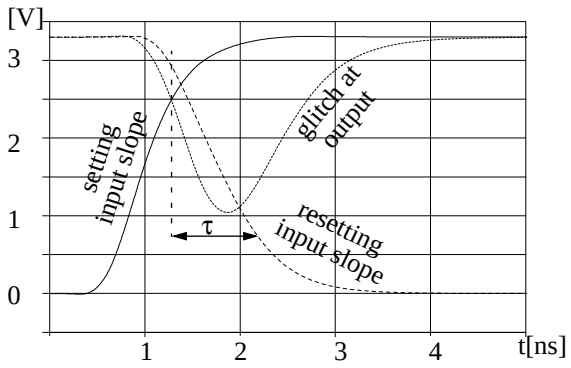

Fig. 4: Region of possible short-circuit currents caused by the resetting input slope

glitches with their peak-voltage between about 1V and 2.5V have an almost constant short-circuit charge (resp. power) consumption. For glitch-peak voltages lower than 1V the resetting input-slope starts before the setting input-slope has reached $V_{DD}+V_{thp}$. In fig. 5 the relative contribution of the short-circuit-current is plotted. The short-circuit's contribu-

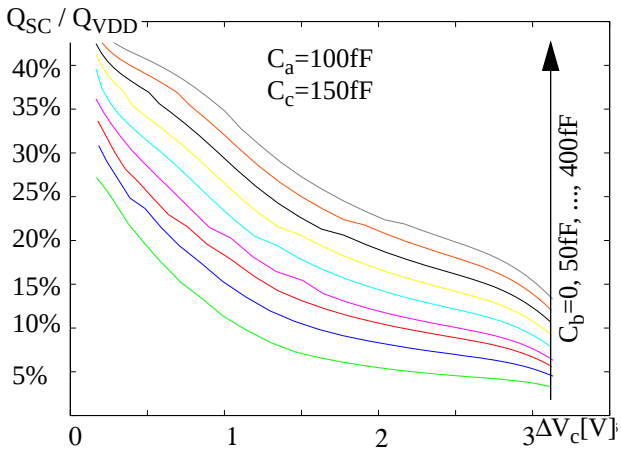

Fig. 5: Relative contribution of the short-circuit charge to the total charge Q_{VDD}

tion is hence significantly higher than for non colliding signal transitions (cf. section 3.1).

3.3 Glitch-Propagation

A glitch which drives an input-pin of a consecutive gate, might be propagated if the output is *sensible* to that input-pin (cf. fig. 1).

There are two reasons why the short-circuit charge might be significantly higher than for two complete transitions at the input-pin. On the one hand the input-voltage might be - due to its commonly flat glitch-peak waveform - in the short-circuit region ($V_{thn}<V_b<V_{DD}+V_{thp}$) for a comparatively long time. On the other hand the capacitive current, which is commonly limiting the short circuit-current for non colliding input-transitions, is quite low, when the glitch-peak voltage at the gate's output is reached. Hence the short-circuit charge strongly depends on the input-volt-

age when the glitch-peak is reached at the gate's output. This later effect was already observed for glitch-generation in section 3.2.

These basic glitch-propagation characteristics are exemplified by simulation results now. In fig. 6 the short-

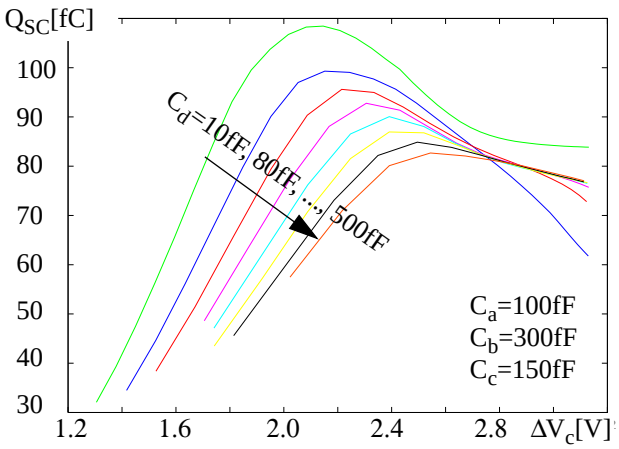

Fig. 6: Short-circuit load over input-glitch peak-voltage for equal input-glitch waveforms and different output-loads

circuit charge is plotted over the input-glitch peak for different output-loads C_d. As the load-capacitor C_c is constant the glitch waveforms are all equal for the same input peak-voltage. The maximum short-circuit charge is reached for each value of C_d, if the input-voltage is in the most critical short-circuit region, i.e. the sum of pullup- and pull-down impedance has a minimum value, when the output glitch reaches its peak-voltage. Hence for high load capacitors C_d the maximum short-circuit charge is reached for large input-glitches. Note that the most critical short-circuit region is always reached when the input-glitch's voltage returns to its initial value.

The high impact of the input-voltage when the output reaches its maximum is also visible in fig. 7. In this figure

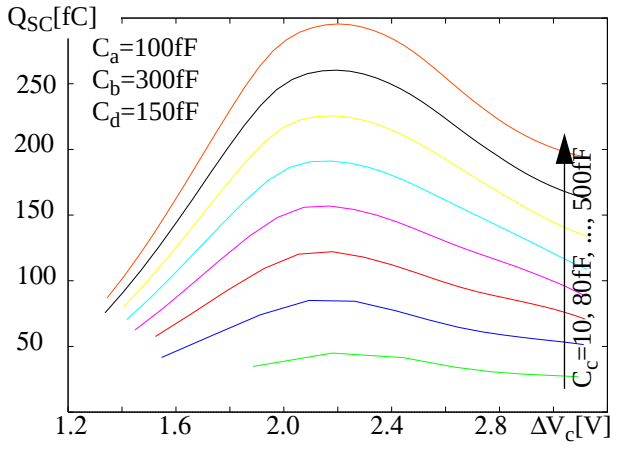

Fig. 7: Short-circuit load over input-glitch peak-voltage for different input-glitch waveforms and equal output-loads

the load capacitor C_d is fixed for all curves and the width of the input glitch is varied by different values for C_c. The maximum short circuit-charge is not reached for the cases in which the input-glitch is in the short-circuit region for the longest time but for the cases in which the output-glitch is reached while the input-glitch is in the most critical part of the short-circuit region.

The relative contribution of the short-circuit charge to the total consumed charge has been investigated again for typical circuit configurations. Depending on the input respectively output glitch-peak the short-circuit's contribution is in the range of 60% for small glitches and 15% for large glitches.

4 Conclusions

Within this paper the impact of the short-circuit power consumption has been investigated for glitch-free and glitch cases. For glitch-free cases the short-circuit's contribution to the total power consumption of a transition is about 3% and hence may be neglected for *well designed* circuit configurations (i.e. equal input and output rise/fall times). However, for cases with slower input-slopes than output-slopes its contribution can be up to 90%. For glitches the short circuit's contribution to the total power consumption is between 10% and 60% for typical cases and hence may not be neglected within the glitch-power calculation.

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