A 1-V 1-Mb SRAM for Portable Equipment

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Abstract

Low-power and high-speed circuit techniques are described for 1-V battery operated SRAMs. A design concept is shown that uses two kinds of MOSFETs different in threshold voltages to reduce power dissipation due to the subthreshold leakage current in both standby and active modes. We propose a step-down boosted wordline scheme to reduce power dissipation in the memory array to 57% while accelerating the sensing speed. A novel bidirectional differential internal-bus architecture provides data transmission that is 45% faster than in the conventional architecture, yet without area or power penalty. A charge-recycling I/O buffer incorporating a data transition detector reduces the power dissipation of the I/O buffer by 30%. A 1-Mb SRAM designed using these techniques and 0.5-μm CMOS technology demonstrated 4.8-mW power dissipation and a 75-ns address access time with standby power of 1.2-μW at a 1-V power supply.

1 Introduction

Low-voltage digital signal processors (DSPs) have been developed for battery-operated portable equipment [1-2]. To create high-performance systems using these DSPs requires the development of low-power external memories. SRAM macrocells based on MTCMOS technology [3] and a cache memory using low-Vth MOSFETs in the peripheral circuitry [4] have been proposed for 1-V high-speed operation. However, these techniques are not suitable for low-power high-speed large-scale memories [5] because the subthreshold leakage current in the active mode is estimated to exceed the sub-mA level, amounting to 10 to 20% of the total active power. For long battery life, power consumption including leakage current must be reduced in not only standby but also active mode.

In this paper, we describe a design concept that reduces leakage current in both standby and active modes, and propose a step-down boosted wordline scheme, a novel bidirectional differential internal-bus architecture, and a charge-recycling I/O buffer incorporating a data transition detector. We also present experimental results for a 1-Mb SRAM fabricated using 0.5-μm single-polysilicon triple-metal CMOS technology.

2 Circuit Techniques

2.1 Design concept for low-power and fast memories

In memory LSIs, the critical path for read-out and data-write is clear because almost all nodes are controlled by address and $\overline{\mathrm{WE}}$-signal. It is thus possible to reduce the leakage current and access time by using the design concept shown in Fig. 1. A high-Vth MOSFET is applied to the cascode-connected MOSFET connected to the power or ground line directly. This is an effective way to suppress the threshold-voltage increase in high-Vth MOSFETs due to the bodyeffect. To reduce area, high-Vth MOSFETs Q_A and Q_B are shared among logic gates that have the same input through a local powerline. High-Vth MOSFETs are applied on the non-critical paths, and low-Vth MOSFETs are applied on the critical path. This reduces delay time in the critical path and cuts off leakage current in all logic gates except those on the critical path. Drivers, consisting of a low-Vth Pch MOSFET and a high-Vth Nch MOSFET, are applied to achieve large drivability for heavy capacitance loads. Their output is set high to cut off leakage current during standby.

A main-decoder configuration based on this concept is shown in Fig. 2. The outputs of the address-bus drivers

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are set high during standby. A conventional NAND gate is not applicable because the leakage current of the Pch MOSFETs is not cut off in this situation. In the NAND gate in Fig. 2, Q1's source node is connected to an address bus and Q2 is controlled by the reverse signal. The NAND gate therefore has no leakage path during standby. Since the main-decoder is not on the critical path for memory-cell access, high-Vth Nch MOSFETs can be used in all of the cascode-connected MOSFETs in the NAND circuit to reduce leakage current in the address decoding.

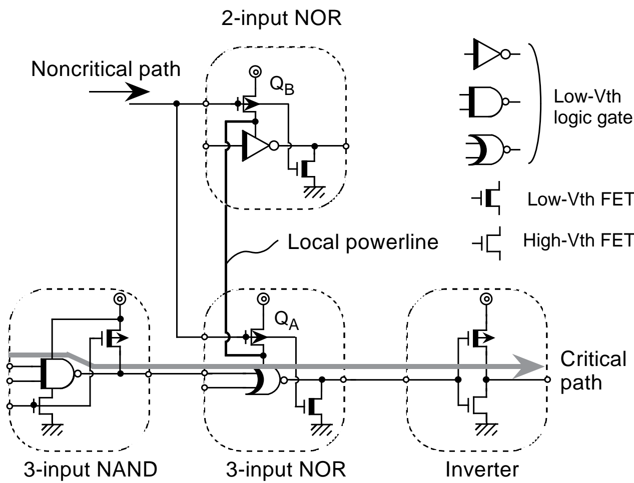

Fig. 1. Design concept for low-power and fast memories.

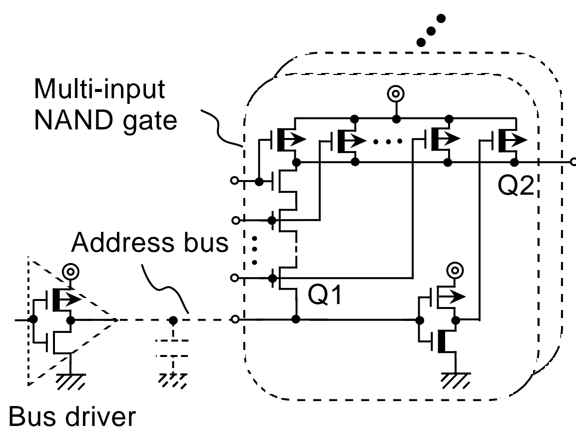

Fig. 2. Main decoder.

2.2 Step-down boosted wordline scheme

Memory cells are composed of high-Vth MOSFETs to reduce leakage current. Although it is possible to use the boosted wordline technique to reduce access time, using it increases the power dissipation in the memory array. We thus propose a step-down boosted wordline scheme to reduce the power dissipation while accelerating sensing speed. This scheme is shown in Fig. 3.

The scheme features a boosted-pulse generator and wordline voltage selectors. The boosted voltage is generated using metal-insulator-metal (MIM) capacitors. These capacitors are embedded along the word driver array to get enough capacity and to reduce area by using a capacitor electrode as a transmission line of the boosted voltage. The selected-wordline voltage is controlled by Q3 and Q4. To activate Q3, the boosted voltage is applied to the gate node to prevent Vth drop. The boost period is determined by the width of the address transition detection (ATD) pulse. Except in the circuit selected by the main-wordline, the leakage current is cut off by the high-Vth MOSFETs.

A simulated waveform of the sub-wordline is shown in Fig. 4. At the beginning of memory-cell access, the

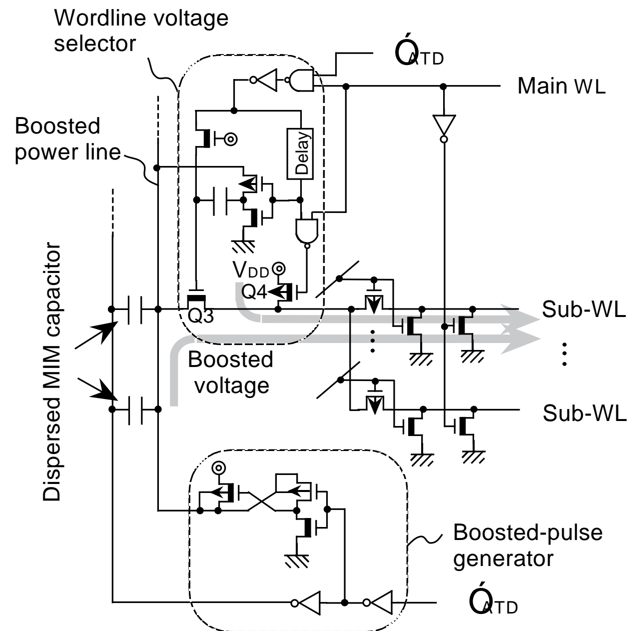

Fig. 3. Step-down boosted wordline scheme.

wordline is boosted to more than 1.4 V at a 1-V power supply. Since the memory-cell drivability is improved by a factor of two, the bitline transition is accelerated. After the sensing operation, Q3 is turned off and Q4 is turned on. The wordline voltage is then set to the supply voltage. This scheme is useful for reducing the power consumption in the memory array because the cell current is reduced by half after the stored data are output to the bitlines. Figure 5 shows the current consumption for various operating frequencies. The simulation results indicate that the power dissipation can be reduced by 43% at 10-MHz compared with a conventional boosted wordline scheme.

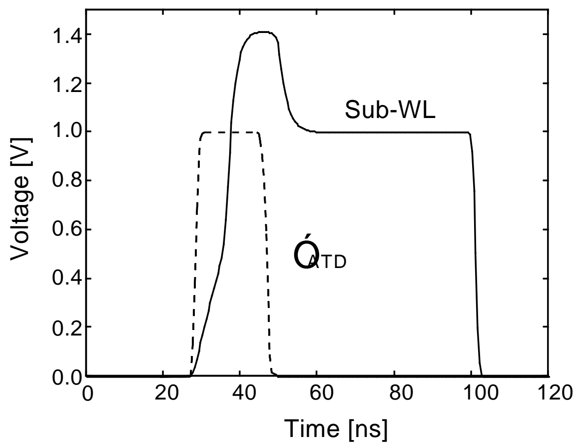

Fig. 4. Simulated waveform of sub-wordline.

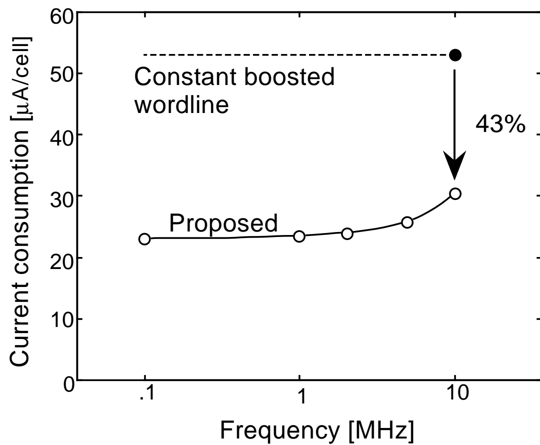

Fig. 5. Current consumption of a selected memory cell.

2.3 Low-Power differential internal-bus architecture

Differential data transmission can be used to decrease the delay time between a memory array and I/O buffers. It is important to reduce both the area and the power dissipation. Our proposed differential internal-bus architecture is shown in Fig. 6.

The bidirectional transmission contributes to area reduction. However, the conventional bidirectional buffer increases stray capacitance because both the driver and receiver are connected to the data bus. Our bidirectional buffer features Q5 and Q6, which work as pull-down transistors during write operations and as transfer gates during read operations. The input capacitance of the receivers is thus separated from the data bus. Furthermore, this architecture consumes no static current. A high-level signal, which is provided through a data-transmission line, controls the gate-input Pch MOSFET and the source-input Nch MOSFET in the receiver to the off-state, cutting the current path from V_{DD} to the ground.

Figure 7 shows the relationship between delay time and current consumption at 10-MHz operation. The proposed architecture reduces delay time to 55-60% in contrast to a conventional single-rail transmission with the same current consumption .

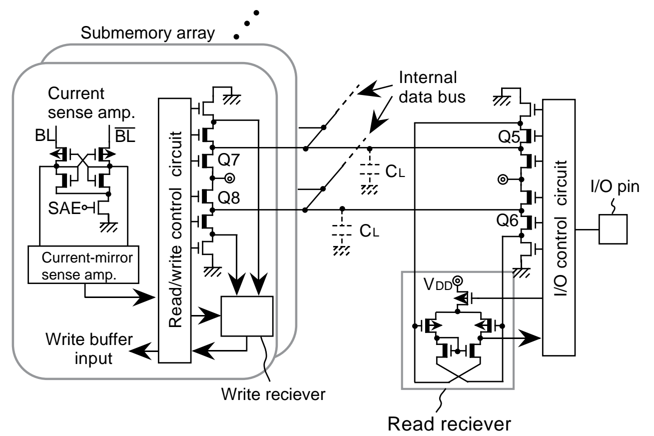

Fig. 6. Differential internal-bus architecture.

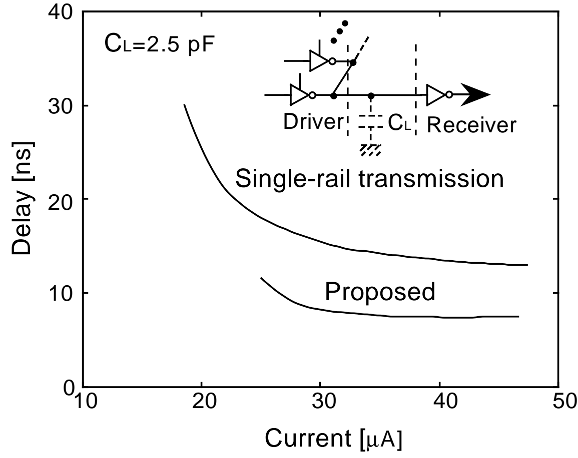

Fig. 7. Relationship between delay time and current consumption.

2.4 charge-recycling I/O buffer

A CMOS interface is used to reduce the power dissipation due to the static current. It is necessary to enhance the drivability of the output buffer and to cut off the leakage current during high-impedance mode because the I/O buses have large stray capacitance of 30-100 pF. It is also important to reduce the dynamic power dissipation in the I/O buffer.

Low-Vth PMOS pull-up are not suitable for use in the output buffers because current leakage into bus stray capacitance is inevitable in high-impedance-mode operation. Figure 8 shows an output buffer configuration for low supply voltages. A low-Vth Nch MOSFET with a boosted gate voltage is employed as a pull-up transistor. When the output buffer is in high-impedance mode, the source-node potential of the Nch pull-up transistor gets higher than the gate potential because of leakage current. This causes reverse bias across the gate-to-source, increasing the threshold voltage due to the bodyeffect. Therefore, leakage current to the bus capacitance is cut off. The high-Vth Pch MOSFET is employed to guarantee high-level output because the boosted voltage falls off gradually due to leakage current.

Our new charge-recycling I/O buffer is shown in Fig. 9. It features a bus-data transition detector. Each I/O pin is connected to a charge-recycling line through an equalizing transistor. The bus data are monitored by

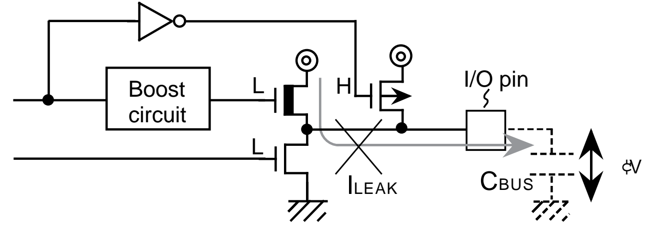

Fig. 8. Output buffer for low supply voltages.

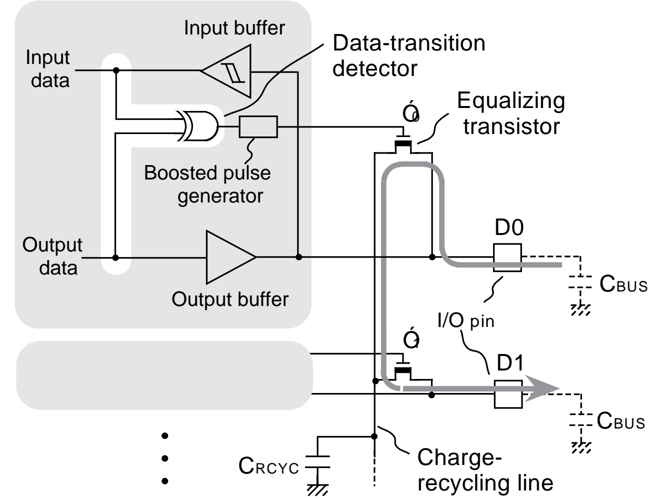

Fig. 9. Charge-recycling I/O buffer.

Schmidt-type input buffers. The equalizing transistor is activated in the I/O buffer that output data different from the bus data; and it is not activated in the I/O buffer whose output data is the same as the bus data. A charge on the bus transiting from high to low is recycled to a charge on the bus transiting from low to high through the charge-recycling line. Since the charge is recycled only among I/O buffers that transit data, power dissipation is reduced efficiently. To enhance recycling efficiency for timing skew, capacitor C_{RCYC} is added to the charge-recycling line.

Figure 10 shows the simulated waveforms of the I/O buffer; ϕ_0 and ϕ_1 are equalize pulses boosted to more than 1.6 V at a 1-V power supply. The charge on the D0 bus is recycled to the D1 bus. Charge recycling achieves, in theory, a maximum efficiency of 50%. The pulse width for charge recycling is set to 5 ns to suppress access time increase. Therefore, the recycle efficiency of this circuit is about 30%.

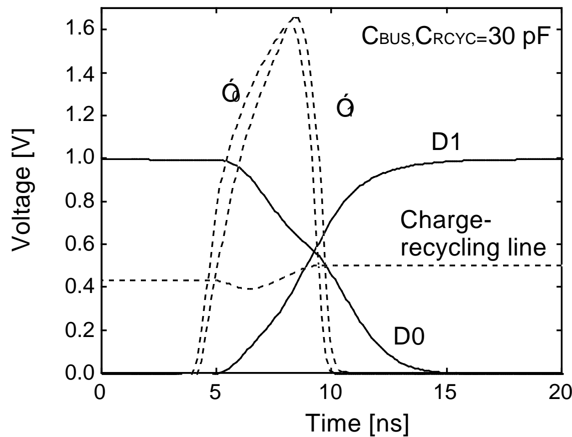

Fig. 10. Simulated waveforms of I/O buffer.

3 Experimental Results

We have designed a 1-V operation 1-Mb SRAM, using 0.5-μm CMOS technology, to confirm the circuit techniques discussed in this paper. Current sense amplifiers were adopted to reduce the sensing delay. Total simulated power dissipation during a read cycle (Fig. 11) was reduced to 77% by using a step-down boosted wordline scheme and charge-recycling I/O buffers.

A microphotograph of the test chip is shown in Fig. 12. The chip size was 16-mm$\times$12.65-mm. The operating waveforms are shown in Fig. 13. The measured address-access time was 75-ns. Power consumption at 10-MHz operation with 30-pF load was 3.6 mW in the write cycle and 4.8 mW in the read cycle. A low standby power of 1.2-μW was achieved by using high-Vth MOSFETs. These power dissipations were low enough to guarantee long battery life. Table 1 summarizes the chip characteristics.

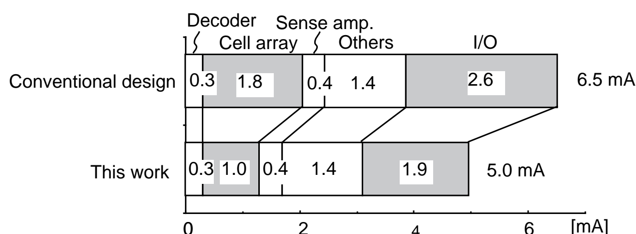

Fig. 11. Power dissipation during read cycle.

Table 1. Chip characteristics.

Process technology	0.5-µm CMOS single-polysilicon triple-metal MIM capacitor
Gate length	
High-Vth FET	0.55 µm
Low-Vth FET	0.65 µm
Gate oxide	11 nm
Threshold voltages	
N-ch FET	0.25 V, 0.55 V
P-ch FET	-0.35 V, -0.65 V
Cell size (pure CMOS)	11µm ~10 µm
Chip size	16 mm ~12.65 mm
Organization	64 Kwords ~16 bits
Supply voltage	1 V
Address access time	75 ns
Power dissipation (@ 10 MHz)	3.6 mW (write) 4.8 mW (read)

4 Summary

We have described a design concept for reducing leakage current in both the active and standby mode for 1-V battery-operated SRAMs. A step-down boosted wordline scheme, a novel bidirectional differential internal-bus architecture, and a charge-recycling I/O buffer with a data-transition detector were proposed. The measured power consumption and address access time were 4.8-mW and 75-ns, and the standby power of 1.2-μW was achieved for a 1-V 1-Mb SRAM fabricated using 0.5-μm CMOS technology.

Acknowledgment

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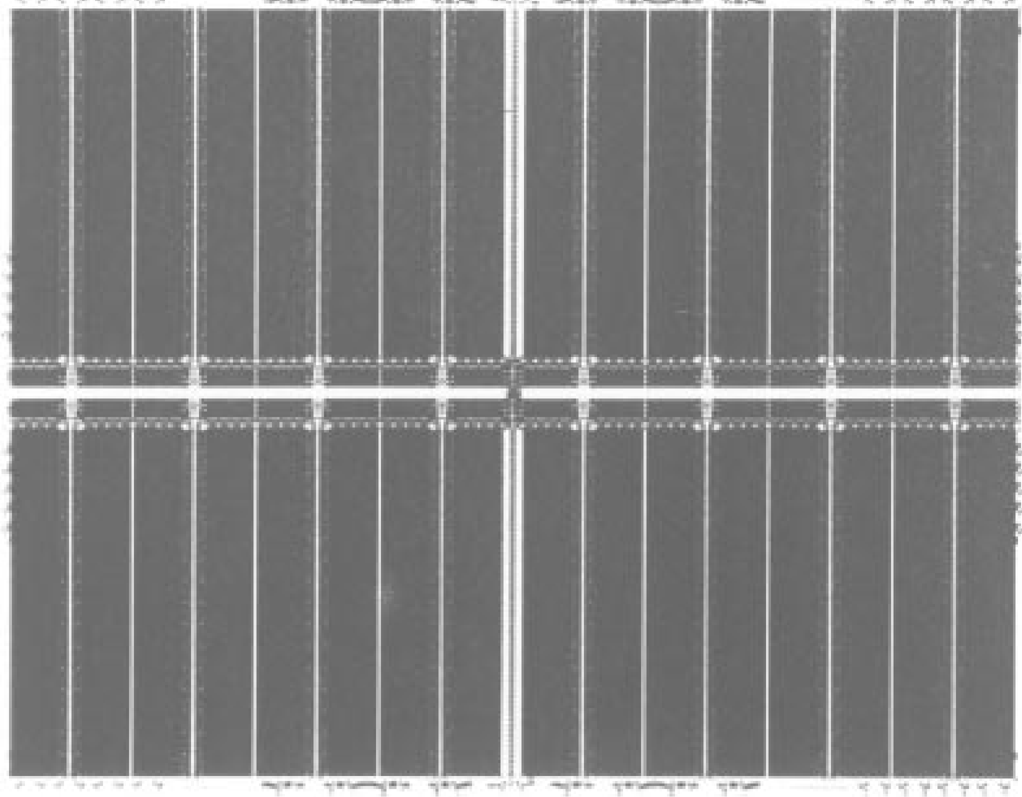

Fig. 12. Microphotograph of 1-V 1-Mb SRAM.

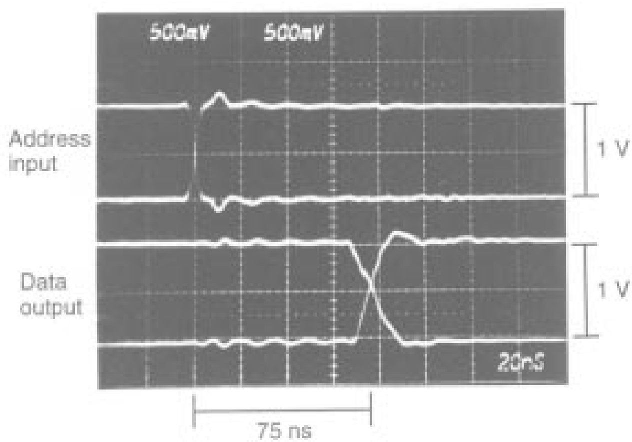

Fig. 13. Measured waveforms of 1-V 1-Mb SRAM.

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