Accurate Interconnect Modeling: Towards Multi-million Transistor Chips As Microwave Circuits

N.P. van der Meijs
Delft University of Technology
Mekelweg 4, 2628 CD Delft, the Netherlands
email: nick@cas.et.tudelft.nl

T. Smedes
Philips Semiconductors
Gerstweg 2, 6534 AE Nijmegen, the Netherlands
email: T.Smedes@nym.sc.philips.com

Abstract — In this tutorial we discuss concepts and techniques for the accurate and efficient modeling and extraction of interconnect parasitics in VLSI designs. Due to increasing operating frequencies, microwave-like effects will become important. Therefore stronger demands are put on extraction and verification tools. We indicate the state-of-the-art for capacitance, resistance and substrate resistance extraction and discuss some open problems. We also discuss several model reduction techniques as well as issues related to simulation and implementation in a CAD system.

1 Introduction

Future submicron integrated circuits will behave more and more like giant microwave circuits. The trend is towards reduced line widths together with larger die size, greater number of interconnect layers and GHz clock frequencies. As a consequence, the electrical characteristics of the interconnections are becoming important factors in the behavior of integrated circuits. Hence, they must be known with greater accuracy in order to avoid the necessity of using large safety margins leading to sub-optimal designs. Therefore, the traditional methods of parasitics extraction are no longer adequate. Much improved methods will be necessary to generate electrical models for the interconnections that accurately account for such effects as delay, crosstalk and resistive voltage drops.

These new methods must be accurate, efficient, flexible and robust. Other important issues include model reduction, in order to avoid overloading the subsequent analysis tools. The accuracy should be known and controllable, allowing a trade-off between accuracy and run-times. The amount of user intervention should be minimized, reducing the possibility for errors. Care must be taken to optimize the design-flow as a whole.

Much research is currently focusing on this subject, and several new extractors are entering the market. In this tutorial, we will review the current state-of-the-art and indicate some important open problems. Although we are dealing with problems in large layouts, for practical reasons we will illustrate the techniques with small examples. We will use capacitance extraction to illustrate some concepts that are relevant for other important extraction problems.

In the following sections we will first discuss techniques for extraction of interconnect capacitances, resistances and substrate resistances. Then we will address open extraction problems that we feel need to be solved in the near future. This is followed by a discussion of model reduction techniques and simulation issues. We end this tutorial with a more general discussion about the consequences for the implementation and application of extraction as described in the earlier sections.

2 Parasitics Extraction

2.1 Interconnect Capacitances

There are many techniques for computing the interconnect capacitances. Analytical techniques are usually not very useful because of the complexity of the interconnect geometries. The other methods can then be subdivided into geometrical and numerical methods.

Geometrical methods have evolved from simple parallel-plate calculations into elaborate geometric models to include more and more fringing effects [1]. Basically, such methods are fitting formulas, of which the coefficients are determined by numerical calculations or sometimes by measurements. All modern extractors (e.g. [2–4]) use such methods, and the fitting coefficients can be determined by automated procedures (e.g. [5]) from a file with layer thicknesses and permittivities. Because of their ability to model certain coupling capacitances, these methods are sometimes called quasi-3D methods.

Such methods are fast, and to a certain extend they can predict the capacitances fairly well. However, with the growth of the number of interconnect layers (2 poly and 5+ metal layers), these approaches become complex and inaccurate. At the very least, designers will want to check the results of those quasi-3D calculations against numerical calculations that start from ‘first principles’. Although it might not be feasible to do this for a full chip, some critical parts of the layout can be analyzed in more detail.

Common numerical techniques include the Finite-Difference Method (FDM) [6], the Finite-Element Method (FEM) [7] and the Boundary-Element Method (BEM) [8–10].

In both the FDM and the FEM, the external field is discretized. Because this field in principle extends to infinity, and can not be truncated easily, this leads to a very large matrix to be solved. Although the matrix is sparse, this re-

ICCAD ’96
1063-6757/96 $5.00 © 1996 IEEE

quires often exhaustive computational resources (time and memory). Special solvers [11] will only partially alleviate these problems. Alternatively, a technique called Geometry Independent Measured Equation of Invariance (GIMEI) [12] can be used to have a much smaller sparse matrix.

In the BEM, on the other hand, only the boundary of the field region is discretized. Hence, the 3D problem is effectively reduced to a 2D problem. The resulting matrix is therefore much smaller, but full. Boundary element methods are most effective when the medium is regular, or in the capacitance extraction case, when the chips have a stratified dielectric structure. To a certain extent, this is usually the case because of planarization.

The (full) BEM matrix **G** must be inverted and, without special techniques, this would result in a $\mathcal{O}(N^3)$ time complexity, where N is a measure of the size of the layout. However, two techniques have been presented to circumvent this problem. The first is the so-called multipole method [13]. To compute the matrix elements, an elementary solution of the partial differential solution (Green's function) has to be integrated over each possible pair of boundary elements. The multipole method hierarchically clusters boundary elements, in order to approximate the mutual influence between far away pairs. The clustering also helps with the matrix inversion and, as a result, the computational complexity is reduced to $\mathcal{O}(Nm)$, where m is the number of different conductors.

Both straight inversion and the multipole method result in a full matrix, which specifies a capacitance between every pair of conductors. When this is not what we want, for conductors that are far apart have a negligible capacitance, a second method even faster than the multipole method can be used. Using a Schur-type algorithm, a so-called *reduced* capacitance model can be produced. Given a parameter w denoting a distance beyond which coupling should be ignored, this algorithm produces an approximate sparse inverse $\mathbf{G}_{SI}^{-1}$ of **G**, that is positive definite and has the desired sparsity pattern.

The algorithm only uses entries from **G** in positions corresponding to the non-zero elements of $\mathbf{G}_{SI}^{-1}$. When $\mathbf{G}_{SI}^{-1}$ would be (exactly) inverted again, it would coincide with **G** on those positions. With a constant value of w, the total running time becomes linear ($\mathcal{O}(N)$) in the size of the layout. Also, the memory becomes $\mathcal{O}(\sqrt{N})$.

As an example, a 6-transistor 0.5 µ CMOS SRAM (Figure 1) has been extracted using the Schur algorithm. The results are shown in Table 1 together with those for an 5x5 SRAM array, indicating that the method is capable of full 3D extraction of fairly large designs using reasonable resources. The performance and number of capacitances extracted depend strongly on the parameter w. The time linearity is actually only shown for $w = 2$, because the edge effects of the small SRAM cause a time smaller than should be expected for the larger values of w. Finally, simulation results showing the effect of the parasitics are given in Table 2.

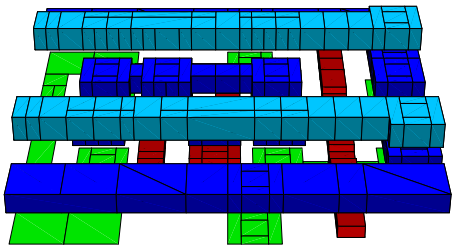

Figure 1: *BE Mesh for CMOS RAM cell.*

Table 1: *Cpu time ([h:m:s]), memory usage ([MB]) and number of capacitances as a function of window size for two different circuits.*

	SRAM (6 trans.)			SRAM 5x5 (150 trans.)		
w	time	mem.	# C	time	mem.	# C
2	27	4.2	24	14:06	6.9	608
4	1:57	23.0	27	1:55:40	36.1	970
6	2:28	38.5	28	7:33:50	151.0	1122

Table 2: *Spice results for CMOS SRAM cell* with *and* without *interconnect parasitics.*

quantity	without	C	RC
t_r (ns)	0.15	0.58	0.62
t_f (ns)	0.06	0.26	0.28
f_m (GHz)	4.0	1.0	0.8

2.2 Interconnect Resistances

Common VLSI interconnect resistances extraction approaches include the FEM [14,15] and the FDM [9]. These methods solve the resistance extraction problem by discretizing the governing differential equation (Laplace equation) and solving the resulting set of algebraic equations. This set of equations is sparse, symmetric and positive definite, and is usually solved by Gaussian elimination.

Compared to other methods for resistance extraction, such as Polygonal Decomposition [16], Conformal Transformation [17] and the BEM [18], the advantages of the FEM include general applicability, robustness, good accuracy and the possibility of accurately extracting RC models [15, 19]. Disadvantages, could be those of longer computation times and higher memory requirements.

However, it has been shown that the performance of FEM based resistance extraction can be greatly improved: Delayed Frontal Solution [20] implements a general technique for speeding up Gaussian Elimination (optimizing the elimination order) in a scanline-based extractor. Insertion of Articulation Nodes [21] employs the typical structure of VLSI wires (predominantly long and narrow) to ef-

fectively partition the problem in many smaller problems. The running times become much more linear with the problem size and will not depend strongly on the geometric structure and the discretization of the problem.

Table 2 shows the effect of interconnect resistances on the behavior of a CMOS RAM cell. Table 3 gives the results for extraction of all interconnect (excluding metal) and contact resistances for different circuits. This data clearly shows the linear time complexity. For comparison, the time and memory for the first (smallest) example without the algorithm improvements is already more than 30 minutes and 10 MB.

Table 3: *Resistance extraction data.*

circuit	#trans.	time [m:s]	memory [MB]
control	1,467	35.1	2.6
logic array 1	4,239	2:06.5	4.3
logic array 2	6,360	3:03.8	5.1
image proc.	32,313	15:56.4	22.2
cordic	63,416	33:58.5	30.1

2.3 Substrate Resistances

Apart from the interconnect above the silicon, true parasitic connections appear within the silicon. Due to the continuing decrease of the distances between components and the simultaneous increase of operating frequencies, the cross-talk between components and/or circuit blocks through the substrate becomes stronger.

Thus, an increasingly urgent topic for the realization of densely packed integrated circuits is prevention or at least control of cross-talk via the substrate. This problem is particularly important in high-frequency mixed-signal integrated circuits: potential spikes, generated by the fast switching logic, propagate through the substrate to sensitive analog nodes, causing distortion of the analog signals.

Currently, the most commonly used method to circumvent these problems is a very costly trial-and-error procedure, relying on experience and expertise of the designer. Methods to analyze these substrate problems and implementation of the methods in CAD tools are receiving a large attention.

Several results were published with a detailed numerical analysis of these problems. They use conventional device simulators for a full (usually Finite Element) numerical analysis of all potentials and currents in the substrate [22, 23]. However approaches like these are not efficient enough for implementation in an extractor. Furthermore, they do not provide a circuit model for the designer as a direct feedback between the circuit design, the layout design and the substrate problems.

Just as in the case of interconnect capacitances we see two approaches for the substrate resistance extraction: one basically geometrical approach [23, 24] and one starting from 'first principles' [25–27].

Often the geometrical methods are tuned on experiments done with general purpose BEM, FEM or on an extractor based on first principles. As with capacitances, the main advantages of geometrical methods is their speed and ease of user-definable modeling. However it is inherently more difficult to calculate process variations and such.

The more principal method usually are based on a numerical technique with several approaches to reduce the computational burden, both for the extractor and the simulator. The BEM is used in both [4,25], however with different approaches for reduction. Whereas [4] applies an actual *model* reduction, [25] proposes a preprocessed BEM with accelerated matrix solution. Section 3 will focus more on several model reduction techniques.

As an example of substrate resistance extraction, we discuss the techniques used in [4]. It uses a BEM on a stratified medium to extract the substrate resistances. The domain represents a layered IC, e.g. a homogeneously doped epi-layer on a homogeneously doped substrate. For such a substrate a Green's function has been derived [26]. More layers are possible at the cost of computation time.

The extractor recognizes those areas that interact with the substrate, such as substrate contacts, diffused resistors, bottoms of MOSFETs or a metal layer above the substrate. These areas are discretized and the BEM problem is solved on this grid. This has been combined with the Schur inversion for model reduction.

For faster (but less accurate) results, [4] also contains a heuristic geometrical method [24]. Here, using a Delauney mesh on the layout with the interacting areas, resistances between 'close areas' are calculated. Furthermore a resistance is calculated between each area and a common 'virtual reference' node. This way of modeling has been derived from BEM principles and comparison with results from the above method.

Measurement and simulation results on a test structure are shown in Figure 2. The structure consisted of 2 interdigitated metal structures above a substrate, shielded by a third metal line that was connected by vias to the epilayer. Extraction of parasitics was done with and without accounting for substrate cross-talk. Neglecting the substrate coupling clearly gives a completely wrong prediction of the behavior. Here the transadmittance is mainly capacitive, i.e. just the coupling capacitance from one metal line to the other. However, with substrate data based on Suprem simulations, the substrate resistance method of [4, 26] finds an excellent agreement with the measurements.

As another example we study the HF behavior of a small

bipolar amplifier. The circuit was extracted without substrate resistances and using both substrate resistance extraction methods. The simulation results are presented in Figure 3, showing that the substrate coupling effects as estimated using both methods are almost identical and have a clear influence on the magnitude of the transfer function.

On an HP 9000/735, extraction of the amplifier using the BEM took 184 seconds (248 elements were used). Extraction on the same computer, using the geometrical method, took less than 1 second (not including the determination of the parameters of the heuristic formulae).

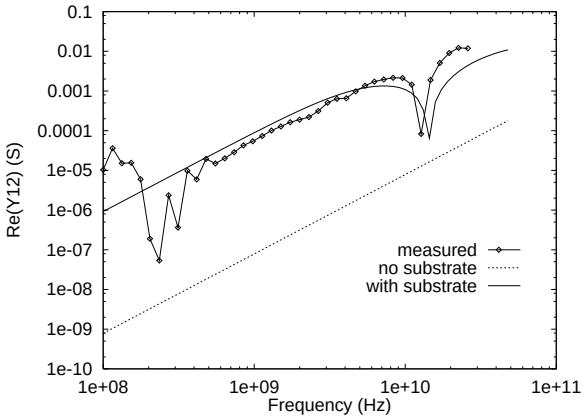

Figure 2: *Real part of transadmittance of test structure.*

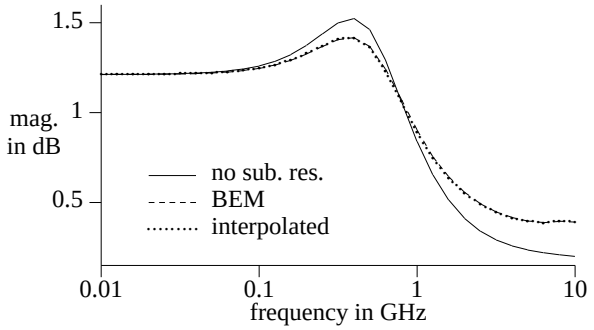

Figure 3: *Magnitude of transfer function of bipolar amplifier.*

2.4 Open Extraction Problems

The previous sections all discussed problems that are, to several degrees of sophistication, available in layout extractors. However, there are still several problems that have not yet been solved for implementation in such extractors. This section will briefly discuss the problems that we feel are the most urgent for the not too far future.

Inductive effects

Line inductance has been a problem in printed circuit board design for some time. This has not been the case in IC design, because of the much smaller dimensions of integrated circuits. However, the typical frequencies of on-chip signals are steadily increasing and the wavelengths are approaching the physical dimensions. Consequently, parasitic on-chip inductances also become important.

These inductances can cause various sorts of undesired electrical behavior, such as cross-coupling noise, signal reflections and switching noise. The result is often manifest on the system level, ranging from degraded performance to malfunctioning of the system. E.g. switching noise can be so severe that state-of-the-art digital circuits utilize tens or even hundreds of separate supply connections.

For the printed circuit board design there exist tools [28] for the analysis of inductive effects. However, until now these have not yet been adapted and applied for IC design.

To calculate lumped line inductances, the partial element equivalent circuit (PEEC) method [29] has been proposed. It is yet unclear how such a method can be made part of a layout to circuit extractor to produce an electrical model of a chip containing the active devices (with detailed specification of their parameters) and a lumped network with the parasitic capacitances, resistances and inductances. In particular, the method must be suited to compute, fully automatically, all important inductances present in the giant digital chips that will be designed in the coming years.

While lumped inductance models are often adequate, especially for the modeling of switching noise, they can be cumbersome in other situations. For example, many lumped sections are needed to accurately model signal delay in long lines. Moreover, when such a model is generated using 3D inductance and capacitance calculation methods, all sections are capacitively and inductively coupled to all other sections.

Lumped models that more accurately reflect the effects of the finite speed of light are the *retarded* PEEC models [30], but these models are also very complex. More compact models, suited for uniform 2D structures supporting TEM or quasi-TEM wave propagations, consider the interconnections as non-ideal coupled transmission lines.

Non-stratified Dielectrics

In most of the methods for interconnect extraction discussed before it was assumed that the dielectrics are stratified. However this assumption is not always valid. In the situation of crossing interconnect lines significant irregularities in the dielectric thickness may appear. In [31] a method is described which is capable of taking into account this phenomenon, by combination of the BEM and the FEM. Here, the FEM is used for the irregularity, while the BEM is used for the stratified parts of the interconnect. This is illustrated in Figure 4.

Even with modern planarization techniques still the interconnect may not be stratified. These modern techniques may give *locally* planar dielectrics, but usually not *globally* planar dielectrics. Note that the technique of [31] is not ef-

ficient in this case, since it would require a large part of the layout to be treated with the FEM. Currently no efficient technique for implementation in an extractor is known.

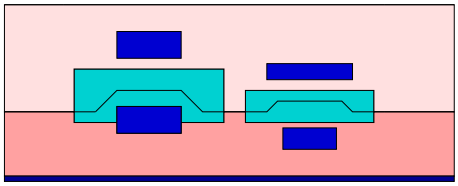

Figure 4: *An example of an IC structure with non-planarized parts, indicating the FEM and BEM areas.*

Coupled Problems

In the previous all effects are treated independently. However, in principle, there is only one electromagnetic problem in an inhomogeneous domain [28, 32]. Already when thinking about transmission lines, we are dealing with coupled differential equations. However the situation may become much more complex, especially when there is interaction between the fields in the dielectric and the fields in the substrate. E.g., the electric fields caused by the interconnect only penetrate the surface of the substrate, whereas the magnetic field fully penetrates the substrate. This leads to slow-wave effects. Presently, there are no VLSI layout extractors capable of handling such situations.

Thus there are several open problems. These are even augmented by the fact that solutions for these in many cases must be consistent and compatible with each other and existing techniques. This has a major impact on the modeling, reduction and implementation issues.

3 Model Reduction

For extraction of parasitics, usually a fine model is created as a first step. This fine model is an accurate representation of the physical structure with a large number of sections to ensure that the distributed properties of interconnect line are maintained. However, this large number of sections makes an efficient circuit simulation or timing analysis afterwards virtually impossible. Therefore a model is sought that has a much lower complexity, but still displays approximately the same transmission behavior.

Several methods for model reduction can be found in the already mentioned extractors. We can distinguish between reduction *before*, *during* and *after* the actual extraction. We will briefly indicate some pro's and con's of reduction methods often encountered.

The multipole method, discussed in Section 2.1, is an example of reduction *before* extraction. The Schur method is a reduction technique *during* the extraction and has also been explained before in Section 2.1. The main advantages are that it is a linear process and yields a reduced netlist. Its disadvantage is that there is not a clear relation between the final accuracy and the size of the reduction.

A popular reduction method *after* RC extraction, that however only yields an adequate low-frequency model, has been presented in [15,19]. This method yields a simple full-graph resistance network between the terminals and distributes the capacitances over those terminals. All internal nodes are eliminated. The resulting network is constructed such that the Elmore delay times are preserved. The disadvantage is that at HF this may not be sufficient.

Congruence transformations [27] have been proposed as an alternative technique to reduce RC networks. This method exploits the RC character of the network and is therefore, like the other methods above, unsuitable for situations with inductive effects. This has been solved by the following techniques.

AWE [33] reduces the large set of system poles to a limited set of approximated poles. Hence, the circuit is simplified, while its behavior essentially is retained. However AWE has two important draw-backs. First, poles are obtained, not a circuit model. This requires a special circuit simulator, even when using special macro-models. Second, AWE cannot guarantee numerical stability, which may lead to un-physical oscillations during simulation.

An extension of the Elmore delay preserving reduction method has been described in [34]. It is capable of dealing with inductive networks. The accuracy is user-controllable, by specifying a maximum operating frequency f_s. The behavior of the reduced network matches that of the original until f_s. With low f_s, the method becomes equivalent to the methods of [15,19]. Otherwise, some internal nodes are retained and the final interconnection topology more resembles the original.

The method *selectively* removes non-terminal nodes: only nodes that are non-essential for the behavior until f_s are eliminated. To decide which nodes are essential in a given configuration, the method calculates for each non-terminal node an estimation of the relative error made if that node should be eliminated. Nodes of which that error does not exceed a predefined tolerance actually are eliminated. By continuously recalculating the errors of the remaining nodes, the method accounts for the increase of the relative importance of those nodes, when a node is eliminated.

Figure 5 shows results from the latter method for a long serpentine resistor in series with a large plate capacitance. Due to the coupling capacitances in the serpentine this is not simply a single pole RC network. The effect of increasing f_s is clear.

4 Consequences for Simulation

It is clear from the previous sections that already at present, and even more so in the future, taking into account electrical effects in the interconnect in the circuit analysis

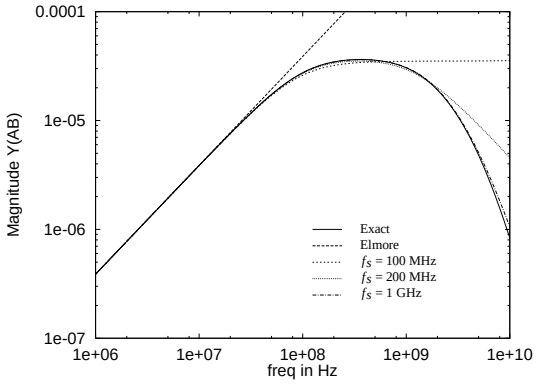

Figure 5: *Magnitude of the transadmittance of the RC structure for several maximum frequencies.*

puts a heavy burden on the circuit simulators to be used. In general the systems to be analyzed will only increase in size, probably non-linear effects will increase and devices will influence each other more and more.

All these effects make the task of circuit simulation more and more difficult. In addition to these, there is the trend to do more robust design, i.e. already in the design and verification stages the effects of possible 'random' process variations are taken into account. Current practice has been for a long time to do a 'slow-nominal-fast' analysis, however there is a trend to more statistically based methods [35,36]. In practice this means that instead of 1 or 3 circuit evaluations, now 10's (quasi MC) or 100's (full MC) evaluations have to be performed in a similar time frame.

Furthermore 'new' analysis types come into play, e.g. power distribution analysis, reliability simulations, etc. It is not the goal of this tutorial to discuss circuit simulation techniques, but we would like to point out that techniques proposed and successfully applied in the past may loose part of their effect in the future. For example, the fact that parts of the circuit will become more coupled to each other electrically, in general reduces the effectivity of Waveform Relaxation techniques in circuit simulators.

An important point to consider is the place where the actual mapping of the extraction results to electrical elements that the core of the simulator understands is done. There are two philosophies: the extractor produces *geometrical* models with their parameters or the extractor produces *electrical* models with their parameters.

In the first case the simulator must have built-in models for all devices (including the parasitics) or it must allow the use of user-programmed models calculating the electrical parameters of the built-in models from the geometrical data and the process data or unity parameters.

An example of this approach is the combination of [37] and [38]. The interfacing is done by so called process blocks. A process block gives the relation between geometrical parameters, process parameters and electrical parameters. It also enables realistic sensitivity analysis, statistical simulations and mismatch analysis by keeping track of correlations between the parameters [35].

An example of the second philosophy is [4]. This extractor directly produces a netlist with built-in electrical elements for several simulators. The advantage is that model reduction based on electrical quantities can be done by the extractor, thus saving on communication between extractor and simulator. The disadvantage is reduced flexibility for statistical analysis and user defined modeling.

However, with the trends as in the previous sections towards more complex models it is questionable whether the 'extractor only supplies geometrical data' philosophy can be kept for interconnect extraction. We have seen 3D extractors with the BEM or FEM. At present there is no general method to directly derive electrical models from 3D geometrical data.

Another important issue is the required 'level' of simulation. The above is mainly described from the viewpoint of analog circuit simulation for maximum accuracy in the prediction of signal behavior. However, for large digital circuits this is not feasible.

Therefore in these cases usually gate-level or switch-level simulators are used. In particular in the first, the focus is on logic functionality and timing analysis. Timing analysis is made possible by characterizing the timing behavior of the logic gates (including their internal parasitics) with an analog simulator and using the results to derive a delay model for the gates. This can be done, since there usually is a library with logic gates that are predefined and reused. However, delays caused by the interconnect between gates can only be taken into account by extraction of the actual layout. Therefore those simulators must be able to handle the electrical models for the parasitics. For many situations this requires a modification of the logic gate models or the switch-level device models. E.g. switch-level MOSFET models usually do not have a back gate contact. For substrate coupling it is necessary that the back gate is taken into account.

As said before, large IC's with all the interconnect circuitry will behave like complete microwave circuits. Thus it is appropriate to investigate microwave simulators [39]. Although these are continuously improving and incorporate ever more device models, they suffer from the same limitation as analogue circuit simulators. They perform well for relatively small circuits, but cannot handle the large VLSI circuits. Typically, microwave circuits contained in the order of 10's of active components. There is a clear trend that this number increases, however with the upcoming microwave effects in VLSI IC's. Hence there is a great challenge to increase the capabilities of these simulators.

5 Future CAD Systems

The ideal tool will be a combination of most of the methods discussed in the previous sections. In order to be able to handle large layouts the extracted netlist will have to be as simple as possible (but not more simple than that) and the simulation will be done at a high abstract level.

However, based on e.g sensitivity analysis or critical path analysis, some parts of the layout will need higher extraction accuracy or higher simulation accuracy. This will then be done on the affected parts of the layout or netlists. The results will be 'merged' with previous results.

For example, if for two blocks it is found that substrate coupling is of great importance for the timing analysis, a BE method might be applied locally, to yield an accurate substrate network. It may now be necessary to simulate this part on an analogue level and the results translated to a more accurate timing description for those blocks in their context for the higher level simulator.

Likewise it is quite possible that a crossing bus situation is sensitive for coupling capacitances and the presence of a substrate. The busses will be extracted using an advanced 3D method (including inductive and slow wave effects) and the results will be resimulated with a microwave solver.

The selection of critical parasitics must not be done by the designer: it will be too risky for him to miss critical ones. As a result, he will probably tend to overestimate their influence and select too many of them. Both situations are wrong: the first can clearly be disastrous and the second can lead to excessive computation times. Moreover, no matter how careful or skilled the designer is, there can be no guarantee that all relevant parasitics have been determined. Thus, the parasitics screening must be automated.

As will be clear from those examples this approach will need a lot of data manipulation to translate results from lower to higher hierarchical levels and vice versa. It is obvious that even for parts of this tool still much research is required. There is still a long way to go until the combination will be available in a useful tool.

It must not be underestimated how important the 'look and feel' of the tools discussed above is. Since the functional complexity is growing, user interfaces need to be concise and easy to use. Localized parts of the design tool will represent the expert knowledge, like that of a microwave engineer, device physicist or analogue designer. Yet the tool itself must be such that it can be used efficiently by an IC designer or more and more a 'system engineer'. Therefore these tools must be an integrated part of a well-established design flow. This requires careful planning of interactions between programs. Thus standardization [40] is of paramount importance if it is desired to be able to use tools of different makes.

Another issue is that of correct verification of so-called clean and dirty hierarchies. Dirty hierarchies are those where the function of one cell is modified by the layout of another cell, at the same or another hierarchical level, whereas clean hierarchies don't exhibit interactions between cells other than via their terminals. However, parasitics become so important that no hierarchy can be treated as clean anymore. The answer usually is flat extraction, but this is obviously at the cost of computation time. Hierarchical extraction that correctly accounts for inter-cell parasitics will be needed.

Acknowledgements

This research is supported in part by the Dutch Technology Foundation (STW) under grants DEL 11.2450 and DEL 22.2810, and has been carried out in the context of DIMES, the Delft Institute of Microelectronics and Submicron Technology. We thank our colleagues at Delft University and Philips Nijmegen for their valuable work, on which this tutorial is partly based.

References

[1] N.D. Arora, K.V. Raol, R. Schumann, and L.M. Richardson, "Modeling and Extraction of Interconnect Capacitances for Multilayer VLSI Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 15, no. 1, pp. 58–67, 1996.

[2] Avant! Star, information can be found at website http://www.avanticorp.com/pdf/star.pdf.

[3] Epic Arcadia, information can be found at website http://www.epic.com/arcadia.html.

[4] Space/OptEM Inspector, information can be found at website http://cas.et.tudelft.nl/research/space.html.

[5] TMA Raphael, information can be found at website http://www.tmai.com/PRODUCT/raphael.html.

[6] R. Guerrieri and A. L. Sangiovanni-Vincentelli, "Three-Dimensional Capacitance Evaluation on a Connection Machine," *IEEE Trans. on Computer-Aided Design*, vol. 7, pp. 1125–1133, Nov. 1988.

[7] P. E. Cottrell and E. M. Buturla, "VLSI Wiring Capacitance," *IBM J. Res. Develop.*, vol. 29, pp. 277–288, May 1985.

[8] A. E. Ruehli, "Survey of computer-aided electrical analysis of integrated circuit interconnections," *IBM J. Res. Develop.*, vol. 23, pp. 626–639, Nov. 1979.

[9] S. P. McCormick, "EXCL: A circuit extractor for IC designs," in *Proc. 21st Design Automation Conference*, pp. 616–623, 1984.

[10] Z. Q. Ning, P. M. Dewilde, and F. L. Neerhoff, "Capacitance Coefficients for VLSI Multilevel Metallization Lines," *IEEE Trans. on Electron Devices*, vol. ED-34, pp. 644–649, Mar. 1987.

[11] O. E. Akcasu, J. Lu, A. Dalal, S. Mitra, L. Lev, N. Vasseghi, A. Pance, H. Hingarh, and H. Basit, "'NET-AN' a Full Three-Dimensional Parasitic Interconnect Distributed RLC Extractor for Large Full Chip Applications," in *Proc. IEDM '95*, pp. 495–498, 1995.

[12] W. Sun, W. Wei-Ming Dai, and W. Hong, "Fast Parameters Extraction of General Three-Dimension Interconnects Using Geometry Independent Measured Equation of Invariance," in *Proc. 33rd Design Automation Conference*, pp. 371–376, 1996.

[13] K. Nabors and J. White, "FastCap: A Multipole Accelerated 3-D Capacitance Extraction Program," *IEEE Trans. on CAD*, vol. CAD-10, pp. 1447–1459, Nov. 1991.

[14] T. Mitsuhashi and K. Yoshida, "A Resistance Calculation Algorithm and its Application to Circuit Extraction," *IEEE Trans. CAD*, vol. CAD-6, no. 3, pp. 337–345, 1987.

[15] A. J. van Genderen and N. P. van der Meijs, "Reduced RC Models for IC Interconnections with Coupling Capacitances," in *Proc. IEEE 3rd European Design Automation Conference*, (Brussels, Belgium), pp. 132–136, Mar. 1992.

[16] M. Horowitz and R. W. Dutton, "Resistance extraction from mask layout data," *IEEE Trans. on CAD*, vol. CAD-2, pp. 145–150, July 1983.

[17] P. M. Hall, "Resistance Calculation for Thin Film Patterns," *Thin Solid Films*, vol. 1, pp. 277–295, 1967/1968.

[18] B. R. Chawla and H. K. Gummel, "A Boundary Technique for Calculation of Distributed Resistance," *IEEE Trans. Electron Devices*, vol. ED-17, pp. 915–25, 1970.

[19] M. G. Harbour and J. M. Drake, "Calculation of Signal Delay in Integrated Interconnections," *IEEE Trans. on Circuits and Systems*, vol. CAS-36, pp. 272–276, Feb. 1989.

[20] N. P. van der Meijs and A. J. van Genderen, "Delayed Frontal Solution for Finite-Element based Resistance Extraction," in *Proceedings of the 32nd Design Automation Conference*, (San Francisco, USA), pp. 273–278, June 1995.

[21] A. J. van Genderen and N. P. van der Meijs, "Using Articulation Nodes to Improve the Efficiency of Finite-Element based Resistance Extraction," in *Proceedings of the 33rd Design Automation Conference*, (Las Vegas, USA), pp. 758–763, June 1996.

[22] M.J. Loinaz D.K. Su, S. Masui, and B.A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, vol. SSC-28, no. 4, pp. 420–430, 1993.

[23] K. Joardar, "Substrate Crosstalk in BiCMOS Mixed Mode Integrated Circuits," *Solid-State Electronics*, vol. 39, no. 4, pp. 511–516, 1996.

[24] A. J. van Genderen, N. P. van der Meijs, and T. Smedes, "Fast Computation of Substrate Resistances in Large Circuits," in *Proc. EDTC Conference*, (Paris, France), pp. 560–565, Mar. 1996.

[25] N.K. Verghese, *Extraction and Simulation Techniques for Substrate-Coupled Noise in Mixed-Signal Integrated Circuits*. PhD thesis, Carnegie Mellon University, Pittsburgh, USA, 1995.

[26] T. Smedes, N. P. van der Meijs, and A. J. van Genderen, "Extraction of Circuit Models for Substrate Cross-talk," in *Proc. of the ICCAD*, (San Jose, CA, USA), pp. 199–206, Nov. 1995.

[27] K.J. Kerns, I.L. Wemple, and A.T. Yang, "Efficient Parasitic Substrate Modeling for Monolithic Mixed-A/D Circuit Design and Verification," *Analog Integrated Circuits and Signal Processing*, vol. 10, pp. 7–21, 1996.

[28] Several authors, "Special Issue on Electromagnetic Compatibility," *Philips Journal of Research*, vol. 48, no. 1–2, pp. 1–144, 1994.

[29] A.E. Ruehli, "Inductance Calculations in a Complex Integrated Circuit Environment," *IBM Journal of Research and Development*, vol. 16, pp. 470–481, Sep. 1972.

[30] H. Heeb and A.E. Ruehli, "Retarded Models for PC board Interconnects — or how the Speed of Light affects your SPICE Circuit Simulation," in *Proc. IEEE Int. Conf. Computer Aided Design*, pp. 70–73, Nov. 1991.

[31] P.M. Dewilde and E.B. Nowacka, "Circuit Models for the Hybrid Element Method," in *Proc. ISCAS '96*, (Atlanta), pp. IV 616–619, May 1996.

[32] A.K. Goel, *High-Speed VLSI Interconnections*. John Wiley & Sons, New York, 1994.

[33] L. Pileggi, "Coping with RC(L) Interconnect Design Headaches," in *Proc. IEEE ICCAD-95*, (Santa Clara), pp. 246–253, nov 1995.

[34] P. J. H. Elias and N. P. van der Meijs, "Extracting Circuit Models for Large RC Interconnections that are Accurate up to a Predefined Signal Frequency," in *Proceedings of the 33rd Design Automation Conference*, (Las Vegas, USA), pp. 764–769, June 1996.

[35] P.J. Rankin, "Statistical Modelling for Integrated Circuits," *IEE Proceedings Part G*, vol. 129, no. 4, pp. 186–191, 1982.

[36] S.G. Duvall, "A Practical Methodology for the Statistical Design of Complex Logic Products for Performance," *IEEE Trans. on VLSI Systems*, vol. 3, no. 1, pp. 112–123, 1995.

[37] L.Th.G Simons and H. van der Gaag, "Principles of LOCAL45," tech. rep., Philips Research Laboratories, Eindhoven, the Netherlands, 1983.

[38] PSTAR, Philips proprietary circuit simulator.

[39] Cadence Analog Artist Microwave Design System, information can be found at website http://www.cadence.com/software/qx-micr.html.

[40] S. Grout, A. Dengi, S. Dasgupta, and D. Nushroe, "Integrated Hierarchical Forward Timing Driven Electrical and Physical Design Requirements for 0.25-micron Chip Design," tech. rep., Sematech, Inc, 1996.