Design Methodology for Analog High Frequency ICs

Yasunori Miyahara, Yoshitomo Oumi and Seijiro Moriyama*

Multi Media Engineering Lab., TOSHIBA Corp.
8,Shinsugita-cho, Isogo-ku, Yokohama, 235, JAPAN
miyahara@cpl.toshiba.co.jp oumi@cpl.toshiba.co.jp

* Semiconductor Group (3L-GI), TOSHIBA Corp.
580-1, Horikawa-cho, Saiwai-ku, Kawasaki,210, JAPAN
s.moriyama@ieee.org

Abstract

This paper presents a methodology suited for high frequency analog IC design. The use of a top-down method with AHDL for circuit designers is proposed. In order to accelerate the re-use of circuits that were previously designed and validated in other ICs, the authors developed a system that eases the re-use in the top-down design environment. Moreover, a model parameter generation technique for bipolar transistors has been developed and its usefulness has been shown for accurate simulation of high frequency analog ICs.

1. Introduction

The authors are developing high frequency analog signal processing ICs for consumer electronic products like TV tuners, satellite broadcasting receivers and multimedia wireless equipment.

In most of these systems, either input or output signals (or both) are transmitted by analog high frequency signals. Input analog signals are processed by analog processing circuitry, and then converted to digital signals. After digital signal processing, the resulting signals are converted back to analog for output.

The development of digital ICs is highly automated: circuit schematics and IC layouts can be synthesized from the system level design which is described in a high level hardware design language.

Unfortunately, the same thing does not happen to most analog designs. In the development of analog ICs, there is no analog synthesis system available and IC layouts can hardly be automatically generated from system descriptions.

To reduce the development time of system ICs, the authors believe that analog top-down design and exact simulation are essentially important. In section 2, top-down design method for analog ICs is proposed with an application to an actual design example of a conventional double-super tuner system. The top-down method will be supplemented by the re-use of previously-designed circuits in section 3. Finally, a bipolar transistor model parameter generation technique for the design of analog high frequency circuits will be introduced in section 4.

2. Top-down design for analog IC's

An AHDL is a description language for behavior level design, and can be used to describe analog operation in detail. Recently, AHDL products have appeared from several CAD venders. As digital IC systems are described by digital HDL (VHDL or Verilog), all analog IC systems can be described by using AHDL.

In digital IC design, HDL is very effective; behavior description can be automatically translated to logic description and then to IC layout using various synthesis tools.

But in analog IC design, there is no design compiler for AHDL. So, what are the merits of using AHDL, and how can AHDL be used by IC circuit designers to develop analog ICs in a short term? The authors propose the use of AHDL in top-down analog IC design flow.

2.1 What is a top-down design?

Advances in IC process technology have made system on chip possible. Because many functions are integrated on a chip, typical analog system ICs have more than 10,000 elements on a chip. In designing such ICs, if circuit blocks are expressed by primitive elements like transistors, it is very difficult to understand the functions of the IC.

Figure 1 shows the top-down design method in an analog IC design flow. In the top-down design method, each function block is described by AHDL at the

33rd Design Automation Conference ®

DAC 96 - 06/96 Las Vegas, NV, USA

behavioral level. So, the whole IC operation can be simulated within a reasonable CPU time. From the simulation results, IC designers can judge or confirm whether the requested specification in each function block is correct or not.

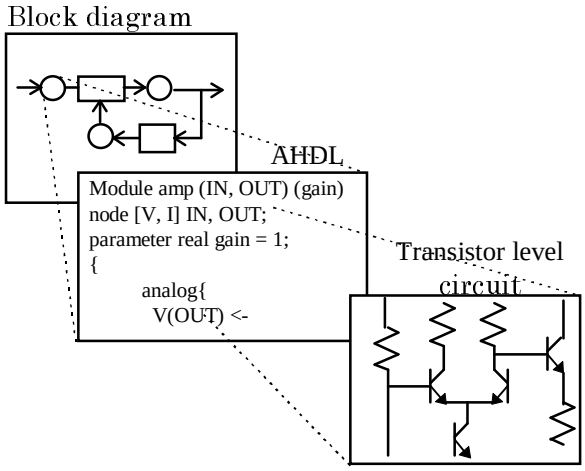

Fig.1 Top-down design method

In the case of ordinary analog ICs, the specification for the whole IC is determined by system designers. Usually, the determination of the specification for each function in the IC is left to the IC circuit designers.

Up until now, analog IC designers have depended on their intuition and experience to determine the specifications for function blocks in the ICs. Their design knowledge has been accumulated by individuals as analog IC design know-how. This is one of the reasons why analog IC design efficiency is very bad. When each block design is complete at the primitive element level and the whole circuit does not work, it often happens that each block has to be re-designed from the beginning.

Thus, the authors propose the top-down design method using AHDL. At the beginning, circuit designers describe the functions of individual blocks using the AHDL, then analyze the whole system. Through the process, they can generate detailed specifications for individual blocks. After determining the specifications of every block in the IC, each block is designed at the primitive element level.

In the top-down design method, it is easy to examine the difference between an ideal circuit and a real circuit. By replacing an AHDL block with a transistor level one, circuit designers can easily find the effects of primitive elements to the whole system.

By using the top-down method, the development efficiency of ICs can be significantly improved.

2.2 Example of top-down design

A tuner system used for CATV receivers is a typical analog system. A double-super type tuner is often used for the set-top box of CATV systems. In such CATV tuner systems, distortion, noise and image signal are main concerns in circuit design.

An actual example of a top-down design applied to a conventional double-super tuner system is shown in Fig. 2.

Figure 3 is the frequency spectrum of the system which explains the image signal.

In a conventional double-super tuner, an input RF signal which includes tuned RF signal (RF1) and an image signal (RF2) are up-converted to the 1st IF frequency of rf1 and rf2 by a local signal of frequency Fup. Moreover, the 1st IF frequency of rf1 and rf2 is down-converted to the 2nd IF signal (fIF) by a local signal of frequency Fdown.

If the relation between the 1st IF signals rf1 and rf2 is rf2-Fdown=Fdown-rf1, then rf1 and rf2 are converted to the same signal of the 2nd IF (fIF).

This is why an RF signal like RF2 is called an image signal. In the CATV system, the frequency of rf2-Fdown is 45 MHz, which makes the rejection of image signals in the 1st IF of the tuner very difficult because it requires a vary narrow band pass filter. So, in order to remove this image signal for CATV, an image rejection mixer for the double-super tuner system is introduced as shown in Fig. 4.

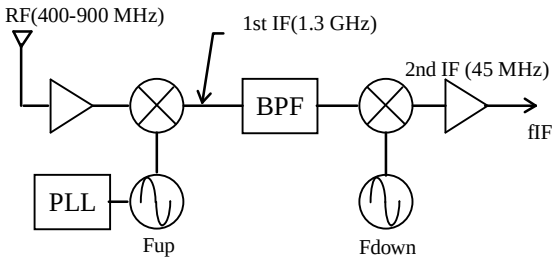

Fig 2. Block diagram of double-super tuner

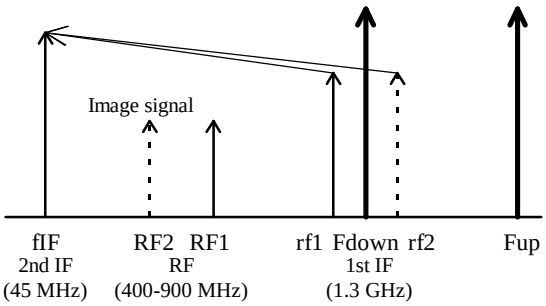

Fig. 3 Frequency spectrum of double-super tuner

In this tuner system, after an input RF signal is up-converted and filtered, the 1st IF signal is divided to two signal paths. These 1st IF signals are down-converted to 2nd IF signals using the 2nd local oscillator (VCO) which has two outputs whose phases are different by 90 degrees. Then, one of the 2nd IF signal phase is shifted by 90 degrees and added to the other 2nd IF signal. Because the image signal's phase turn reverse to cancel themselves, only tuned signals are output to the 2nd IF by this system.

Now, IC circuit designers have to examine the performance of this system taking IC process variations into account. It takes a very long time to analyze the circuit at the transistor level, because the circuit has over several thousands elements. Practically, it can only be simulated by using AHDL.

The performance deterioration of this image rejection system is determined by the phase balance and the gain balance of 90 degree phase shifters in the VCO and 2nd IF signal path. The effects of the gain balance and the phase balance in the image rejection system can be simulated by AHDL [1]. The result is show in Fig. 5, where the image rejection ratio is plotted against the phase error, changing the gain balance as a parameter. From this figure, we can understand how the phase balance and the gain balance influence the image rejection.

Assume that a system designer requests an image rejection ratio of 30 dB. Then, by using Fig. 5, an IC circuit designer can determine an optimum set of specifications for the combination of the gain balance and the phase balance for the 90 degree phase shifters.

In this way, by using AHDL, IC circuit designers are able to determine the block specifications in more detail from the system level specification. The top-down design method enables IC circuit designers to determine the specification of IC blocks easier and more precise, and thus eliminates the need to re-design the circuits many times.

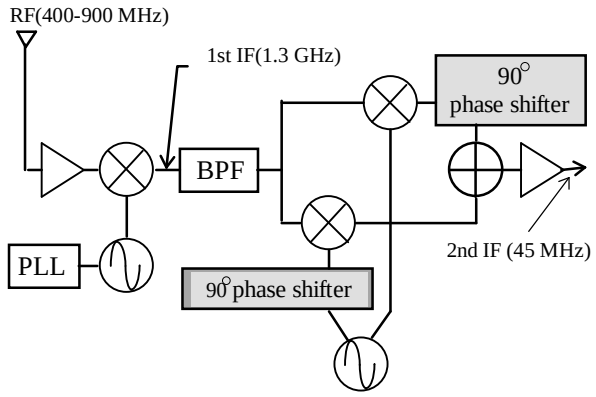

Fig 4. Block diagram of double-super tuner with image rejection mixer

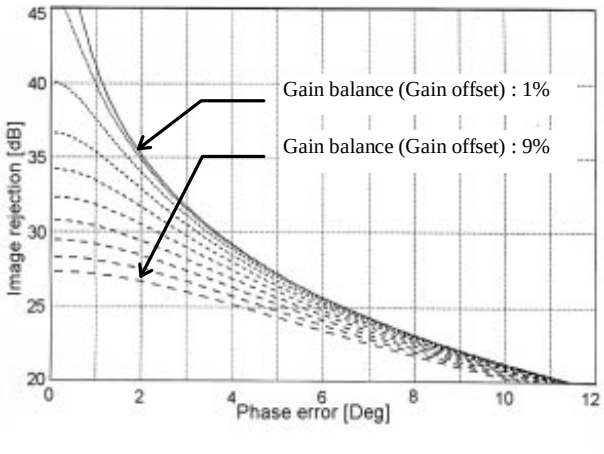

Fig. 5 AHDL simulation result of image rejection tuner

3. Re-use of circuits for efficient IC development

Not all circuits are newly designed in most analog IC systems, even if the requirement to the circuit specification is different from the old system. Only some portions of the circuits are changed. Investigating the re-use of IC design in the authors' design group revealed that above 70% of the circuits can be re-used.

In spite of the usefulness of AHDL, conventional circuit designers, who are specialists in analog circuit design, cannot always use AHDL easily, because they do not usually have good programming skill. A database of previously-designed circuits allows them to re-use circuits easily.

The authors have developed an Analog Cell-based Design Supporting System, where the circuit data for re-use are composed of documents that describe the individual operations of circuits, the descriptions of the individual behavior of circuits, the primitive element implementations of circuits, and block symbols needed for the top-down design method. This system has been built on the top of Analog Artist from CADENCE.

This system is composed of two parts. One part is for the circuit designer who registers circuits. The other part is for those who search registered circuits and copy them from the database for re-use. As shown in Fig. 6, this database system is classified according to the application field, and the category to which the circuit belongs. Figure 7 shows an example of an analog cell data.

The IC development period is expected to be substantially reduced by adopting the top-down method with the analog cell-based design supporting system.

The authors also offer a library of circuits by a WWW server in TOSHIBA. This WWW based system is different from the cell-based design supporting system; the system can be used to make a quick inspection of circuit diagrams and documents on circuit operation which are classified in many categories.

The properties of circuits designed in the past can be fully utilized when circuit designers use both systems.

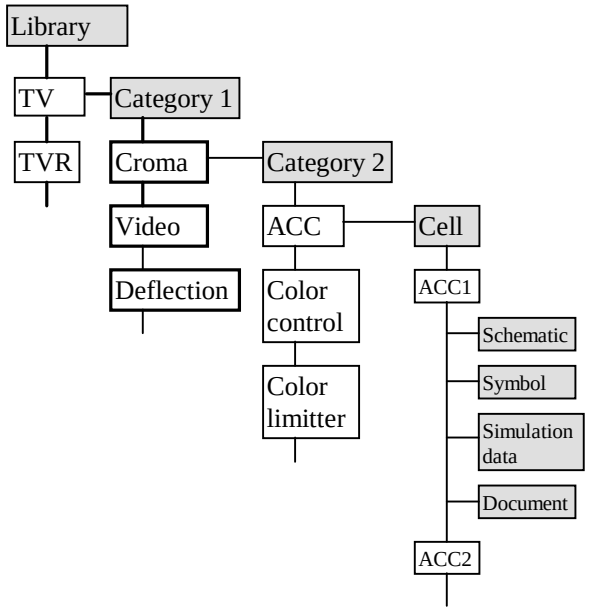

Fig. 6 Structure of an analog cell database

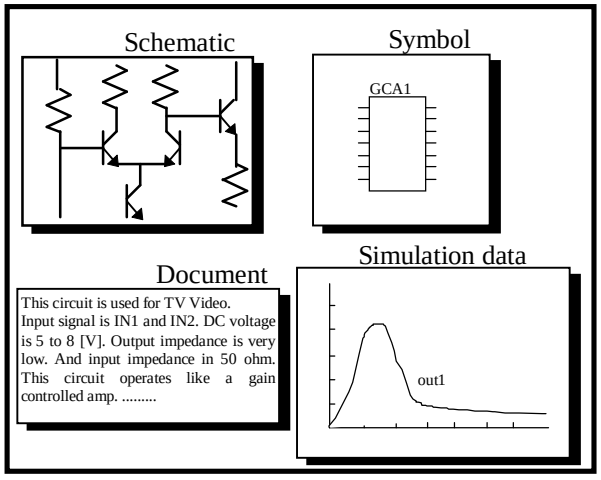

Fig.7 An example of an analog cell data

4. An improved bipolar transistor model parameter generation technique

Finally, a bipolar transistor model parameter generation technique is introduced which is used for the design of analog high frequency circuits.

Generally, transistors used in ICs are not of a single shape. It is desirable that transistors of various shapes can be used in high frequency ICs. For bipolar devices, the emitter shape (length, width, number of strips) and the base shape (length, stripes) need to be freely selected for optimum design. An example of transistor shapes are shown in Fig. 8.

The transistor shape is selected by considering the priority of the parasitic elements' parameters in terms of the required circuit performance. In high frequency circuits whose operating frequency is very close to the transition frequency (f_T), the transistor's shape affects the circuit performance significantly.

The Ic-f_T characteristics of various shape transistors are shown in Fig. 9. As shown in this figure, the collector current which gives the peak f_T changes depending on the shapes of the transistors. This means that if the collector current is not used at f_T peak frequency, characteristics of a circuit will get worse.

There is another factor which determines the transistors' shapes. In most of analog ICs, the current needed for a circuit has been decided considering the radiation from the IC packages. Once the circuit topology and operating current are determined, the transistor shape will then be selected according to that current. So, in high frequency circuits, the shapes of the transistors must be chosen to optimize the circuit performance.

The problem here is that, usually, only limited sets of transistor model parameters are provided for various transistor shapes. In SPICE simulation, this problem is partially solved by using the emitter ‘area factor’ instead of generating model parameters for various transistor shapes. Model parameters such as RB, RE, RC, CJE, CJC and CJS, which depend not only on the emitter area but also on their perimeter and their specific device geometry, are just scaled according to the area factor in SPICE [2] [3]. It is obvious that the computing method in SPICE is not sufficiently accurate for modeling important shape dependent parameters.

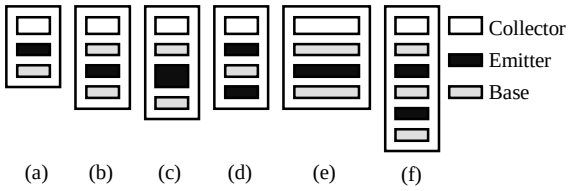

Fig. 8 Various transistor shapes in ICs

(a) N1.2-6S: Single emitter, single base (emitter length 6um emitter width 1.2um).
(b) N1.2-6D: Single emitter, double base (same emitter size as (a)).
(c) N2.4-6D: Single emitter, double base (emitter length 6um emitter width 2.4um).
(d) N1.2-6-2S: Double emitter, single base (same emitter size as (a)).
(e) N1.2-12D: Single emitter, double base (emitter length 12um emitter width 1.2um).
(f) N1.2-6-2D: Double emitter, triple base (same emitter size as (a)).

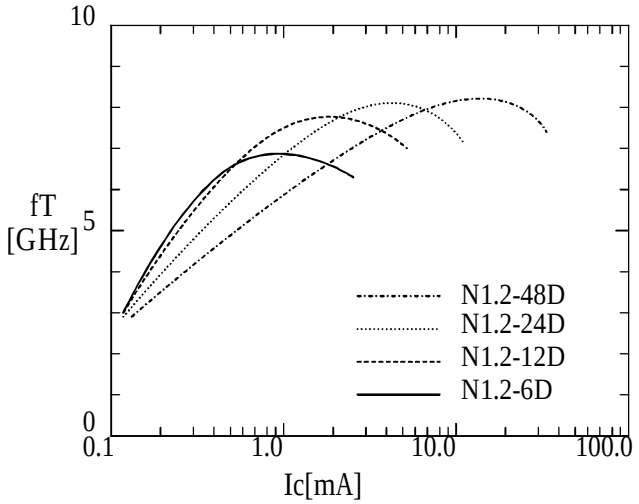

Fig.9 Transition frequency vs collector current for npn transistors.

Accurate model parameters for precise simulation must be generated for various transistor shapes. The authors have developed a program which automatically generates SPICE model parameters to solve this problem [4]. The flow diagram of the transistor model parameter generation program is shown in Fig. 10.

First, the program extracts the transistor shape description from the transistor properties on a schematic, then calculates the geometry dependent parameters from the transistor shape description and generates a set of SPICE model parameters for the shape. In this calculation, this program needs reference transistor model parameters which are based on actual measurements [5]. It also needs the transistor process data and its mask design rule.

Figure 11 shows an actual five-stage ring oscillator which is designed by using the transistor model parameter generation technique.

The oscillator was optimized for high speed operation, so the circuit topology and the current values were fixed, and only the shapes of the transistors at differential pairs were optimized.

The simulation result for the oscillation frequency of the circuit is shown in table 1. From this result, it was concluded that the best shape for the transistors was N1.2-12D. Without this technique, it would have been difficult to determine the shapes of the transistors which best fit the circuit [6] [7].

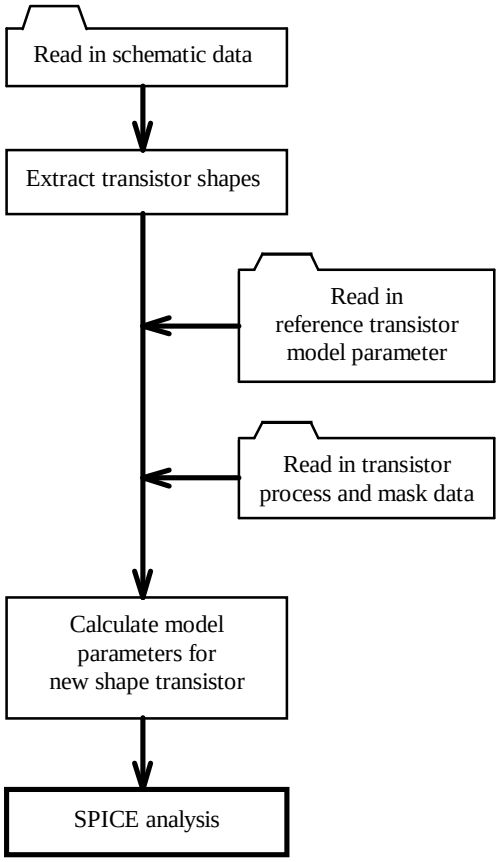

Fig. 10 Flow diagram for transistor model parameter generation program for various transistor shapes

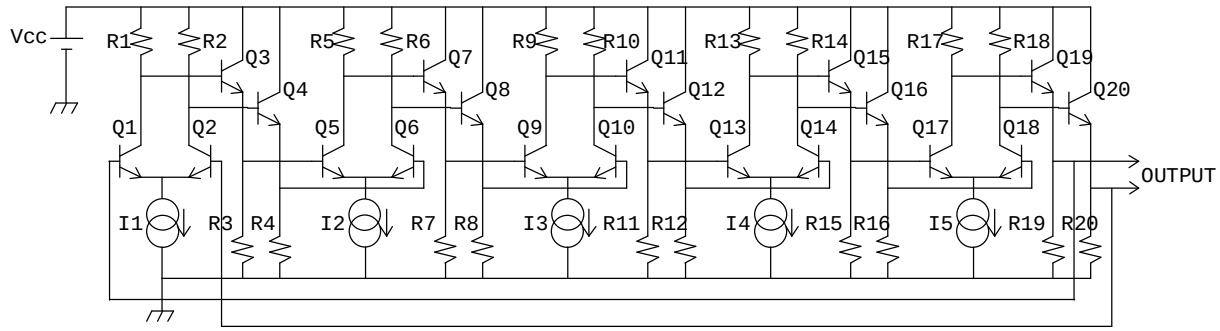

Fig. 11 Five stage ring oscillator

Table 1 Free-running frequency of ring oscillator in which transistor shapes of Q1, Q2, Q5, Q6, Q9, Q10, Q13, Q14, Q17 and Q18 are changed uniformly

Emitter size	Shape of transistor	Free-running frequency
Small	N1.2-6S	477.8 MHz
	N1.2-6D	535.2 MHz
	N1.2-12D	601.3 MHz
	N1.2-24D	588.1 MHz
	N1.2-48D	475.5 MHz
Large	N1.2-48-2D	329.3 MHz

5. Conclusion

Methods and strategies for high frequency analog ICs to achieve a short development period have been described. Due to difficulties, the analog CAD has been far behind the digital CAD which resulted in longer analog design period compared with digital design. The authors have shown that, to reduce the analog design period, a top-down design method which features AHDL and circuit re-use and the model parameter generation technique are very effective. At Toshiba's Multi Media Engineering Laboratory, these methods have been successfully used to reduce the development time.

References

[1] Mantooth, H.A., Fiegenbaum, M., "Modeling with an Analog Hardware Description Language," Analogy Inc., Kluwer Academic Publishers., Boston / Dordrecht / London, 1995.

[2] Vladimirescu, A., Zhang, K., Newton, A.R., Pederson, D. O. and Vincentelli, A.S., "SPICE Version 2G User's Guide (10 Aug. 1981), "Department of Electrical Engineering and Computer University of California, Berkeley, Ca., 94720 Aug.1981.

[3] Gray, P. R. and Meyer, R. G., "Analysis and Design of Analog Integrated Circuits," John Wiley & Sons, New York, 1977.

[4] Miyahara, Y. and Nagata, M., "An Improved Bipolar Transistor Model Parameter Generation Technique for High-Speed LSI Design Considering Geometry-Dependent Parasitic Elements," *Trans. IEICE* vol.E76-A, No.2, Feb. 1993.

[5] Getreu, I. E., "Modeling the bipolar transistor," Elsevier Scientific Publications Co., Amsterdam, 1978.

[6] Miyahara, Y., Metoki, T., Ito, H. and Kobayashi, T., "Single-chip down converter IC for UHF/VHF TV tuner," *IETEC 1991: ITE Annual Conversion*, 23-1, 1991.

[7] Miyahara, Y., Saito, M. and Yamada, Y., "2'nd Converter IC for BS/CS Tuner," *IETEC 1993: ITE Annual Conversion*, 9-2, 1993.