# Low Power and EMI, High Frequency, Crystal Oscillator

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## Abstract

The high-frequency oscillator is one of the major causes of both high power consumption and high Electro-Magnetic Interference (EMI) in Embedded Systems (ES).

This paper presents a high frequency oscillator circuit that reduces substantially both power consumption and EMI, compared to high frequency oscillators currently in use. Using this oscillator spares the need for special isolation techniques used to reduce EMI in ES. It further saves the need for an additional low frequency oscillator that is used for reducing power consumption.

The oscillator is designed for frequencies in the range of 10-60MHz. It consumes 350uA at 40.96MHz with a 5V power supply.

## Introduction

Many ES chip-sets currently use two different crystal oscillators [1], one is a high frequency oscillator, typically in the range of 20-40MHz, and the other is a low frequency oscillator, typically in the range of 32-455KHz. The high frequency oscillator is activated only at normal operation mode, while the low frequency oscillator is activated also in the power down mode in order to update a real time clock, and supply refresh signals for DRAMs.

Using the oscillator presented here, as the high frequency oscillator, provides more than 30db reduction in EMI at the fundamental frequency, and all higher overtones, and at the same time current consumption is reduced by more than 4mA, compared to high frequency oscillators currently used in ES.

The current consumption of the oscillator, when used as a low frequency oscillator, is similar to that calculated at [2].

## **High-Efficiency Oscillator**

The high efficiency of the oscillator presented here is achieved by using the peak-to-peak value of the voltage at the osciallator's input to control its current. Higher peakto-peak values cause less current to flow in the oscillator's amplifier, and vice versa. This ensures fast start-up time, and minimum current waste during steady oscillation. A complete oscillator's circuit diagram is presented in Fig. 1.

The oscillator's amplifier consists of transistors m14m15. Bias current supplied by m14 is expected to hold m15 at the edge of sub-threshold, when oscillation becomes steady.

The peak-to-peak detector is fed from the oscillator's amplifier input. The gate of m4 is biased at  $V_{Tn}$  and therefore its source clips at  $V_{SS}$ . When oscillations occur, the voltage at the gate of m6 oscillates between  $V_{SS}$  and  $V_{peak-to-peak}$ , and the peak-to-peak value is stored on capacitor  $C_2$ . The peak-to-peak voltage is fed to a voltage-to-current converter that has exponential characteristics. The gate of m9 is biased at  $V_{Tn}+|V_{Tp}|$  and therefore transistors m9-m10 are at the edge of sub-threshold. As the peak-to-peak voltage rises, m9 & m10 go deeper into weak inversion and the current to the oscillator's amplifier is reduced exponentially. The bulk of m10 is connected to its source in order to increase the dynamic range of the current, and make the current less susceptible to exponential reduction.

The output amplifier is a class B, push-pull, output stage. Transistor m20 is biased at  $V_{CC}$ - $|V_{Tp}|$  and m21 is biased at  $V_{Tn}$ , by m16-m17 and m18-m19 respectively. Using this configuration dramatically reduces the DC bias current consumption of the circuit. The amplifier's output as a result of 200mv peak-to-peak signal injected at *oscout* is shown at Fig. 2.

Fig. 3 shows the intersection of the following two curves:

(a) The oscillator's amplifier bias current  $(i_{d_m14})$  as a function of peak-to-peak voltage at the input to the peak-to-peak detector (*oscin*);

(b) The peak-to-peak amplitude of oscillation as a function of bias current to the oscillator's amplifier.

The expected operating point is at the intersection of both curves.

Root-Locus of one of the complex conjugated dominant poles, for 42.54MHz crystal at the corners of the process, is shown at Fig. 4.

## **EMI considerations in crystal oscillators**

The EMI caused by a crystal oscillator is the result of high frequency currents in the oscillator. When the circuit on the Printed Circuit Board (PCB), is correctly designed, the current's loop area is relatively small. In this case, when measuring electric field from a far distance, the loop is considered a "magnetic dipole" [3]. The maximum electric field in the far distance [4] is given by (1), where *A* is

the area of the loop, I(f) is the current component at frequency f, and R is the distance from the center of the magnetic dipole.

The measured field is considered as a close field when (2) holds, where *r* is the distance of the probe's head from the line, and  $\lambda$  is the wavelength. The magnetic field is given by (3), where *l* is the length of the wire.

(1) 
$$E_p\left[\mu \frac{V}{m}\right] = 1.317 \cdot \frac{A \cdot I(f) \cdot f^2}{R}$$
  
(2)  $\frac{2\pi r}{\lambda} \ll 1$ 

(3) 
$$H\left[\frac{A}{m}\right] \cong \frac{I(f) \cdot l}{4\pi r^2}$$

#### A. Non-Efficient Oscillator

Fig. 5 describes all the current loops in a "non-efficient" CMOS crystal oscillator [5]. Loop 1 is the loop formed by the crystal and the load capacitors  $C_1$  and  $C_2$ . The current in this loop is the outcome of charge exchange between capacitors  $C_1$  and  $C_2$  during oscillations. In this loop, the current has only the fundamental frequency of the oscillator. Loop 2 is the feedthrough current loop of the oscillator. The feedthrough current is the current flowing from  $V_{CC}$  to ground when both transistors, mp<sub>1</sub> and mn<sub>1</sub>, conduct current. This current is relatively high, due to the sinusoidal signal at oscin. The current conducted by mp<sub>1</sub> comes from the decoupling capacitor C<sub>d</sub> that supplies the currents at high frequencies. Loop 3 is the charging current of capacitor  $C_2$ . Since the signal at *oscout* is not a pure sine wave, it contains also harmonics in the overtones of the oscillator (2f, 3f,...). Transistor  $mp_1$  charges capacitor C<sub>2</sub> in all those frequencies. Loop 4 is the discharge current from capacitor  $C_2$  into the ground, through  $mn_1$ . The discharge current contains the same harmonics as loop 3.

The area of loop 1 is defined by the distance between capacitors  $C_1$ ,  $C_2$  and the crystal. The area of loop 2 depends on the distance between the supply pins of the chip and capacitor  $C_d$ . The area of loops 3 and 4 depends on the distance between the oscillator on the chip and the crystal. Currents in loops 3 and 4 depend on the amplitude of oscillation and the value of  $C_2$ . As the amplitude or  $C_2$ 's value rises, the current increases.

For reducing emission in high frequency oscillator, there are basically two factors which can be controlled: the area -*A* of the loop, and the current -I(f). In some cases, a ferrite bead replaces resistor  $R_1$ , in order to raise the series impedance in the path of loops 3 and 4. Further reduction can be achieved by reducing the feedthrough currents in the oscillator.

## B. High-Efficiency Oscillator

Fig. 6 shows a principle description of the "high-ef-

ficiency" oscillator's current loops. Loop 1 is the charge exchange current between capacitors  $C_1$  and  $C_2$ . Since the amplitude voltage of oscillations is about 400mv, this current is small compared to the "non-efficient" oscillator. Loop 2 is the discharge current loop of capacitor  $C_2$ . Most of the current in this loop is in the overtones frequencies of the oscillator, and it is very small, since the signal at *oscout* has low distortions. Loop 2 has a very small area since both mn and  $C_2$  are placed on the chip, thus contribute negligible emission in the far distance. The charging current of capacitor  $C_2$ , loop 3, comes from the current source - mp, it is a constant current, and therefore neither the  $V_{CC}$  current nor the feedthrough current have high frequency components.

Integrating capacitors  $C_1$  and  $C_2$  internally enables to place the crystal very close to the chip, hence reducing loop area. Effectively, only loop 1 contributes emissions in the far distance.

## Results

The high-efficiency oscillator was integrated in a 0.8um n-well CMOS process as part of an ES controller. Fig. 7 shows the *oscin* and *oscout* signals, AC coupled, oscillation amplitude is 400mv, *oscin* and *oscout* are almost pure sine waves shifted by  $168^{\circ}$ . The start-up process is shown in Fig. 8.

EMI results of the high-efficiency oscillator, compared to results of a "non-efficient" crystal oscillator, that consumes 4.5mA when using the same crystal, are shown in Fig. 9. The EMI difference in the fundamental frequency is 30dB, in the first overtone 35dB, and the difference increases in the higher overtones

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#### References

- [1] National Semiconductor, NSV AM160 ED Board (Parrot board), Reference Manual, March 1992.
- [2] E. Vittoz, M. Degrauwe and S. Bitz, "High-Performance Crystal Oscillator Circuits: Theory and Application", IEEE J. Solid-State Circuits, vol. SC-23, pp. 774-783, June 1988.
- [3] P. Clayton, Electro magnetic Compatibility, New York: Willy, 1992.
- [4] M. Mardiguian, Interference Control in Computers and Microprocessor-Based Equipment, Dom White Consultants Inc., 1984.
- [5] "Oscillators for Micro controllers", Intel, 1983, Application Note AP-155.



Fig. 1. High-efficiency crystal oscillator.



Fig. 2. Output amplifier's in/out.



Fig. 3. Oscillator's operating point.



Fig. 4. Root-Locus of the "high-efficiency" osc.



Fig. 5. "Non-efficient" oscillator's loops.



Fig. 6. "High-efficiency" oscillator's loops.



Fig. 7. Oscin and oscout, AC coupled.



Fig. 8. Oscin and Oscout at Start-up.



(a) "High-efficiency" oscillator.



(b) "Non-efficient" oscillator.

Fig. 9. Magnetic field near the oscillator.