Design Based Analog Testing by Characteristic Observation Inference

Walter M. Lindermeir Helmut E. Graeb Kurt J. Antreich

Department of Electrical Engineering, Institute of Electronic Design Automation
Technical University of Munich, 80290 Munich, Germany

Abstract

In this paper, a new approach to analog test design based on the circuit design process, called **Characteristic Observation Inference (COI)***, is presented. In many situations, it is prohibitive to directly verify the circuit specifications due to the test equipment costs. Our approach considers a given universal set of reasonable input stimuli and measurements that can be performed with the given test equipment. From this universal set, a minimal number of measurements is automatically selected that represent a set of observations characterizing the state of the circuit under test with respect to parametric faults. A parametric fault model is introduced which is related to the individual circuit specifications. For each given circuit specification, a corresponding test inference criterion is computed, based on logistic discrimination analysis. By applying these criteria, the satisfaction or violation of the given circuit specifications can be inferred from the observations of the circuit under test.*

The COI method applied to a complex operational amplifier yields very encouraging simulated results with respect to parametric faults as well as to catastrophic faults.

1 Introduction

Parametric testing of analog circuits is a topic of growing importance [1].

The faults of an analog circuit are usually split into two classes [1]: Parametric faults, which result e.g. from inevitable fluctuations inherent to the manufacturing process are usually modeled by small deviations of the circuit parameters. Catastrophic faults, due to e.g. spot defects, are usually modeled by a topological change of the circuit.

The detection of parametric faults is regarded as a much more difficult problem than the detection of catastrophic faults [2]. Commonly, parametric testing of analog circuits is done by verifying all circuit specifications. A circuit is accepted if all specifications are satisfied. In [3], a more sophisticated test decision based on aggregating all functional tests is presented. Nevertheless, evaluating all performances of the circuit results in a very long production testing time and in strict demands on test equipment. Due to these reasons, analog testing is very expensive. It is estimated to account for about 30% of total manufacturing cost [2]. So the goals of an analog test design are production testing with reasonable test equipment and in short testing time.

The latter is e.g. addressed by the authors in [2, 4, 5]. In [2], a time–optimal ordering of the functional tests is determined and for a given fault coverage some tests can even be eliminated. In [4], an approach called 'Predictive Subset Testing' is presented. Here, a subset of functional tests is determined that is under certain conditions sufficient to test the whole circuit. The approach of [5] determines a minimal number of functional tests such that the system performance is within given bounds. All these approaches need to evaluate the given circuit performances.

In [6], analog fault detection is addressed under the assumption of dc and ac nodal voltage measurements for linear circuits. A hypothesis test is performed with respect to parametric faults. In [7], neural networks are used for fault diagnosis of analog circuits, and different methods for establishing training data sets are investigated. In both approaches, the fault model with respect to parametric faults is geometrically defined in the parameter space. In [6], hyperellipsoids that represent the process statistics are used, while in [7], coordinate hyperplanes are assumed that bound parameter tolerances. As analog testing consists of validating a circuit's functionality, e.g. by checking the satisfaction of the given specifications, it seems worth striving for a fault model closer related to the given specifications of the circuit.

This paper presents a new and very efficient method for the test design of analog circuits. The COI method is based on a novel fault modeling that is closely related to circuit design methodologies [8]. The main improvements of our COI method on the state of the art are that we avoid expensive functional testing and that we maintain a parametric fault model that is related to the given specifications of the circuit. The costs of analog testing can be significantly reduced by integrating the COI method into the manufacturing process. The measurements to be performed are automatically selected from a given universal set of reasonable input stimuli and measurements. This universal set considers the capacity of the available test equipment and restrictions of the test configuration. For instance it can be advantageous to use dc and low–frequency ac input stimuli as especially the high–frequent signal portions are most distorted by the probe. Moreover, on determination of the universal set the COI test design can easily be restricted to consider only measurements at such nodes of the circuit that really can be probed. Therefore, a high grade of practical applicability is provided. For each given circuit specification, a corresponding test inference criterion is computed by applying logistic discrimination analysis. The test decision is made after all selected measurements

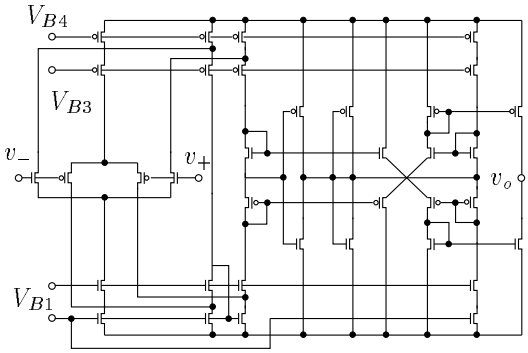

Figure 1: CMOS operational amplifier to be tested.

Gain	GBW	SR_-	SR_+	ΔV_{out}
$>$85dB	$>$4.3MHz	$>$5.0V/μs	$>$8.0V/μs	$>$4.1V

Table 1: Specifications given for the circuit.

have been evaluated.
The paper is organized as follows: In Section 2, the motivation of our approach is given using an operational amplifier as example circuit. In Section 3, the COI method is presented. Section 4 shows the results for the operational amplifier of Section 2. Section 5 concludes the paper.

2 Motivation

Let us regard the CMOS operational amplifier in Fig. 1. The specifications that are given for the circuit are shown in Table 1.
In order to test the circuit with respect to parametric faults, we could measure the given performances of the circuit, i.e. Gain, GBW, SR_-, SR_+, and ΔV_{out}. We would then accept the circuit if all specifications of Table 1 are satisfied.
However, let us assume that we do not want to perform the required measurements, e.g. in order to save testing time and test equipment costs, or because we know that the original performances are insensitive by design. Then, we need to take other measurements from the circuit and derive a test decision whether to accept or to reject the circuit based on these measurements. In this situation, we need to have a universal set of input stimuli and measurements that we can perform reasonably with the given test equipment. This set can usually be obtained from the test engineer. For the testing of the example circuit, we restrict ourselves e.g. to dc and small–signal ac input stimuli. We consider the test configuration shown in Fig. 2. In order to determine the universal set of input stimuli, we select a grid of pairs of operating voltages U_{op} and frequencies ω of the small–signal ac source. The grid positions with respect to the operating voltage U_{op} are 1.5 V, 2.5 V, and 3.5 V. The frequency ω of the small–signal ac source is varied from 1 kHz to 32 kHz in 1 kHz steps. We assume that only signals at the accessible nodes of the circuit can be probed. So we can measure the signals listed in Table 2.

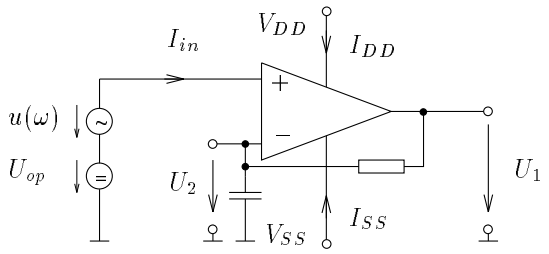

Figure 2: Test configuration for testing the operational amplifier.

DC	I_{in}	I_{DD}	I_{SS}	U_1	U_2
AC	$\lvert\hat{I}_{\mathrm{in}}\rvert$	$\lvert\hat{I}_{DD}\rvert$	$\lvert\hat{I}_{SS}\rvert$	$\lvert\hat{U}_1\rvert$	$\lvert\hat{U}_2\rvert$
	$\varphi\left(\hat{I}_{\mathrm{in}}\right)$	$\varphi\left(\hat{I}_{DD}\right)$	$\varphi\left(\hat{I}_{SS}\right)$	$\varphi\left(\hat{U}_1\right)$	$\varphi\left(\hat{U}_2\right)$

Table 2: Accessible signals.

These measurements are very simple and can be performed without sophisticated test equipment. They contain information of the circuit concerning the non–linear behavior of the circuit by applying different operating voltages U_{op} and they contain information concerning the dynamical behavior of the circuit by using different frequencies ω of the small–signal ac source.
In order to obtain a test inference criterion whether to accept or to reject a circuit based on such measurements, we first of all need to determine a set of parameters reflecting parametric fluctuations of the manufacturing process. Here we consider twelve statistical transistor model parameters, e.g. oxide thickness or length and width reduction, that reflect parametric faults.
We now can outline the main stages of our COI approach:

- In order to provide a short production testing time, we determine a minimal number of input stimuli from the given universal set of reasonable input stimuli. The selected input stimuli are sufficient to characterize the state of the circuit with respect to the statistical parameters that reflect parametric faults of the circuit (Section 3.2). These measurements represent characteristic observations of the circuit under test.
- Based on these characteristic observations, a test inference criterion whether to accept or to reject a circuit is designed. This criterion is based on a parametric fault model that combines circuit specifications, statistical parameters reflecting parametric faults, and characteristic observations (Section 3.3). For each given specification of the circuit, one test inference criterion is computed based on logistic discrimination analysis (Section 3.4). The circuit is accepted if all test inference criteria are satisfied.

3 Proposed approach

In order to apply our design based approach towards analog testing, the following items concerning the design and

testing problem have to be given:

- A universal set of input stimuli and measurements that can be performed reasonably with the given test equipment is available. E.g. for our circuit example, we restrict ourselves to dc and low–frequency ac input stimuli and to measurements at I/O nodes of the circuit. Of course, each measurement recommended by an expert can be added.
- Simulation of the circuit and the testing environment is available.
- The set of statistical parameters reflecting parametric fluctuations is given. Parametric fluctuations are usually modeled as a statistical distribution of these parameters. Therefore, parametric faults can be modeled in the space of statistical parameters.
- Lower and/or upper boundary values for the circuit performances are given. These so–called circuit specifications are required for our fault modeling.

Though our approach focuses mainly on detection of parametric faults we achieve very good fault coverages with respect to modeled catastrophic faults as will be shown in Section 4. This confirms the statement in [2] that parametric faults are much harder to detect than catastrophic faults, and justifies the proceeding of our approach.

3.1 Basic relationships

Since circuit design serves as a basis for the COI approach towards analog testing, we require a few basic relationships from circuit optimization and design centering [9]. The performances $\mathbf{f} \in \mathcal{R}^{n_f}$ of the circuit depend on the statistical circuit parameters $\mathbf{s} \in \mathcal{R}^{n_s}$. For a given set of parameters, the performances can be evaluated by circuit simulation:

$$\mathbf{f} : \mathbf{s} \longmapsto \mathbf{f}(\mathbf{s}). \tag{1}$$

A circuit performance f_i may have a lower bound f_i^L, an upper bound f_i^U, or both a lower and an upper bound. Each lower or upper bound for each circuit performance is called a **specification**.
A circuit is regarded as fault–free if all specifications are satisfied, i.e.:

$$\mathbf{f}^L \leq \mathbf{f} \leq \mathbf{f}^U. \tag{2}$$

If only one specification is given for a performance f_i, the unspecified component f_i^L or f_i^U is set to $-\infty$ or $+\infty$, respectively.
The region in the space of performances $\mathbf{f}$ that satisfies Eq. (2), defines the acceptance region A_f in the performance space. The acceptance region A_s in the space of the statistical parameters $\mathbf{s}$ is defined as the set of parameters that represent fault–free circuits:

$$A_s := \{\mathbf{s} \in \mathcal{R}^{n_s} |\ \mathbf{f}(\mathbf{s}) \in A_f\}.$$

This situation is shown in Fig. 3.
One specification induces a hyperplane of dimension $n_s - 1$ in the space of statistical parameters $\mathbf{s}$. This hyperplane separates the space of statistical parameters such that all circuits satisfying this specification are located on one side of this hyperplane. This is (at least locally) true if we demand that mapping (1) is continuously differentiable taking the implicit function theorem into account.

3.2 Measurement selection

In this section, we deal with the determination of a minimal number of input stimuli and measurements (**observations**) $\mathbf{o} \in \mathcal{R}^{n_o}$ that completely characterize the state of the circuit with respect to the statistical parameters $\mathbf{s}$ that reflect parametric faults of the circuit.
We consider the input stimuli and measurements defined in the given universal set that can be performed with the given test equipment. In general, these are other performances of the circuit than those specified for the circuit. The special case that some specified performances of the circuit are regarded as measurements, too, may occur. We define the space $\mathcal{R}^{n_o}$ of observations $\mathbf{o}$ of the circuit. As for the performances, the observations $\mathbf{o}$ depend on the statistical parameters $\mathbf{s}$ of the circuit:

$$\mathbf{m} : \mathbf{s} \longmapsto \mathbf{o}. \tag{3}$$

This functional dependency is evaluated by circuit simulation. Analogous to the acceptance regions of fault–free circuits in the performance space A_f and in the parameter space A_s, we define the acceptance region A_o in the space of observations (Fig. 3):

$$A_o := \{\mathbf{o} \in \mathcal{R}^{n_o} |\ \exists\ \mathbf{s},\ \ \mathbf{o} = \mathbf{m}(\mathbf{s}) \wedge \mathbf{f}(\mathbf{s}) \in A_f\}. \tag{4}$$

Analogous to the parameter space, one specification induces one separating hyperplane of dimension $n_o - 1$ in the space of observations (Fig. 3).
In order to completely characterize the state of a circuit with respect to the statistical parameters $\mathbf{s}$ by the observations $\mathbf{o}$ of the circuit, mapping (3) has to be a 1–1 mapping. This means: $\mathbf{m}(\mathbf{s}_1) \neq \mathbf{m}(\mathbf{s}_2)$ whenever $\mathbf{s}_1 \neq \mathbf{s}_2$.
We perform a linearization of mapping (3) at the nominal parameter set $\mathbf{s}_0$ of the circuit. This yields

$$\overline{\mathbf{m}} : \mathbf{s} \longmapsto \mathbf{m}(\mathbf{s}_0) + \left.\frac{\partial \mathbf{m}(\mathbf{s})}{\partial \mathbf{s}}\right|_{\mathbf{s}_0} \cdot (\mathbf{s} - \mathbf{s}_0). \tag{5}$$

Mapping (5) is a 1–1 mapping if and only if:

$$\operatorname{rank}\left(\left.\frac{\partial \mathbf{m}(\mathbf{s})}{\partial \mathbf{s}}\right|_{\mathbf{s}_0}\right) = n_s. \tag{6}$$

If this equation holds, mapping (3) is a 1–1 mapping. This is due to the fact that the rank of the sensitivity matrix of the observations with respect to the statistical parameters is constant for almost all parameters $\mathbf{s} \in \mathcal{R}^{n_s}$ (we assume that all observations are continuously differentiable) [10]. Therefore, our algorithm for measurement selection works as follows:

- A sensitivity analysis is performed for all measurements in the given universal set of possible input stimuli and measurements with respect to the statistical parameters $\mathbf{s}$ at the nominal point $\mathbf{s}_0$.

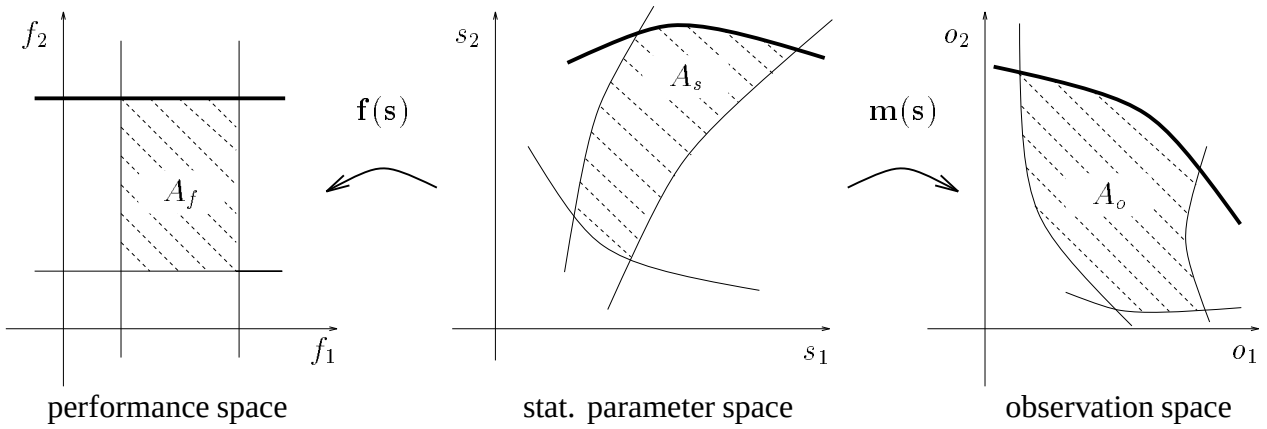

Figure 3: Acceptance regions A_f, A_s, and A_o.

- In order to satisfy Eq. (6) and to provide a good numerical condition of the sensitivity matrix, the most linearly independent and the most sensitive measurements are selected. This is a problem of subspace calculation [11, 12]. We solve this problem by employing e.g. the Householder algorithm.

Please note that all dc measurements are selected in advance and that all signals that can be measured simultaneous to selected ones are added, assuming that the production testing time is not significantly extended by this. This is done in order to gain more information about the circuit under test and in order to increase the detectability of catastrophic faults.

3.3 Fault modeling

Parametric faults are modeled by deviations of the statistical parameters of the circuit [2], considering multiple deviations of these parameters at a time. Usually, the statistical distribution of these parameters is needed to define a parametric fault as a parameter set outside a certain tolerance range [6], or is needed to determine a functional testing order for low testing time [2].
Our fault model is related to the original specifications that would be verified in functional testing. It reproduces the circuit specifications in the space of observations, i.e. it reproduces the acceptance region A_o in the observation space. The acceptance region A_o is hard to obtain. It is not explicitly known, and in real situations, it may be complicated in shape (see Fig. 3).
Therefore, we reproduce each circuit specification in the observation space individually. The acceptance region of one single specification in the observation space is bounded by a hyperplane as indicated by the thick line in Fig. 3. Based on a formal description of this hyperplane, the satisfaction or violation of one original circuit specification can be inferred from the observations of the circuit under test. Therefore, an approximation of this hyperplane is computed, which builds the test inference criterion for the corresponding circuit specification.
The test inference criteria for all specifications together represent the fault model of our approach. A circuit is accepted if all test inference criteria are satisfied for the circuit under test.
Please note that, as our fault model is based on circuit specifications, it only requires the knowledge which parameters are statistically varying. It does not necessarily require the detailed knowledge of the distribution, e.g. variances, correlations. This information is helpful to generate a starting solution and a training data set to compute the separating hyperplanes, but it is not mandatory.

3.4 Logistic discrimination analysis

Here, we will present how one test inference criterion is computed for one specification. The test inference criterion depends on the observations of the circuit. It should be satisfied if and only if the corresponding specification is satisfied.

3.4.1 Introduction and problem formulation

Here, we will give a short introduction to logistic discrimination analysis [13, 14, 15]. For go/no–go testing, two populations Π_1 and Π_2 are considered. We denote population Π_1 as good circuits and Π_2 as faulty circuits with respect to a single specification.
Suppose a set of observations $\mathbf{o} \in \mathcal{R}^{n_o}$ is given such that the observations differ to some extent from one population to the other. The discrimination problem is to find a rule for allocating an object of unknown origin to exactly one of the two populations, based on given observations $\hat{\mathbf{o}}$ of this object. The posteriori probabilities $p\,(\Pi_1|\hat{\mathbf{o}})$ and $p\,(\Pi_2|\hat{\mathbf{o}})$ play an important role for classification. They give the conditional probabilities that an object with a given observation $\hat{\mathbf{o}}$ belongs to population Π_1 or Π_2, respectively. An unknown object with observation $\hat{\mathbf{o}}$ is allocated to the population with the larger posteriori probability. It can be proven that this allocation rule maximizes the probability of correct allocation [13].
The problem arising is that the posteriori probabilities are unknown. So we first of all have to generate a data training set. For the experimental results, this data set was generated by Monte Carlo simulation taking the given process statistics into account. From this training set, the posteriori probabilities can be estimated. In logistic discrimination

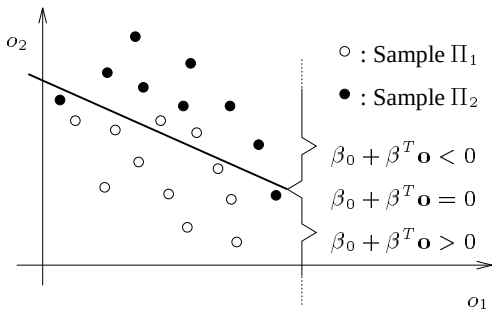

Figure 4: Allocation rule.

analysis, the logistic form for the posteriori probabilities is postulated as [14]:

$$p\left(\Pi_1|\hat{\mathbf{o}}\right) = \frac{\exp\left(\beta_0 + \boldsymbol{\beta}^T\hat{\mathbf{o}}\right)}{1+\exp\left(\beta_0 + \boldsymbol{\beta}^T\hat{\mathbf{o}}\right)}, \quad (7)$$

$$p\left(\Pi_2|\hat{\mathbf{o}}\right) = \frac{1}{1+\exp\left(\beta_0 + \boldsymbol{\beta}^T\hat{\mathbf{o}}\right)}. \quad (8)$$

This induces the following allocation rule:
The object described by the observations $\hat{\mathbf{o}}$ is allocated to the population Π_1 if:

$$p\left(\Pi_1|\hat{\mathbf{o}}\right) \geq p\left(\Pi_2|\hat{\mathbf{o}}\right) \iff \beta_0 + \boldsymbol{\beta}^T\hat{\mathbf{o}} \geq 0, \quad (9)$$

otherwise it is allocated to population Π_2. This allocation rule is illustrated in Fig. 4. All samples that are located below or on the separation line are allocated to population Π_1. All other samples are allocated to population Π_2. Please note that this allocation rule corresponds to a linear approximation of the separating hyperplane in the observation space (see Fig 3).
Logistic discrimination analysis only estimates the parameters that are specifically required for the allocation rule. On the contrary, the classical approach to discrimination analysis, e.g. used in [6] for the detection of catastrophic faults, is to derive the allocation rule from estimates of the probability density of the samples in the two populations: $p\left(\mathbf{o}|\Pi_1\right)$ and $p\left(\mathbf{o}|\Pi_2\right)$. Therefore, many more parameters have to be estimated in the classical approach to establish the allocation rule, yielding a lower accuracy when using the same training samples [14].

3.4.2 Parameter estimation

In this section, we describe how to calculate the parameters β_0 and $\boldsymbol{\beta} \in \mathcal{R}^{n_o}$ that define the allocation rule (9). The likelihood of the observations $\mathbf{o}$ in the training data set is

$$L\left(\beta_0, \boldsymbol{\beta}\right) = \prod_{\mathbf{o}} p\left(\Pi_1|\mathbf{o}\right)^{y(\mathbf{o})} \cdot p\left(\Pi_2|\mathbf{o}\right)^{1-y(\mathbf{o})} \quad (10)$$

where $p\left(\Pi_1|\mathbf{o}\right)$ and $p\left(\Pi_2|\mathbf{o}\right)$ depend on β_0 and $\boldsymbol{\beta}$ due to Eq. (7) and (8), respectively. $y(\mathbf{o})$ is set to 1 if $\mathbf{o}$ belongs to population Π_1. It is otherwise set to 0 if $\mathbf{o}$ belongs to population Π_2.

The parameters β_0 and $\boldsymbol{\beta}$ are obtained by solving the following unconstraint optimization problem [14]:

$$\max_{\beta_0, \boldsymbol{\beta}} L\left(\beta_0, \boldsymbol{\beta}\right). \quad (11)$$

This optimization problem can be solved by using Newton's method.
In order to provide a reasonable **initial estimate** for the numerical solution of (11), we interpret the allocation rule (9) from a more technical point of view. Recall that the observations $\mathbf{o}$ depend on the set of statistical parameters $\mathbf{s}$ of the circuit (Eq. (3)). Therefore, we can rewrite (9) as

$$t\left(\mathbf{s}\right) := \boldsymbol{\beta}^T\mathbf{m}(\mathbf{s}) \geq -\beta_0 =: t^L. \quad (12)$$

This offers the possibility to interpret the allocation rule (9) as a circuit specification for testing the circuit with respect to exactly one given specification. t^L represents a lower boundary value for the circuit performance $t\left(\mathbf{s}\right)$ that can be evaluated by measurements from the circuit under test.
The goal of the presented logistic discrimination analysis is to achieve that the test specification is satisfied if and only if the corresponding circuit specification is satisfied. This implies that the acceptance regions of the original specification and of the test specification in the space of the statistical parameters need to be identical. In [9], a linear approximation of the acceptance region of a single specification for a circuit performance f is presented based on the worst–case point $\mathbf{s}_w$ and on the performance gradient $\left.\frac{\partial f(\mathbf{s})}{\partial \mathbf{s}}\right|_{\mathbf{s_w}}$ of the specification. It is obvious that if the acceptance regions of the original specification and the test specification are identical, this is true for the linearized acceptance regions as well. So the initial solution for β_0 and $\boldsymbol{\beta}$ are given by the following equations [8]:

$$\left.\frac{\partial f\left(\mathbf{s}\right)}{\partial \mathbf{s}}\right|_{\mathbf{s_w}} = \mu \cdot \left.\frac{\partial t\left(\mathbf{s}\right)}{\partial \mathbf{s}}\right|_{\mathbf{s_w}} = \mu \cdot \left.\frac{\partial \mathbf{m}\left(\mathbf{s}\right)}{\partial \mathbf{s}}\right|_{\mathbf{s_w}} \cdot \boldsymbol{\beta}, \quad (13)$$

$$\beta_0 = -t\left(\mathbf{s_w}\right). \quad (14)$$

μ is either $+1$ if the original specification involves a lower bound and -1 otherwise.

3.4.3 Classification quality and interactive adjustment of test specification

As can be seen from Fig. 4, there may be samples that are misclassified. The probabilities of correct classification are given by the following equations:

$$p(1|1) = p\left(\text{ classify a } \Pi_1 \text{ observation as } \Pi_1\right), \quad (15)$$

$$p(2|2) = p\left(\text{ classify a } \Pi_2 \text{ observation as } \Pi_2\right). \quad (16)$$

The classification quality is described by these two probabilities. $p(2|2)$ denotes the probability to detect a faulty circuit. In electronic testing, this probability is commonly defined as **fault coverage** [2]. $p(1|1)$ denotes the probability to accept a fault–free circuit. The problem of discarding good circuits arises in analog testing, e.g. due to measurement errors, and leads to an additional yield loss. Therefore, we call $p(1|1)$ **yield coverage**.

U_{op}	1.5V	2.5V	3.5V
ω	dc 1kHz 23kHz 28kHz 30kHz	dc 30kHz 31kHz	dc 1kHz 28kHz 30kHz 31kHz 32kHz

Table 3: Automatically selected input stimuli.

The goal of discrimination analysis is to make both the yield coverage and the fault coverage as close to 100% as possible. There is a trade off between these two probabilities, that could be considered by introducing different costs of misclassification into the parameter estimation procedure. The problem of such an approach is that these costs are typically unknown. On the other hand, we can provide a graphical support that shows the yield coverage and the fault coverage for the training samples for different boundary values t^L of the test specification (12). This results from parallel shifting of the separation line in Fig. 4 and evaluating the two considered probabilities for the training samples. This is shown e.g. in Fig. 5.

4 Results

We applied our approach to the CMOS operational amplifier shown in Fig. 1. The specifications in Table 1 are given. As mentioned, we consider twelve statistical transistor model parameters for the modeling of parametric faults. The test configuration is shown in Fig. 2. The universal set of possible input stimuli was chosen as outlined in Section 2.

We ran our algorithm for automatic selection of a minimal number of input stimuli. The selected input stimuli are listed in Table 3. The number of measurements in a dc or an ac test is five or ten, respectively (see Table 2). So we obtain $n_o = 125$ observations of the circuit under test.

The test inference criteria were computed with training data sets of different sample sizes (500, 1000, 2000, 4000). β_0 and $\boldsymbol{\beta}$ of allocation rule (9) were computed for each of the five specifications and for the different training sets, by solving optimization problem (11). The training data sets were generated with a Monte Carlo simulation, taking the statistical distribution of the twelve statistical transistor parameters into account. For each sample, all specified performances and all selected measurements were simulated. Multiple parametric deviations are considered, as all twelve statistical parameters are perturbed at a time. The achievable yield coverages ($p(1|1)$) and fault coverages ($p(2|2)$) were verified with a separate 3500 samples Monte Carlo simulation of the parameter distribution. The results are shown in Table 4.

It can be seen that transient performances (SR_-, SR_+) as well as high–frequent ac performances (GBW) can be efficiently tested by the COI method. E.g. the high–frequent ac specification 4.3MHz of GBW (Table 1) can be tested by characteristic observations of not more than 32kHz (Table 3). The quality of our method decreases only slightly if the training sample size is reduced from 4000 to 500 samples. This confirms the statement in Section 3.4.1 that logistic discrimination analysis features a good accuracy with moderate training data sizes.

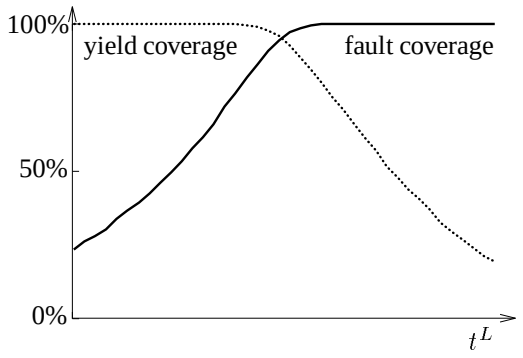

Figure 5: Trade off between yield coverage and fault coverage for specification SR_- (2000 training samples).

In order to provide a means for fine tuning of the trade off between fault coverage and yield coverage, a graphical support shown in Fig. 5 is plotted. For $t^L \to +\infty$, no circuit at all will be accepted by the test. So we have a fault coverage of 100% and a yield coverage of 0% (Eq. (12)). For $t^L \to -\infty$, all circuits will be accepted, which leads to a fault coverage of 0% and a yield coverage of 100%. The test engineer can interactively adjust the boundary value of the test specification t^L with respect to the estimated costs of accepting a faulty circuit and of rejecting a good one.

In order to evaluate the efficiency of our approach with respect to catastrophic faults, we consider gain to drain short, gain to source short, drain contact open and source contact open for each transistor [16]. This fault modeling results in a fault list with 160 faults (single fault assumption; designed shorts as e.g. in current mirrors are removed). With this fault list, analog fault simulation was performed. The results for functional testing and for our COI method are shown in Table 5.

It can be seen that the COI method features a very good fault coverage for the modeled catastrophic faults, while functional testing lags behind. Moreover, all faulty circuits detected by functional testing make up a subset of the circuits detected by the COI method.

One reason for the high efficiency of the COI method for parametric and catastrophic faults may be the measurement selection procedure that selects the most sensitive measurements. On the other hand, the original performances can be less adequate for functional testing, as one goal of circuit design is to make them as insensitive to variations as possible.

5 Conclusion

In this paper, we presented an efficient method for the test design of analog circuits that is based on the circuit design process. The method automatically provides a **minimal number** of **reasonable measurements**, called **characteristic observations**. It therefore addresses the two main problems of analog testing: production testing time and costs of analog test equipment.

#training samples		500		1000		2000		4000	
Spec.	yield	$p(1\|1)$	$p(2\|2)$	$p(1\|1)$	$p(2\|2)$	$p(1\|1)$	$p(2\|2)$	$p(1\|1)$	$p(2\|2)$
Gain	67.6%	95.8%	95.4%	95.8%	97.6%	97.0%	97.9%	97.5%	98.5%
GBW	67.3%	98.0%	93.1%	98.3%	94.8%	98.4%	96.7%	98.1%	98.4%
SR_-	55.4%	95.3%	93.5%	95.3%	94.8%	95.3%	95.3%	95.8%	94.4%
SR_+	67.7%	97.3%	85.1%	97.0%	88.0%	96.7%	89.0%	95.2%	93.7%
ΔV_{out}	51.4%	95.5%	96.5%	95.4%	97.3%	96.4%	97.4%	97.1%	97.7%
total	33.6%	92.4%	96.6%	92.3%	97.5%	93.3%	97.6%	94.7%	97.3%

Table 4: Yield coverages $p(1|1)$ and fault coverages $p(2|2)$ for different training sets. Verification with a separate 3500 samples Monte Carlo simulation.

160 faults considered	# tested	fault coverage
Functional Testing	117	73.1%
COI	158	98.8%

Table 5: Results for catastrophic faults.

A fault model is introduced that is based on individual specification values, on the set of parameters reflecting parametric faults, and on the characteristic observations of the circuit under test. For each given specification, a **test inference criterion** is computed based on logistic discrimination analysis. By applying this criterion, the satisfaction or violation of the original circuit specifications can be inferred from the observations of the circuit under test. The trade off between fault and yield coverage can be interactively controlled. First results of our approach with respect to parametric and catastrophic faults are very encouraging. Further research topics include a more sophisticated sampling strategy [7] and the consideration of measurement errors.

Acknowledgement

The authors wish to thank the SIEMENS AG for facilitating this work by providing circuit examples and statistical data and wish to thank Dr. Ch. Kredler from the Mathematical Institute of the Technical University of Munich for helpful discussions on discrimination analysis.

References

[1] J. L. Huertas. Test and Design for Testability of Analog and Mixed–Signal Integrated Circuits: Theoretical Basis and Pragmatical Approaches. *Proc. ECCTD*, 1993.

[2] L. Milor and A. L. Sangiovanni-Vincentelli. Minimizing Production Test Time to Detect Faults in Analog Circuits. *IEEE Trans. CAD*, 13:796–813, 1994.

[3] M. Fares and B. Kaminska. Fuzzy Optimization Models for Analog Test Decisions. *JETTA*, 5:299–305, 1994.

[4] J. B. Brockman and S. W. Director. Predictive Subset Testing: Optimizing IC Parametric Performance for Quality, Cost and Yield. *IEEE Trans. Semiconductor Manufacturing*, 2:104–113, 1989.

[5] E. Felt and A. Sangiovanni-Vincentelli. Testing of Analog Systems Using Behavioral Models and Optimal Experimental Design Techniques. *Proc. IEEE ICCAD*, pages 672–678, 1994.

[6] B. R. Epstein, M. Czigler, and S. R. Miller. Fault Detection and Classification in Linear Integrated Circuits: An Application of Discrimination Analysis and Hypothesis Testing. *IEEE Trans. CAD*, 12:102–113, 1993.

[7] A. Wu and J. Meador. Measurement Selection for Parametric IC Fault Diagnosis. *JETTA*, 5:9–18, 1994.

[8] W.M. Lindermeir and H.E. Graeb. On the production test of analog circuits by statistical fault modeling. *Archiv für Elektronik und Übertragungstechnik*, 49(2):64–71, 1995.

[9] K. J. Antreich, H. E. Graeb, and C. U. Wieser. Circuit Analysis and Optimization Driven by Worst–Case Distances. *IEEE Trans. CAD*, 13:57–71, 1994.

[10] V. Visvanathan and Alberto Sangiovanni-Vincentelli. A Computational Approach for the Diagnosability of Dynamical Circuits. *IEEE Trans. CAD*, 3:165–171, 1984.

[11] G. H. Golub and C. F. van Loan. Matrix Computations. *2nd Edition, The John Hopkins University Press*, 1989.

[12] P. Comon and G. H. Golub. Tracking a Few Extreme Singular Values and Vectors in Signal Processing. *Proc. IEEE*, 78:1327–1343, 1990.

[13] R. A. Johnson and D. W. Wichern. *Applied Multivariate Statistical Analysis*. Prentice Hall, Englewood Cliffs, New Jersey, third edition, 1992.

[14] J. A. Anderson. Separate Sample Logistic Discrimination. *Biometrika*, pages 19–35, 1972.

[15] J. A. Anderson and S. C. Richardson. Logistic Discrimination and Bias Correction in Maximum Likelihood Estimation. *Technometrics*, pages 71–78, 1979.

[16] Linda Milor and V. Visvanathan. Detection of Catastrophic Faults in Analog Integrated Circuits. *IEEE Trans. CAD*, 8:114–130, 1989.