Rectangle-Packing-Based Module Placement *

Hiroshi Murata †, Kunihiro Fujiyoshi †,
Shigetoshi Nakatake †, and Yoji Kajitani ‡

†School of Information Science, Japan Advanced Institute of Science and Technology
Tatsunokuchi, Ishikawa 923-12, Japan

‡Department of Electrical and Electronic Engineering, Tokyo Institute of Technology
Meguro-ku, Tokyo 152, Japan

abstract

The first and the most critical stage in VLSI layout design is the placement, the background of which is the rectangle packing problem: Given many rectangular modules of arbitrary size, place them without overlapping on a layer in the smallest bounding rectangle. Since the variety of the packing is infinite (two-dimensionally continuous) many, the key issue for successful optimization is in the introduction of a P-admissible solution space, which is a finite set of solutions at least one of which is optimal. This paper proposes such a solution space where each packing is represented by a pair of module name sequences. Searching this space by simulated annealing, hundreds of modules could be successfully packed as demonstrated. Combining a conventional wiring method, the biggest MCNC benchmark ami49 is challenged.

1 Introduction

Layout in physical design of VLSI is, simply to say, to pack all the circuit elements in a chip without violating the design rules, so that the circuit performs well and the production yield is heigh. So much the variety of targets in different stages, the problem defined as follows is the base of all of them.

Rectangle Packing Problem: RP
Let $\mathcal{M}$ be a set of m rectangular modules whose height and width are given in real numbers. (Orientation is fixed.) A packing of $\mathcal{M}$ is a non-overlapping placement of the modules. The minimum bounding rectangle of a packing is called the chip. Find a packing of $\mathcal{M}$ in a chip of the minimum area.

A packing of six modules is shown in Fig.1.

RP can be shown to be NP-hard by reducing an NP-hard problem which is **RP** with a constraint that the width of the chip is fixed[1].

Since the height and width of modules are continuous real numbers, **RP** is not simply a combinatorial optimization problem. Hence there have been several numerical approaches[2, 3].

An alternative approach is "combinatorial search". Define a solution space which is a set of codes. Each code represents a construction of placement. A code is said to be *feasible* if the construction is consistent, i.e. there exists a packing corresponding to the code. The evaluation of a code is the evaluation of the packing (the area of the chip). Search a feasible code which yields the best packing.

If a trade-off to the computation time is imposed, the heuristics will stop the search on the way. Being effective this search, the minimum requirement of the solution space is

(1) The solution space is finite,

(2) Every solution is feasible,

(3) Evaluation for each code is possible in polynomial time and so is the realization of the corresponding packing,

(4) The packing corresponding to the best evaluated code in the space coincides with an optimal solution of **RP**.

The solution space that satisfies the above four requirements is called *P-admissible*.

*This work was supported in part by a Grant in Aid for Scientific Research of the Ministry of Education, Science, and Culture of Japan (05452209) and Research Body CAD21 at JAIST.

The reasons for (1),(3) and (4) are obvious. That for (2) is: most heuristics pick up one solution after another along the neighboring structure defined on the space[4], consulting with the difference of evaluations (gain) to the previous solution. Therefore, if infeasible solutions are included, the continuity will be destroyed and the convergence to a feasible solution is not guaranteed.

A practically known solution space is the one derived from *slicing floorplan* proposed by Otten[5] and others. Since it satisfies (1), (2) and (3) several optimization heuristics are applied for the space, and one of the most successful approaches uses simulated annealing[6]. Since the optimal solution can be non-slicing, it lacks (4). Efforts have been paid to add non-slicing structures[7, 8].

On the other hand, Onodera et.al.[9] uses a solution space by assigning one out of four relations, "left to" , "right to", "above", "below", to every pair of modules. This space satisfies (4) since any packing satisfies a combination of the relations. But there are many infeasible codes such as; module a is left to module b, b is left to module c and c is left-to a. As a consequence, the space does not admit such a heuristics as simulated annealing. In their paper, an exhaustive search with a branch-and-bound technique is applied to find an exactly optimal solution, but the size of tractable problems is limited up to six modules. Thus these two are not P-admissible.

This paper provides a P-admissible solution space, in which each code is a pair of module name sequences. Searching this space, hundreds of modules have become able to be packed very efficiently, almost optimally at a look as in Fig.9 and in Fig.10.

Utilizing this solution space of **RP** for VLSI layout design, the evaluation of a packing has to be modified to consider wires. Many formulae have been proposed for this purpose[6, 9], and we follow [9]. The largest MCNC building-block benchmark is successfully placed by simulated annealing in about 30 minutes(Fig.11).

This paper is organized as follows. In Section 2, a mapping from a given packing to a pair of module name sequences is given, to show that an optimal solution is included. Section 3 provides a procedure of an inverse mapping from a sequence pair to a packing. Section 4 demonstrates how the space can be utilized in placement problems. Section 5 is for concluding remarks.

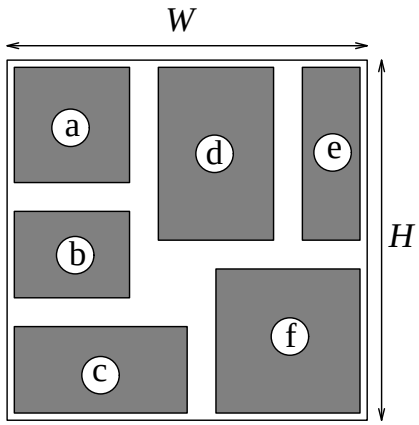

Fig.1: A packing in a chip of area $H \times W$

2 From a Packing to a Sequence-Pair

Let Π be a packing on chip C. See Fig.1 for an example.

2.1 Gridding

A *floorplan* is a partition of C into rectangles, called *rooms*, such that a room contains at most one module. A room which contains no module is said to be *empty*.

The line segments forming the room boundaries (including four sides of C) are called the *cutting-segs*. We assume that a cutting-seg, except for four sides of C, stops at an inside point of an orthogonal cutting-seg (forming a T-intersection). It is trivial that such a floorplan is always possible.

In the following, we describe a procedure to get a pair of module name sequences from a packing.

procedure: Gridding(Π)

> Obtain one arbitrary floorplan and fix it. (See Fig.2 which is an example floorplan corresponding to Π in Fig.1.) Take a non-empty room. Put a pebble p at the center of the room. Move it right up to hit the cutting-seg which is the side of the room. Then, move p upward until to hit an orthogonal cutting-seg. Then, move it right to hit an orthogonal cutting-seg, and continue turning its direction as right, up, right, up, $\cdots$, until to reach

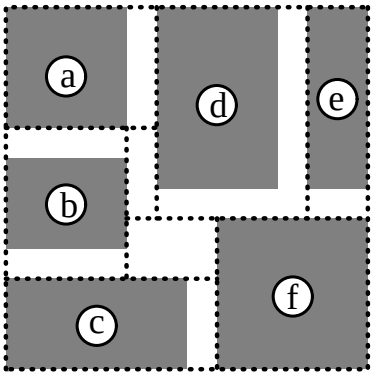

Fig.2: A floorplan of a packing

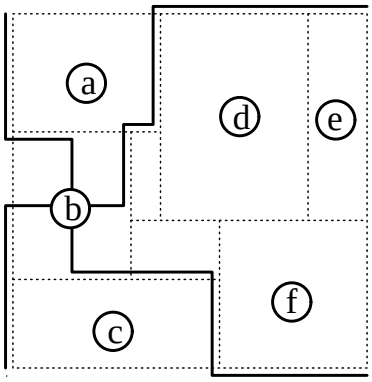

Fig.3: Loci of module b

the upper right corner of the chip. The locus of pebble p is called the *right-up locus* of the module. Similarly, *up-left locus*, *left-down locus*, and *down-right locus* are defined. (Fig.3 shows these four loci of one module.)

The union of right-up locus of x and left-down locus of x is called the *positive locus* (since it tends to go inside the 1st and 3rd quadrants). Analogously, the union of the up-left locus of x and down-right locus of x is called the *negative locus*. For every module, one positive locus and one negative locus are uniquely defined. They are referred to by the corresponding module names. (An example with all loci is shown in Fig.4.)

Theorem 1 :

No pair of positive loci cross each other. No pair of negative loci cross each other. (They may run along the same cutting-segs, but not cross each other.)

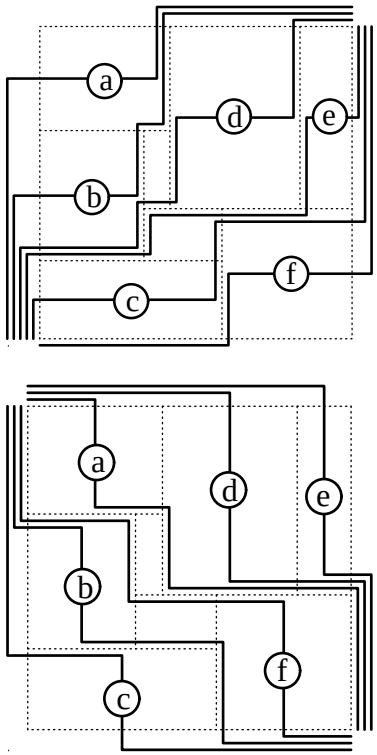

Fig.4: Positive loci(above) and negative loci(below), resulted in $(\Gamma_+, \Gamma_-) = (abdecf, cbfade)$

Proof: Let two modules be a and b. Since positive loci of a and b cannot be inside the other room, a crossing, if any, would occur outside their rooms. Denote the right-up locus of module a be RU(a). Similar notation is applied for the other three types loci.

Suppose that RU(b) comes from below and hits RU(a) at a point p_1. See Fig.5 case 1. Since RU(a) and RU(b) are along cutting-segs, RU(b) cannot cross RU(a) at p_1 by definition of the cutting-seg. After p_1, the two must run for a while. Since they are following the same rule of right-up locus, they run together and never cross each other. Hence, right-up loci of a and b do not cross. By the same reason, left-down loci of a and b do not cross.

Suppose that RU(b) comes from below and hits LD(a) at a point p_2. See Fig.5 case 2. After p_2, RU(b) goes right upstream along LD(a) for a while. Then RU(b) reaches to the point where LD(a) comes from above. After that point, RU(b) continues to go right

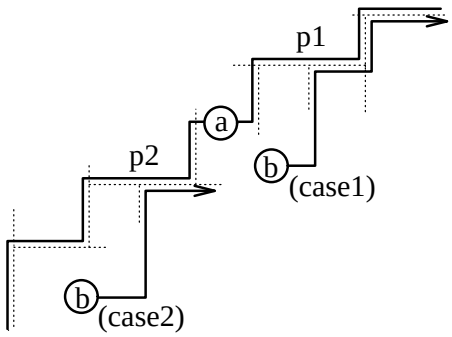

Fig.5: Loci used in the proof of Theorem 1

and thus goes below of LD(a) again. Since RU(b) can not go inside the room of a, it goes below of the room of a. Hence, left-down locus of a and right-up locus of b do not cross. By the same reason, right-up locus of a and left-down locus of b do not cross.

Then, the positive loci of a and b do not cross. Similarly, negative loci of a and b do not cross. □

The implication of the theorem is significant: m positive loci are linearly ordered, and so are negative loci. Here we order the positive loci from upper left, and order the negative loci from lower left. Since each locus is uniquely referred to by the module name, we have obtained an ordered pair of module name sequences (Γ_+, Γ_-), which we call *sequence-pair*, where Γ_+(resp. Γ_-) is a module name sequence which represents the order of positive (resp. negative) loci.

In Fig.4, positive loci are in order "$abdecf$" and negative loci are in order "$cbfade$", then $(\Gamma_+, \Gamma_-) = (abdecf, cbfade)$ is obtained.

Given packing Π, the resultant (Γ_+, Γ_-) obtained by **Gridding** is denoted **Gridding**(Π).

2.2 Geometrical Information of Sequence-Pair

Let **Gridding**(Π) $= (\Gamma_+, \Gamma_-)$. For a module x, any other module x' is uniquely one of four cases, x' is after/before x in Γ_+/Γ_-. Let us define four classes, accordingly.

$\mathcal{M}^{\mathrm{aa}}(x) = \{x' \mid x'$ is after x in both Γ_+ and $\Gamma_-\}$,

$\mathcal{M}^{\mathrm{bb}}(x) = \{x' \mid x'$ is before x in both Γ_+ and $\Gamma_-\}$,

$\mathcal{M}^{\mathrm{ba}}(x) = \{x' \mid x'$ is before x in Γ_+ and after x in $\Gamma_-\}$,

$\mathcal{M}^{\mathrm{ab}}(x) = \{x' \mid x'$ is after x in Γ_+ and before x in $\Gamma_-\}$.

For example, with respect to $(\Gamma_+, \Gamma_-) = (abdecf, cbfade)$, four subsets for module b are: $\mathcal{M}^{\mathrm{aa}}(b) = \{d, e, f\}$, $\mathcal{M}^{\mathrm{bb}}(b) = \emptyset$, $\mathcal{M}^{\mathrm{ba}}(b) = \{a\}$, and $\mathcal{M}^{\mathrm{ab}}(b) = \{c\}$.

Any module other than x belongs to a unique subset, and it is trivial that two modules are in a dual relation through $x \leftrightarrow x'$, and $a \leftrightarrow b$ as:

$$x' \in \mathcal{M}^{\mathrm{aa}}(x) \quad \Leftrightarrow \quad x \in \mathcal{M}^{\mathrm{bb}}(x')$$
$$x' \in \mathcal{M}^{\mathrm{ba}}(x) \quad \Leftrightarrow \quad x \in \mathcal{M}^{\mathrm{ab}}(x')$$

In a packing, if the left side of module x is right to the right side of module x', x is said to be *right to* x'. Similarly, *left to*, *above*, *below* relations between two modules are defined. These notations follow [9].

Theorem 2 :

Let **Gridding**(Π) $= (\Gamma_+, \Gamma_-)$. If $x' \in \mathcal{M}^{\mathrm{aa}}(x)$, then x' is right to x in Π.

The claim holds replacing the pair of words ("$\mathcal{M}^{\mathrm{aa}}$" and "right to") with any of ("$\mathcal{M}^{\mathrm{bb}}$" and "left to"), ("$\mathcal{M}^{\mathrm{ba}}$" and "above"), and ("$\mathcal{M}^{\mathrm{ab}}$" and "below").

Before the proof, an example is shown. In Fig.3, modules d, e, f are in $\mathcal{M}^{\mathrm{aa}}(b)$, and they are right to b in Π.

Proof: We sketch the proof taking an example of Fig.3. Pick arbitrary two modules, b and f. The loci of b divide the chip into four regions. Among them, the region surrounded by the right-up locus of b, down-right locus of b, and the right side of the chip is called the *right-cone* of b. Similarly, the *left-*, *above-*, and *below-cone* denote other three regions.

Suppose f is in $\mathcal{M}^{\mathrm{aa}}(b)$. This implies that the positive locus of f is in the union of the right-cone and below-cone of b. Also it is implied that the negative locus of f is in the union of the right-cone and above-cone of b. The cross point of the positive and negative locus of f is in their intersection, that is, the right-cone of b. Then the module f is in the right-cone of b. All the modules in the right-cone of b must be right to module b by definition of right-up locus and down-right locus of b.

Similarly, the claim holds for the other cases. □

3 From a Sequence-Pair to a Packing

In the previous section, we analyzed the packing, and fixed the way "gridding" to get one sequence-pair

from a given packing. Now we synthesize one packing from an arbitrary sequence-pair.

3.1 (Γ_+, Γ_-)-Packing

Let (Γ_+, Γ_-) be an arbitrary sequence-pair. We define a geometrical constraint derived from (Γ_+, Γ_-).

GeomConst(Γ_+, Γ_-)

> For every two modules x and x', x' must be right to x in Π if $x' \in \mathcal{M}^{\mathrm{aa}}(x)$. This is also the constraint with replacing the pair of words ("$\mathcal{M}^{\mathrm{aa}}$" and "right to") with any of ("$\mathcal{M}^{\mathrm{bb}}$" and "left to"), ("$\mathcal{M}^{\mathrm{ba}}$" and "above"), and ("$\mathcal{M}^{\mathrm{ab}}$" and "below").

A packing Π is called (Γ_+, Γ_-)-*packing* if Π satisfies **GeomConst**(Γ_+, Γ_-).

Corollary 1 : There is a (Γ_+, Γ_-)-packing if (Γ_+, Γ_-) is the sequence-pair obtained by **Gridding**. □

However, we can prove the following fact.

Theorem 3 : For every sequence-pair (Γ_+, Γ_-), there is a (Γ_+, Γ_-)-packing.

Proof: Consider an $m \times m$ grid. Label the horizontal grid lines and vertical grid lines with module names along Γ_+ and Γ_- from top and from left in order, respectively. A cross point of the horizontal grid line of label x and the vertical grid line of label x' is referred to by (x, x'). Then, draw the resultant grid on a plane rotating 45 degrees. (See Fig.6.) Put each module x with its center being on (x, x). Expand the separation of grid lines enough to eliminate overlapping of modules. (Actually, the expansion is enough if it is $\sqrt{2}$ times larger than the longest width/height over modules.) Trivially, the resultant packing satisfies the requirement implied by the given sequence-pair. □

An example is shown in Fig.6 which corresponds to $(\Gamma_+, \Gamma_-) = (abdecf, cbfade)$.

3.2 (Γ_+, Γ_-)-Optimal Packing

Given (Γ_+, Γ_-), an optimal packing of (Γ_+, Γ_-)-packings is said (Γ_+, Γ_-)-optimal. A (Γ_+, Γ_-)-optimal packing can be obtained in $O(m^2)$ time by applying the well-known *longest path algorithm* for vertex weighted directed acyclic graphs. The formulation is given below.

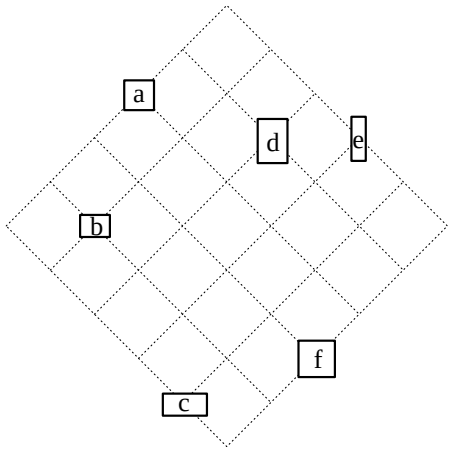

Fig.6: A (Γ_+, Γ_-)-packing
$(\Gamma_+, \Gamma_-) = (abdecf, cbfade)$

Based on "right to" constraint of $(\Gamma+, \Gamma_-)$, a directed and vertex-weighted graph, called *horizontal-constraint graph* $G_H(V, E)$, is constructed as follows.

V : source s, sink t, and m vertices labeled with module names

E : (s, x) and (x, t) for each module x, and (x, x') iff x and x' are in the constraint "x must be left-to x'".

Vertex-weight : zero for s and t, width of module x for the other vertices

Similarly the *vertical-constraint graph* $G_V(V, E)$ is constructed using "below" constraint and the height of each module.

Both graphs do not contain any directed cycle. Furthermore, for every pair of modules, there is always an edge in G_H or in G_V, and not in both. From this fact, the X-coordinate and the Y-coordinate of each module can be determined independently to satisfy the constraint in the direction, and the resultant placement is guaranteed not to contain any overlap. Then, the X and Y coordinates of each module are determined as the minimum by assigning the longest path length between the source and the node of the module in G_H and G_V, respectively. Similarly, the width and the height of the chip is determined as the longest path length between the source and the sink in G_H and G_V, respectively. Since the width and the height of the chip is independently minimum, the resultant packing is (Γ_+, Γ_-)-optimal. The longest path calculation can be done in $O(m^2)$ time, proportional to the number of edges in the graph.

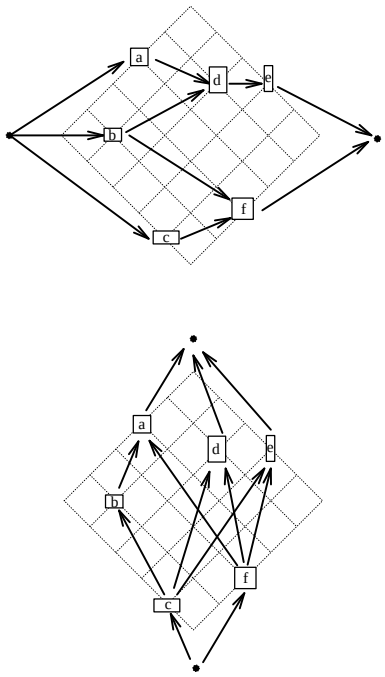

Fig.7: Constraint graphs G_H(above) and G_V(below) (transitive edges are not drawn for simplicity)

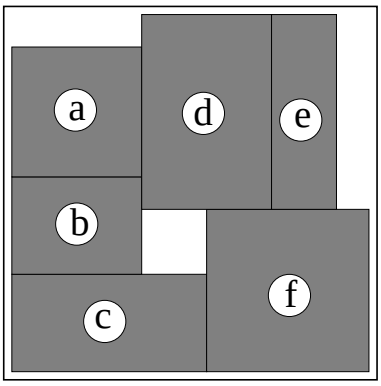

Fig.8: A (Γ_+, Γ_-)-optimal packing for $(\Gamma_+, \Gamma_-) = (abdecf, cbfade)$

As an example, G_H and G_H are shown in Fig.7 for $(\Gamma_+, \Gamma_-) = (abdecf, cbfade)$. The resultant placement after longest path length calculation is shown in Fig.8.

3.3 The P-admissible Solution Space

Previous discussions conclude:

Theorem 4 : The set of all sequence-pairs is a P-admissible solution space of **RP**. More precisely, it consists of $(m!)^2$ sequence-pairs, each of which can be mapped to a packing in $O(m^2)$ time, and at least one of which corresponds to an optimal solution of **RP**. □

Our discussion started for minimizing the area of the chip. However, all the theorems except Theorem 4 do not mention about the evaluation. While, Theorem 4 holds for any evaluating function as long as it is independently non-decreasing both for the width and height of the chip. Therefore we may assume instead, for example, perimeter of the chip, area of chip of pre-specified aspect ratio, and height of the chip when width of the chip is fixed. This fact will expand the applicability of our solution space.

It has also been assumed that the orientation of each module (vertically laid or horizontally laid) is fixed. When the orientation is also requested to be optimized, we hold a $\{0,1\}$ sequence of length m, expressing the orientation of each module is horizontal or vertical. The solution space is enlarged to the size of $(m!)^2 2^m$. (The orientation optimization for a fixed floorplan is known to be NP-hard[10].) This technique can be easily extended for so called "soft" modules, by preparing three or more candidates of (width, height) pairs for one module[11].

4 Experiments

4.1 Rectangle Packing

To show the usefulness of the proposed solution space, dimensions of 146 modules are extracted from a printed circuit board in an industry example, and packed by a simulated annealing method based on three kinds of pair-interchanges of: (i) two module names in Γ_+, (ii) two module names both in Γ_+ and Γ_-, and (iii) the width and the height of a module, where the last one is for orientation optimization. The initial sequence-pair was given by assuming $\Gamma_+ = \Gamma_-$. The temperature was decreased following a quite standard annealing schedule but from a heuristic point of view, operation (i) was selected with higher probability in higher temperature, and operation (iii) was selected with higher probability in lower temperature.

The result is shown in Fig.9. Computation on Sun SparcStationII stopped in 29.9 minutes reach-

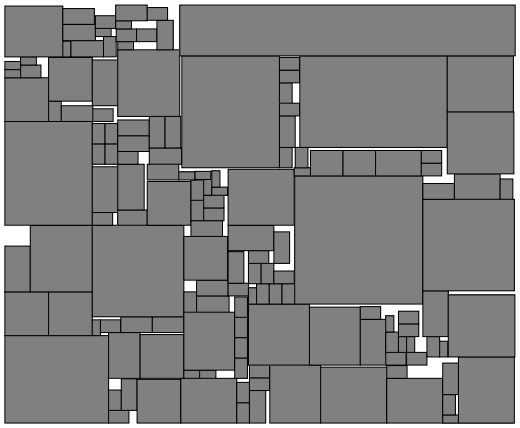

Fig.9: Packing of 146 modules

ing the terminating temperature. The algorithm has searched not greater than 606,192 distinct sequence-pairs out of the solution space of size $(146!)^2 2^{146} \sim 1.23 \times 10^{552}$. Notice that, only the search of a fraction about 4.92×10^{-547} of the solution space was enough to obtain Fig.9. As a challenge, we tried 500 pieces, using 18.83 hours to get the result shown in Fig.10.

4.2 Module Placement with Wire Consideration

For VLSI placement problems, we extend the evaluation to consider wires. Among various possible evaluations about wires, here we focus the final chip area (after every wires are routed in detail). It would be ideal to invent a P-admissible solution space for this evaluation. However, it is difficult at this moment and we make an estimation of final chip area without actual routing phase.

Assume (Γ_+, Γ_-) be a sequence-pair, Π be a (Γ_+, Γ_-)-optimal packing, and W and H be the width and height of Π. Terminals are given as fixed points on the boundary of each module. A *net* is a set of terminals(multi-terminal net), which must be connected by wires, later in detailed routing phase. A set of net is given as the netlist $\mathcal{N}$. When observing the terminals of a net i, which spread over Π, the width and height of the smallest bounding box of these terminals are denoted W_i and H_i, respectively. T is the sum of wiring width and wiring space (obtained from a design rule set). We use following formulae to estimate the final chip width W' and height H', which is the one proposed in [9].

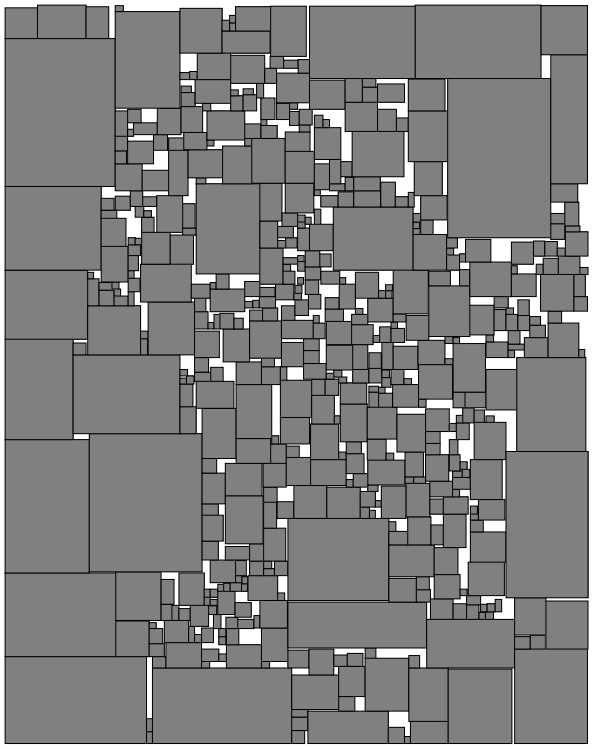

Fig.10: Packing of 500 modules

$$W' = W + T\frac{\Sigma_{i\in\mathcal{N}} H_i}{H}$$
$$H' = H + T\frac{\Sigma_{i\in\mathcal{N}} W_i}{W}$$

The second term of each formula estimates the amount of increase in one direction owing to the wires, assuming all wires are uniformly distributed in the final chip. They experimentally showed that the resultant placement is acceptable for later detailed routing stage.

There are totally eight choices per a module, which is the combination of four choices of $\{0, 90, 180, 270\}$ degree rotations, and two choises of {yes,no} value of the reflection about Y axis. In our system, this code for orientation and a sequence-pair are put together into a simulated annealing process, which runs in a similar fashon as rectangle packing optimization. The process searches the solution space of size $(m!)^2 8^m$.

The point which is not mentioned in [9] is how the location of each individual module is calculated. After the best evaluated code is obtained, coordinates of each module is determined as follows. Assume

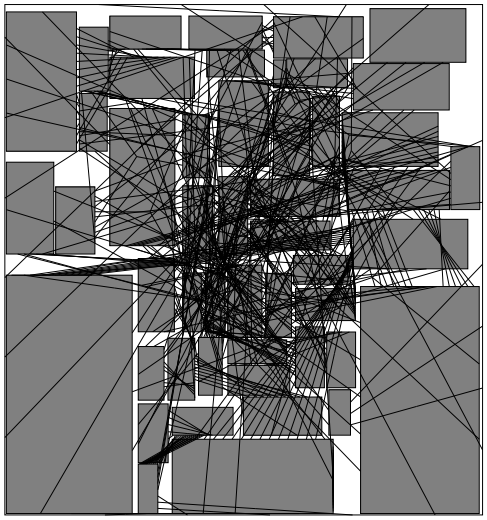

Fig.11: Placement of MCNC "ami49"

(X_j, Y_j) is the coordinates of lower left corner of module j in Π. (Which is the information we can use in this phase.) Let $\mathcal{N}_{X_j}$ be a set of nets such that the X coordinate of left side of bounding box of the net is less than or equal to X_j. Similarly, $\mathcal{N}_{Y_j}$ is defined using Y_j. We determine the coordinates (X'_j, Y'_j) of the lower left corner of module j in the resultant chip by the following formulae.

$$X'_j = X_j + T\frac{\Sigma_{i\in\mathcal{N}_{X_j}} H_i}{H}$$
$$Y'_j = Y_j + T\frac{\Sigma_{i\in\mathcal{N}_{Y_j}} W_j}{W}$$

The biggest building block layout data, called "ami49", is taken from the MCNC benchmarks, and placed by the above described method in a one level computation with additional constraint: aspect ratio = 1. For authors' knowledge, it has not been dealt without hierarchically dividing the problem to reduce the problem size. The result is shown in Fig.11. Computation time was 31.36 minutes on SunIPX.

5 Concluding Remarks

The motivation of this work was our experience that many VLSI designers are not satisfied with slicing structures. This paper has achieved a breakthrough by introducing a P-admissible solution space to the rectangle packing problem, which is fundamental to the layout design.

Experiments suggest that hundreds of rectangles can be packed very effectively in reasonable time. The biggest MCNC benchmark data, ami49, is now tractable without hierarchically dividing the problem, by utilizing the proposed solution space.

As experiments revealed, the search covers only a fraction whole of the solution space. Though the results are of the quality high enough for practical use, the space is too vast. They would hope to create a smaller space but we conjecture that the size of the space can not be decreased drastically.

References

[1] B.S.Baker, E.G.Coffman, and R.L.Rivest, "Orthogonal Packings in Two Dimensions," *SIAM J. Comput.*, vol. 9, no. 4, pp. 846–855, 1980.

[2] L. Sha and R. W. Dutton, "An Analytical Algorithm for Placement of Arbitrarily Sized Rectangular Blocks," in *Proc. 22th ACM/IEEE Design Automation Conf.*, pp. 602–608, 1985.

[3] A.Alon and U.Ascher, "Model and Solution Strategy for Placement of Rectangular Blocks in the Euclidean Plane," *IEEE Trans. on CAD*, vol. 7, no. 3, pp. 378–386, 1988.

[4] Y.G.Saab and V.B.Rao, "Combinatorial Optimization by Stochastic Evolution," *IEEE Trans. on CAD*, vol. CAD-10, no. 4, pp. 525–535, 1991.

[5] R.H.J.M.Otten, "Automatic Floorplan Design," in *Proc. 19th ACM/IEEE Design Automation Conf.*, pp. 261–267, 1982.

[6] D.F.Wong and C.L.Liu, "A New Algorithm for Floorplan Designs," in *Proc. 23rd ACM/IEEE Design Automation Conf.*, pp. 101–107, 1986.

[7] W.M.Dai and E.Kuh, "Simaltaneous Floorplanning and Global Routing for Hierarchical Building Block Layout," *IEEE Trans. on CAD*, vol. CAD-6, no. 5, pp. 828–837, 1987.

[8] T.C.Wang and D.F.Wong, "An Optimal Algorithm for Floorplan Area Optimization," in *Proc. 27th ACM/IEEE Design Automation Conf.*, pp. 180–186, 1990.

[9] H.Onodera, Y.Taniguchi, and K.Tamaru, "Branch-and-Bound Placement for Building Block Layout," in *Proc. 28th ACM/IEEE Design Automation Conf.*, pp. 433–439, 1991.

[10] L.Stockmeyer, "Optimal Orientations of Cells in Slicing Floorplan Designs," *Information and Control*, vol. 59, pp. 91–101, 1983.

[11] P. Pan, W. Shi, and C. L. Liu, "Area Minimization for Hierarchical Floorplans," in *IEEE International Conf. on Computer Aided Design*, pp. 436–440, 1994.