Coping with RC(L) Interconnect Design Headaches[†]

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Abstract

Physical interconnect effects have a dominant impact on today's deep submicron IC designs. In this tutorial paper we will describe the technology trends which have brought about this interconnect dominance, then consider some of the modeling and analysis approximations available for both pre- and post-layout interconnect design.This coverage will not be an exhaustive summary, but one that is primarily focused on moment-based analysis techniques, from the Elmore delay, to the more recent advances in moment-matching approximations, and the corresponding nonlinear driver/load interfaces. Future modeling, analysis, and design challenges will be considered throughout this paper.

1: Introduction

As CMOS technologies are scaled down into the deep submicron range, active-device counts are reaching ten's of millions. The amount of interconnect among the devices tends to grow superlinearly with the transistor counts. For this reason the chip area is often limited by the physical interconnect area, so the interconnect dimensions are also scaled whenever possible. In addition, to generate more wiring area, IC's now commonly accommodate 4-5 or more metallization layers, with more to come in the future.

These advances in technology that result in scaled, multi-level interconnects may address the wireability problem, but in the process create problems with signal integrity and interconnect delay. This tutorial paper will describe some of the technology trends that have resulted in these interconnect design headaches, along with some of the approaches used to analyze and control the problems. We should point out that due to the enormous amount of research in this area, this is not a complete survey paper, but rather a sample of some of the more prominent problems and techniques.

2: Interconnect Trends

At maximum wiring density, each wire sees nearest neighbors on the same layer, as well as wires above and below it, as shown in Fig.1. As device sizes have been scaled for improved performance and increased density, the interconnect sizing, spacing, and conductor thicknesses have been reduced too[4,31,32]. If all of the dimensions (including conductor thicknesses) in Fig.1 are scaled by S, the capacitance per unit length (cross-section) among the wires remains unchanged. In contrast, the resistance per unit length for each wire is increased by $\frac{1}{S^2}$. Therefore, the RC per unit length is increased by the same factor.

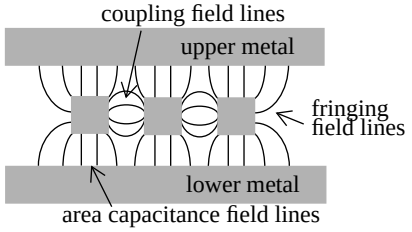

FIGURE 1: Multi-level metal interconnect cross-section. Wires are alternated in direction from layer-to layer.

If all of the lengths of interconnect are scaled, which would be the case for a complete die shrink, then the total RC for the interconnects would remain unchanged. But as device sizes are reduced, there is a tendency to place more functionality on the chip, and therefore the average interconnect lengths do not scale. Moreover, as the devices are scaled, there may be an improvement in their operating

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speed or output impedance that will make the R of the interconnect relatively larger in comparison to the "R" of the driver[3]. So while the operating speed of the gates is improving, the delays of the interconnect between the gates remain fixed. This translates into an increase in the interconnect delay, relative to the driver delay, even when the lengths are scaled. And, without complete length scaling, which is more common, the relative increase in interconnect delay is even more dramatic.

But this analysis assumes that the conductor thicknesses are scaled, and this is not always desirable if interconnect resistance is required to be smaller. If the conductor thicknesses are held constant, then R per unit length of interconnect increases by only $\frac{1}{S}$. However, due to fringing and coupling capacitance effects, the capacitance per unit length increases when conductor thicknesses are not scaled, and the RC per unit length increase is greater than $\frac{1}{S}$.

The cross-sectional capacitance in Fig.1 is calculated from the 2D field lines, and for deep submicron technologies, the fringing fields are a significant portion of the overall capacitance. For example, assume that the metal widths, spacings, and distances to upper and lower layers in Fig.1 are all 4 microns, while the conductor thickness is 0.7 microns. The resulting capacitance terms are shown in Fig.2 for the scale factor value, S=1. Notice that even at 4 microns the fringe capacitance is comparable to the area capacitance for a relatively thin (0.7 micron) wire[3].

Now, scaling all of the width and height dimensions in Fig.1, but leaving the width fixed at 0.7 microns, the area capacitance decreases as expected, but the fringe and coupling capacitances increase. For a scale factor of 0.25, the coupling capacitance increases dramatically, and the total capacitance increases at a faster rate accordingly. Since the resistance also increases in proportion to the scaling, the RC per unit length increase is even more dramatic.

2.1: Coupling Capacitance Effects

When the conductor spacings become comparable to the conductor thicknesses, which is the case for S=0.25 in the example above, the coupling capacitance between wires is significant. One has to be concerned with the coupling between signal wires, as it impacts performance and signal integrity. Moreover, assuming that the wiring layers in Fig.1 represent upper and lower level metal layers, it should be noted that the majority of the total capacitance will be between signal wires for multi-level technologies, and very little capacitance will be to the substrate (ground).

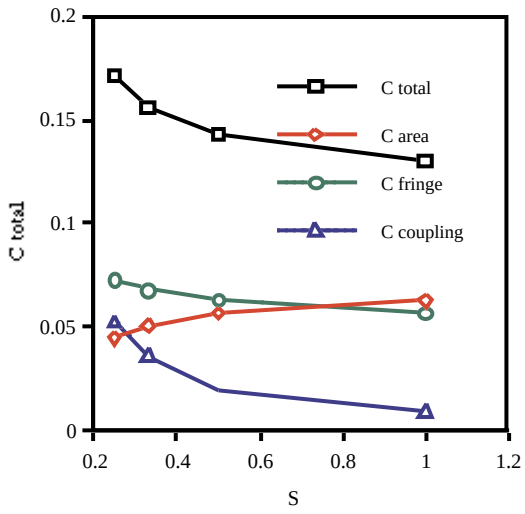

FIGURE 2: Coupling, fringe, area and total capacitance per unit length (fF per micron) of the middle wire in Fig.1 for a fixed wire thickness and scaling of all other dimensions.

For delay analysis purposes we would like to create simple RC models with the capacitance connected from the line to ground. Representing all of the coupling to other wires is generally intractable. But if the coupling is to be modeled as a grounded C, the value is sometimes adjusted to consider the worst case conditions of switching from the other line(s).

Consider two coupled lines, as shown in Fig.3. If one line is switching high, while the other is switching low, the waveform on line 1 may become non-monotone, and the "delay" is increased. If for delay calculation purposes we want to analyze the delay of line 1, independent of line 2, then we can consider modeling the coupling capacitance by an effective capacitance to ground.

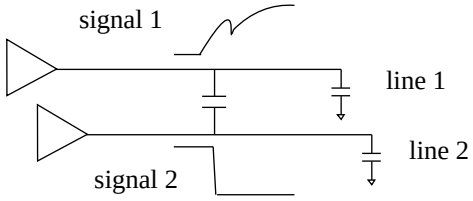

FIGURE 3: Two coupled lines.

For example, referring to Fig.4, assume that the rate of change of signal 1 is $\dot{v}(t)$ and that of signal 2 is $\beta\dot{v}(t)$ (where $\beta \geq 1$) during the time period of switching for line 1, ΔT. While line 2 is switching, the current through the coupling capacitor is $C(1+\beta)\dot{v}(t)$, for a time duration of $\frac{VDD}{\beta}$. The effective capacitance for line 1 (if the coupling capacitor is modeled as a C to ground) is $C(1+\beta)$ for this

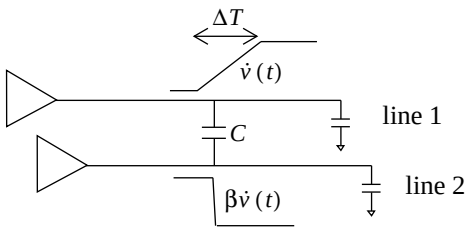

FIGURE 4: Ideal waveshape assumption.

period of time. For the remaining portions of the switching period on line 1, the capacitance is approximately C (it is actually slightly less than C since line 2 is not a perfect ground) for the duration of $\Delta T - \frac{VDD}{\beta}$. In summary, we have a brief period of time for which the effective capacitance is quite large, and then the remaining time the effective capacitance is approximately C. One can average these two capacitors, over the corresponding time periods, which results in an average effective capacitance of $2C$ (as expected since the total change in voltage is $2VDD$). But the actual effect on delay is obtained only by a complete simulation of the coupled lines.

If the lines are switching in the same direction, one can derive a similar formula for the *decrease* in effective capacitance. As we scale to deep submicron technologies and multi-levels of metal interconnect, most of the coupling will be between signal lines, and the pessimistic/ optimistic impact of coupling on delay will become increasingly more significant.

2.2: Inductance Effects?

As technologies are advanced and individual interconnect and device dimensions are scaled, die sizes generally remain constant or increase. If the switching speeds and operating frequencies also increase as the devices scale, then there is the potential for inductance to play a role in the calculation of interconnect delay, or the construction of the interconnect design.

As chip sizes grow, it is increasingly difficult to run long, resistive, metal lines across the chip and operate in the 100's of megahertz. For this reason there have been proposals for using thicker, wider, hence lower resistance metal for the top layer of interconnect to reduce the RC delay[30]. However, if the R per unit length is reduced significantly, the inductance could become a factor.

Up to now, RC models have been used because the on-chip interconnect resistance, R, dominates the on-chip inductive impedance, $|j\omega L|$ (a less conservative measure of the boundary between RC and RLC propagation is given in [35]). While both inductance and resistance tend to increase as the interconnect wire widths are scaled, we expect the operating frequency to increase with scaling too, thereby increasing $|j\omega L|$. As vertical interconnect dimensions are scaled, we might expect the inductance to decrease, due to the tighter return current loops. But because of the poor conductivity of the silicon substrate, the potential decrease in inductance due to smaller vertical dimensions is nullified by the slow-wave effect[35].

In [25] it is claimed that the 200MHz DEC alpha chip was designed with inductive effects in mind. Experiments in [25] illustrate the on-chip inductance effects when very wide lines (so that R is small compared to $|j\omega L|$), or sets of parallel lines over the substrate, are switched in one direction, thereby creating large current transients. To avoid large inductance effects, design rules required that metal return paths were made available so that the return currents were not in the silicon substrate.

3: Interconnect Analysis

Once we have extracted values for the interconnect resistances, capacitances (and inductances), we can analyze the delay, rise-time, noise, etc., by various analysis and simulation algorithms. However, due to the nature and size of interconnect circuit models, one efficient solution approach is in terms of moments, and moment matching. In this section we will review the definition of moments, and explain how and why they are efficiently calculated. But first we consider the interconnect circuit models.

3.1: Interconnect Models

The R and C per unit length values from Section 2 can be used to model the total RC of a straight segment of metal — often referred to as a uniform RC segment (URC). Bends in the metal paths, and vias between metal layers, add additional R and C components that are often described by lumped elements. URCs are best described in the Laplace domain, making them somewhat incompatible with traditional transient-analysis algorithms. But the moments of a URC are easily calculated as described in [20], and convolution of several URCs, in terms of their moments, can be accomplished using special nodal analysis algorithms[20].

But due to the low pass nature of RC circuits, it can be shown that only a small number of lumped segments are required to accurately model a URC, and there is never a need for more than five lumped segments to model any URC for digital circuit applications[9]. Moreover, as inter-

connect paths pass over other metal layers, each metal crossing represents a discontinuity in the per-unit-length C, so there are few *uniform* RCs of sizeable length anyway. Moreover, fewer than five lumps are adequate in most cases.

One conservative estimate for the number of lumped segments (*N*) required to model a URC, based on the maximum signal frequency of interest, is obtained by solving:

$$fmax \le \left| \frac{2N^2}{RC}\left(1 - cos\frac{(2N-1)\,\pi}{2N}\right)\right| \qquad (1)$$

for *N* [9].

One can also create lumped approximations for RLC lines, but these are efficient only if the loss of the line is high (which would probably be the case for any on-chip interconnect). For applications of moment matching, which we are about to consider, there are algorithms for generating lumped circuit approximations with 2p segments that exactly match the first p moments of the distributed circuit model[34,15].

3.2: Calculating Moments for Lumped Circuits

We will demonstrate the steps for calculating moments for the simple, lumped, RC tree circuit shown in Fig.5. We

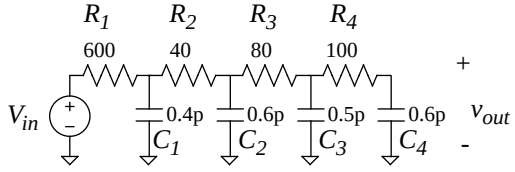

FIGURE 5: Simple RC ladder circuit.

can express the transfer function of this circuit as

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1 + a_1 s + a_2 s^2 + \ldots + a_n s^n}{1 + b_1 s + b_2 s^2 + \ldots + b_m s^m} \qquad (2)$$

where $m > n$. Expanding (2) about $s = 0$ we can rewrite the transfer function as a series in powers of s:

$$H(s) = m_0 + m_1 s + m_2 s^2 + m_3 s^3 + \ldots \qquad (3)$$

The time-frequency domain relationship follows from the Laplace Transform of $h(t)$

$$H(s) = \int_0^\infty h(t)\, e^{-st} dt\,. \qquad (4)$$

Expanding e^{-st} about $s = 0$ in (4) yields:

$$H(s) = \int_0^\infty h(t)\left[1 - st + \frac{1}{2}s^2t^2 - \frac{1}{6}s^3t^3 + \ldots\right]dt = \sum_{k=0}^{\infty} \frac{(-1)^k}{k!} s^k \int_0^\infty t^k h(t)\, dt \qquad (5)$$

It follows from (5) that the *q*-th coefficient of the impulse response in (3) is

$$m_q = \frac{(-1)^q}{q!}\int_0^\infty t^q h(t)\, dt \qquad (6)$$

These coefficients, m_j's, are related to *moments* by the $\frac{(-1)^q}{q!}$ term. That is, from distribution theory, the *n*-th moment of a function $h(t)$ is defined to be $\int_0^\infty t^n h(t)\, dt$. For ease of notation, we often refer to the series coefficients in (3) as moments.

The frequency-domain impulse response of the circuit in Fig.5 can be analyzed in terms of the circuit in Fig.6, where capacitors have been replaced by their complex admittances. From (2) and (3) we know that each capacitor voltage (which are also the node voltages for this circuit) can be expressed in terms of an infinite series in powers of s, as shown in the Fig.6. Expressing the capacitor voltages

$$V^{Cj} = m_0^{Cj} + m_1^{Cj} s + m_2^{Cj} s^2 + \ldots$$

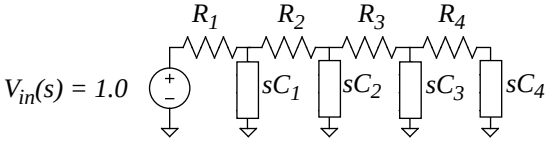

FIGURE 6: Frequency domain representation.

in this way and knowing the capacitor admittances, we can write similar expressions for the capacitor currents, as shown in Fig.7. Since the capacitor currents are a function

$$I^{Cj} = sC_j\left(m_0^{Cj} + m_1^{Cj} s + m_2^{Cj} s^2 + \ldots\right)$$

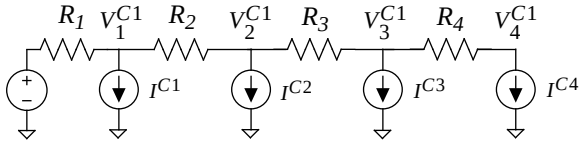

FIGURE 7: Capacitors replaced by current sources.

of the capacitor voltages, we can replace the complex admittances by current sources so that the m_j terms are the only unknowns in Fig.7.

Referring to Fig.7, we can solve for the m_0's for all of the capacitor voltages by setting $s = 0$. Since there are no constant terms (s^0 terms) in the capacitor currents (they are open for $s = 0$), we set the current sources in Fig.7 to zero and solve for the m_0's. For this RC tree, the m_0's are all equal to 1.0, signifying a unity dc gain.

We next solve for the s^1 coefficients, m_1's. It is the s-terms in the current source expressions which produce the m_1's in the voltage responses. Since we know the m_0's, the s-terms in the current source expressions are known. Therefore, we can evaluate the m_1's of the voltage responses by setting all of the current sources equal to $C_j m_0^j$, and solving for the node voltages, which are the m_1^j's. The voltage input for an impulse input has a constant coefficient with all other coefficients equal to zero, so it affects only the calculation of the m_0's.

Higher order moments are calculated following a similar recursion. To summarize, all subsequent moments are calculated from a dc equivalent circuit, as shown in Fig.8.

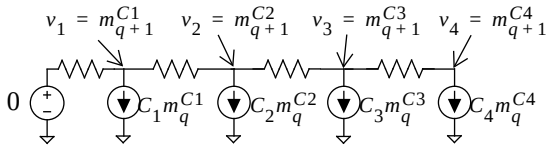

FIGURE 8: dc equivalent circuit to solve for moments.

Note that this procedure for replacing capacitors by current sources to calculate moments holds for all circuit topologies. A more complete explanation of the recursive procedure for calculating moments of general lumped, linear RLC circuits is described in terms of state variables in [23]. Efficient calculation of moments for RLC interconnect topologies is described in [28].

4: Interconnect Metrics

Moments are extremely useful for analyzing RLC interconnect circuits via moment matching (Section 5), but moments themselves are also useful as interconnect metrics. In particular, the first moment of the impulse response, the Elmore delay, is by far the most popular delay metric for RC interconnect trees. Similarly, for RLC trees, the first few moments can be used as metrics for delay and signal integrity control[17].

4.1: Elmore Delay — First Moment

The Elmore delay[7], or first moment of the impulse response, is a popular metric for RC trees since it is perhaps the most accurate delay metric that is a simple algebraic function of the R's and C's. Penfield and Rubenstein introduced this metric and the ease with which it's calculated for RC tree type problems[29]. Two $O(N)$ traversals of the tree, where N is the number of nodes in the tree, yield the Elmore delay for node *i*:

$$T_{D_i} = \sum_{k=1}^{N} R_{ki} C_k \qquad (7)$$

where R_{ki} is the resistance of the portion of the (unique) path between the input and node *i*, that is common with the (unique) path between the input and node *k*, and C_k is the capacitance at node *k* [29].

Recently it was shown that the Elmore delay is an absolute upper bound on the 50% delay of an RC, even for finite rise-time input signals[10]. But it was also shown that this bound results in large relative delay errors for different nodes of the same circuit.

For example, consider the RC tree circuit in Fig.9. The

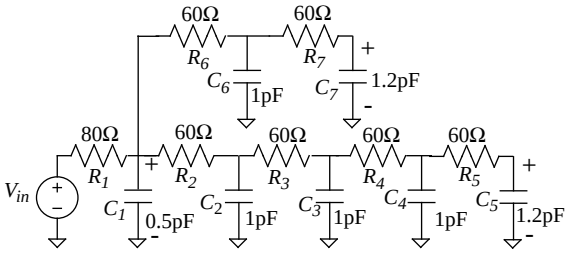

FIGURE 9: SImple RC tree example circuit

impulse ($h(t)$) and step responses for the capacitor C_5 voltage are shown in Fig.10.The 50% point delay of the

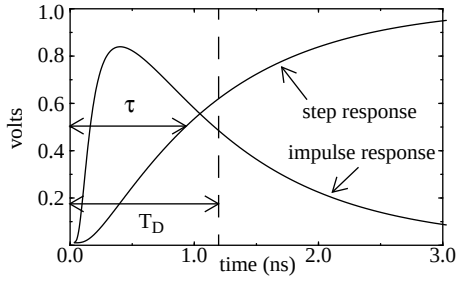

FIGURE 10: : The unit step and the unit impulse (scaled) responses for the voltage at C_5 in Fig.9.

monotonic step response (nonnegative transfer function) is

the time τ at which $\int_0^\tau h(t)\,dt = 0.5$. Referring to Fig.10, Elmore proposed to approximate τ by the mean of the $h(t)$ distribution:

$$T_D = m_1 = \int_0^\infty t\,h(t)\,dt \tag{8}$$

where, $\int_0^\infty h(t)\,dt = 1$. This approximation is exact for a symmetrical impulse response, where the mean is equal to the median, but it is somewhat erroneous for an actual impulse response (e.g. Fig.10) that is skewed asymmetrically.

The accuracy of the Elmore delay will be affected by the spread (variance) and skew (asymmetry) of the impulse distributions. Unfortunately, the impulse response shape, hence the Elmore delay accuracy, changes dramatically from one node to the next in an RC tree. The fact that T_D is a better approximation of the net delay farther away from the driving point is illustrated in Fig.11 which displays impulse responses for 3 different nodes from a 25 node RC tree. From this example we would expect the Elmore delay to become more accurate toward the leaf nodes of the tree, where the impulse response shape approaches a more symmetrical distribution [10].

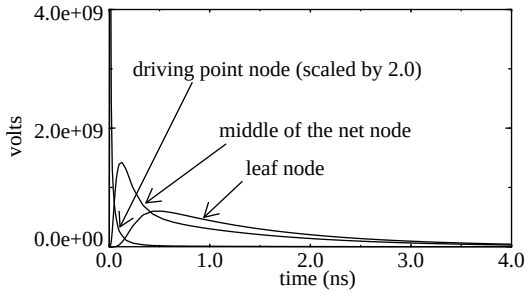

FIGURE 11: Impulse responses for 25 node RC tree.

From distribution theory, the 2nd and 3rd central moments μ_n of a distribution function, which represent the variance and skewness respectively, are given by:

$$\mu_2 = 2m_2 - m_1^2 \quad \textit{and} \quad \mu_3 = -6m_3 + 6m_1m_2 - 2m_1^3 \tag{9}$$

From Fig.11 it is apparent that three central moments may be required to estimate the delay with less relative error. Using the Elmore delay as a dominant time constant scales the delay approximation by 0.7 and can help the relative errors somewhat, but not sufficiently in all cases, and with some of the estimates becoming optimistic[10].

4.2: RLC Metrics

Recently, metrics for RLC interconnects have been proposed based on the first three central moments[17]. Three moments are used to detect underdamping (ringing), specify proper termination, and estimate delay provided that the line is properly terminated. As lower resistance on-chip interconnects are developed, central moments may become important for detection and control of inductance effects.

5: Moment Matching

If more moments are required for an accurate approximation, moment matching can be used to generate reduced-order dominant pole/zero approximations for the interconnect transfer functions and impedances. Asymptotic Waveform Evaluation (AWE)[23] uses 2q moments to generate a q pole transfer function approximation, where q is much less than the order of the circuit.

If we expand the transfer function in (2) into its partial fractions,

$$H(s) = \frac{1 + a_1 s + a_2 s^2 + \ldots + a_n s^n}{1 + b_1 s + b_2 s^2 + \ldots + b_m s^m} = \sum_{j=1}^{m} \frac{k_j}{s - p_j} \tag{10}$$

we observe that for the case of distinct poles the time domain impulse response is

$$h(t) = \sum_{j=1}^{m} k_j e^{p_j t}\,. \tag{11}$$

Where the p_j 's are the poles and the k_j 's are the corresponding residues.

We can uniquely specify the poles and residues by forcing the first 2q moments of (11) to match the first 2q moments from (3)[23]. Although this is recognized to be a form of Padé approximation, which is prone to producing unstable models of stable systems [12,24], there have been various algorithms proposed which generate stable low-order models with excellent reliability[1,2,13,12,18]. In addition, the recent introduction of the PVL algorithm provides a means of getting stable Padé approximations, with controlled error, when a large set of dominant poles are required[8].

6: Interconnect and Driver Interaction

All of the efficient moment-based models for interconnect analysis are for *linear* circuits. The overall behavior and performance of a signal on the interconnect path is strongly dependent upon the nonlinear drivers and loads too.

One straightforward way of combining moment-matched models (e.g. AWE) and nonlinear components (e.g. transistors) is to characterize the linear interconnect

portion of the circuit by a reduced order N-port. For example, approximate the y-parameters in terms of the dominant poles and zeros. Such approaches work well when there are a small number of ports[27,16], but they become extremely inefficient as the number of ports become large.

Of perhaps greater interest is the interfacing of interconnect models with higher-level gate or transistor timing models, since these are the pre- and post-layout design models used to analyze large portions of the chip.

6.1: Timing level modeling

As discussed in Section 2, the percentage of the delay due to the RC interconnect increases relative to the gate delay with scaling. Another effect that contributes to the relative increase of the RC interconnect delay is the resistance shielding effect. If the resistive component of the RC load is comparable or larger than the gate output impedance, the gate does not "see" all of the capacitance loading since the metal resistance "shields" some capacitance.

Most gate level models are incompatible with RC interconnect loads, but it is important to consider this shielding effect. There are two popular approaches to gate modeling: 1) empirically derived expressions for delay and output-signal transition time as a function of load capacitance and input-signal transition time (*k*-factor equations)[33], and 2) switch-resistor models [14,22,11]. It would appear that the switch-resistor model is a more effective delay model when the load is not purely capacitive, since it naturally captures the interaction of the gate's output resistance and the RC load. However, both methods are empirically-based, since even the switch-R method requires empirical fitting [22,5] to approximate the resistance value as a function of input transition time and output load.

Due to the increase in total metal resistance with scaling, and the tendency for the gate output resistances to decrease as technologies are advanced, the RC shielding effect is significant for deep submicron CMOS. To illustrate this point, consider a simple gate model driving a distributed RC interconnect, with a load capacitance at the end of the line, as shown in Fig.12. Assume that the gate is modeled by a resistance and a Thevenin voltage source that are a function of input transition time and output capacitance load. In this case, assume that the gate output resistance, R_d, and Thevenin voltage signal were selected as those values that would yield the same output delay and transition time as the actual gate when the load is the total capacitance, $C_M + C_L$.

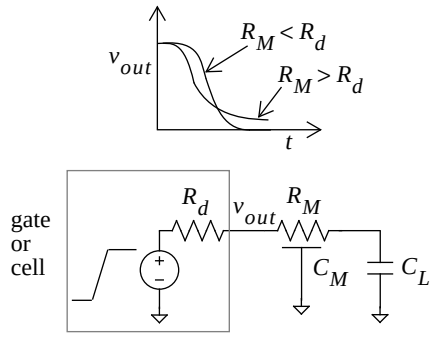

FIGURE 12: Gate driving RC load for different metal resistances.

If $R_d \gg R_M$, then the gate delay is accurately characterized by the empirical model as a function of total capacitance. However, if we consider the same gate resistance and total load capacitance, but increase the metal resistance so that $R_d \ll R_M$, then the gate delay at node v_{out} will *decrease*, since the metal resistance will tend to shield some of the load capacitance. The difference in responses are sketched in Fig.12. Note that the gate delay decreases, but the overall delay at C_L would increase due to an increase in R_M. We should also point out that the responses for lines with significant metal resistance also tend to have non-digital shaped waveforms as shown.

In order to preserve the simplicity and efficiency of these empirical gate models for complex RC loads, one can map the complex load to an *effective capacitance* [26]. A recent model, which captures the gate and load interaction, and produces accurate gate-output waveshape approximations is described in [6]. The importance of modeling this effective capacitance loading for high-speed design was analyzed in [19].

7: Future Considerations

If interconnect effects dominate IC performance, it is imperative to consider their impact in the early design phases. One must consider sizing the interconnects, instead of or in addition to the gates, for high performance design. This requires advances in physical extraction to produce accurate circuit models as a function of wire sizing. Also required are new physical design tools, such as variable width routers. Early analyses must also be advanced to consider coupling between lines, complex waveshapes, and determination of when and how to insert repeaters in the interconnect paths.

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