Software System for Semiconductor Devices, Monolith and Hybrid ICs Thermal Analysis.

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Abstract. *A three level software system for thermal analysis of semiconductor devices, one-chip monolith IC's, multi-chip modules (MCM) and hybrid IC's is presented.*

For each design level the 3D temperature simulators are described to analyze the steady state and transient thermal behavior and connect the design results with the device and/or IC layout and packaging constructions. Practical examples are discussed illustrating the possibilities of developed techniques and software tools.

Introduction

Thermal effects are a limiting factor in the development of IC's. Accurate modeling of the stationary and transient thermal behavior of IC's is necessary to:

1) obtain a realistic evaluation of the reliability of circuit from an electro-thermal standpoint;

2) appropriately lay out the circuits reducing the rise in temperature caused by heat generated in the chips;

3) stabilize electrical characteristics by reducing temperature gradients;

4) reduce thermal mechanical deformation and stress.

Actually, there are several temperature distribution mechanisms in IC's. One mechanism, called global heating, is the rise in the overall chip temperature due to the total power dissipated on the chip. This temperature rise is controlled by the chip-to-package and package-to-ambient thermal impedances. For large-area devices, or those dissipating large power, there can be direct coupling between the heat dissipated in one device and the temperature of the other devices. This mechanism is strongly affected by the circuit layout. The third mechanism is the self-heating of a transistor by its own power dissipation and cannot be eliminated through scaling or layout.

Prior thermal simulators [1-3] are too specific and cannotconsider all three mechanisms commonly.

In this paper the 3D and quasi-3D thermal simulators linked together to form a unified analysis system are presented (fig. 1). They allow the designer to make reasonably accurate predictions on a wide variety of designs/analysis of semiconductor devices, sensors, one-chip monolith IC's, MCM's, HIC's and other packages. They all have multi-layered structures in which various materials with different properties are bonded (fig. 2).

1. Electro-thermal Analysis Program of power IC's elements.

This program is applied to high speed switch transistors of ECL, power output transistors of analog, A/D, D/A IC's, discrete power transistors, semiconductor sensor elements where modeling of the self-heating effect is necessary.

The DC mathematical model is based on the equation for electrical potential $U_\xi(x,y)$ and current density $j(x,y,U_\xi,T)$ distributions in the semiconductor regions (emitter, base, collector for bipolar devices or source, drain, substrate for MOS)

$$\nabla[\sigma_\xi \nabla U_\xi]=j(x,y,z,U_\xi,T),\ \xi=e,b,c\ (s,d,g,sub) \quad (1)$$

where σ_ξ - electrical conductivity

and classical heat-flow-equation in 3D-space:

$$\nabla^2 T(x,y,z)=0 \quad (2)$$

with different boundary conditions:

$$[\lambda \frac{\partial T}{\partial n} + \alpha T]_l = Q_l \ (2,a) \qquad \lambda_l \frac{\partial T}{\partial n_l} = \lambda_{l+1} \frac{\partial T}{\partial n_{l+1}} \ (2,b)$$

$$T_l=T_{l+1} \ (2,c) \qquad T(x,y,z)|_l=T_o \ (2,d)$$

The self-consistent system (1)-(2) is solved numerically with adequate boundary conditions by Newton-Kantorovich and SOR-method with respect to layout (x,y) - plane. The solution of eq. (2) is found by applying multiple finite Fourier

transforms [4]. A computer program based on this solution gives the 2D-current density j(x,y) isolines on the layout surface and 3D-temperature distribution T(x,y,z) in device structure. The program is implemented on VAX 11/780 and IBM PC. Maximum size of difference grid in x, y is 257x257.
As an example the temperature and potential 2D distributions in structure of high current multi-emitter transistor of power analog IC is presented at fig. 4.

2. Programs for Thermal Analysis of monolith IC's.

These programs are applied to one-chip IC's with different package constructions. More important are two polar types:

1) low- and middle-power large-scale precise operational amplifiers, comparators, D/A and A/D converters;

2) power TV, audio amplifiers, smart power IC's for automotive electronics and motor driving etc.

3D steady - state thermal IC's analysis program solves the equation (2) for multi-layer structure with boundary conditions adequate to the different packages. After descretization of eq. (2) the multiple Fourier transforms are used determining Fourier components $T_{i,l}(Z)$ of the thermal transfer function:

$$T_{i,l}(z) = T_s + P_{0,0}(z_s - z) + \sum_{\alpha=0}^{M}\sum_{\beta=0}^{N} \bar{P}_{\alpha,\beta} sh[\sqrt{\mu_{\alpha,\beta}}(z_s - z)]\cos\frac{\alpha\pi i}{M}\cos\frac{\beta\pi l}{N},$$

where i=0,M; l=0,N and $P_{\alpha,\beta}$-Fourier component of power dissipation.
The solution is discussed in more details in [5].

The program is implemented on VAX11/780 and IBM PC. The maximum number of heat dissipation elements is 500, size of difference network is 257 x 257.

The possibilities of the program are illustrated by:

1) lay out design of low-power OA 153UD6, taking into account thermal symmetry and intercommunion of elements (fig. 5);

2) thermal distribution in the power R-G-B color chip of TV-set (fig. 6).

3D transient thermal IC's analysis program calculates the temperature distribution of different packages by solving the transient heat-flow equation in 3D space

$$\lambda\nabla^2 T(x,y,z,t) = \rho c\frac{\partial T}{\partial t} \qquad (3)$$

The solution of eq. (3) is described by T(x,y,z,t)=

$$\sum_{i=0}^{n}\gamma_i z^i \sum_{k=0}^{\infty}\sum_{l=0}^{\infty}\sum_{m=0}^{\infty} B_{klm} e^{-\lambda_{klm}^2 t} v_{klm}(x,y,z)$$

,
where *n*-number of package structure layers,

v_{klm}-defined from boundary conditions between layers.

The mathematical aspects of this problem is discussed in [6].

The program is implemented on VAX11/780 and IBM PC.

In fig.7 the thermal pulse response of OA 153UD6 after feed turning on and off is presented. In fig. 8 the temperature rising process in the structure of sensor transistor of smart power IC after switching on is shown illustrating the development of a carefull layout for the IC delayed protection.

3. Quasi - 3D thermal HIC's analysis program

The formulation of HIC thermal analysis problem can be simplified by the linearisation of the solution $T_{i,l}(x,y,z)$ along z because $L_x,L_y>>L_z$. (see fig. 3). After that the 3D-problem is reduced into two 2D-subproblems for the dielectric substrate and adhesive layers in x,y plane which are solved by SOR method.

$$0.5\nabla[\lambda_{sub}Z_{sub}\nabla T_{sub}(x,y)] - \frac{\lambda_{sub}}{z_{sub}}(T_{sub} - T_{ad}) = -f(x,y);$$

$$0.5\nabla[(\lambda_{sub}Z_{sub} + \lambda_{ad}Z_{ad})\nabla T_{ad}(x,y)] + \frac{\lambda_{sub}}{z_{sub}}(T_{sub} - T_{ad}) - \frac{\lambda_{ad}}{z_{ad}}(T_{ad} - T_{hs}) = 0;$$

where $\nabla = \frac{\partial}{\partial x}i + \frac{\partial}{\partial y}j$; f(x,y)= Psour, (x,y)∈ Ssour
.

The program is implemented on VAX 11/780 and IBM PC. The maximum number of heat-dissipation elements - 200, grid size - 257x257.

The possibility of the program is illustrated by steady state solution in multi-layer HIC - structure with total power 15W. (see fig. 9).

The power transistors and IC chips are placed on the glass ceramic substrate with λ=1.47 10^{-3} W/(mm K) (left side); The resistors are placed on the substrate with λ=30 10^{-3} W/(mm K) (right side).

Conclusions.

A unified software system for three level thermal analysis has been developed. It is widely used for thermal design and/or analysis of power discrete and IC devices and sensors; monolith one-chip IC's and VLSI's fabricated in Si and GaAs wafers; hybrid IC's and MCM. The steady state and transient modeling results are in good agreement with the thermal pictures measured by infrared and luquid crystalline techniques.

3D temperature simulators are connected with circuit simulator PSPICE to make a mixed electrical-thermal analysis of IC's and HIC's providing the additional power for ASIC-designer.

References

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6., Koljago V.I. Transient Thermal Analysis of Integrated Circuits. Computer technique and numerical problems. Proc. of Latvien Techn. Univ., Riga, 1990, pp. 67-77.

Fig. 1. Software system for semiconductor devices,monolith and hybrid IC's thermal analysis.

Fig. 2 Schematic representation of power IC.

Fig. 3 Formulation of hybrid IC thermal analysis problem.

Fig. 4 Temperature and potential 2D-distributions in structure of high current multi-emitter transistor of power analog IC.

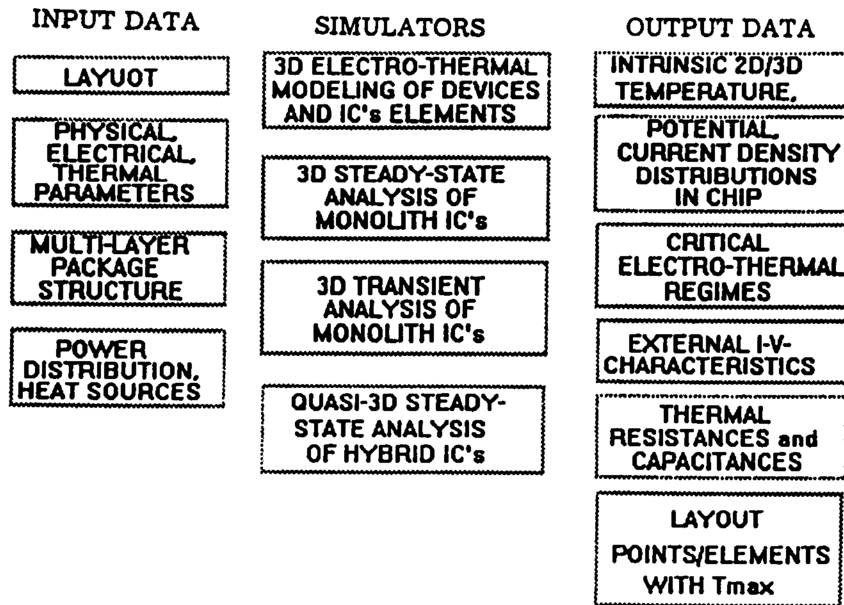
Fig. 5 2D-thermal distribution over the substrate surface of OpAmp 153UD6 chip.

Fig. 6 Map of the temperature distribution over the substrate surface of TV-set R-G-B colour chip K174AF5.

Fig. 7 Transistor T32 thermal transient response after OA153UD6 (see fig. 5) turning on at t=0 and turning off at t=40s.

Fig. 8 The temperature rising process in the structure of sensor transistor of smart power IC after switching on.

Fig. 9 Thermal modeling of hybrid IC with total power dissipation 15 W.



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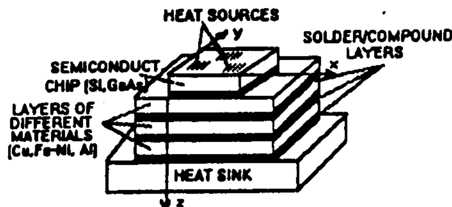
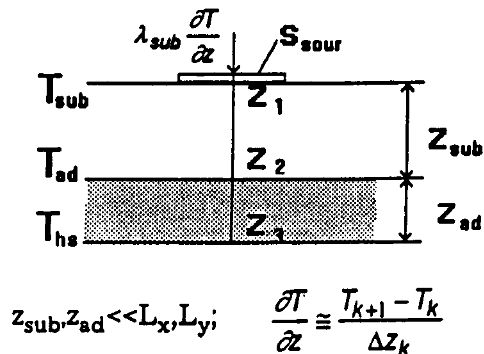


Fig. 2 Schematic representation of power IC.



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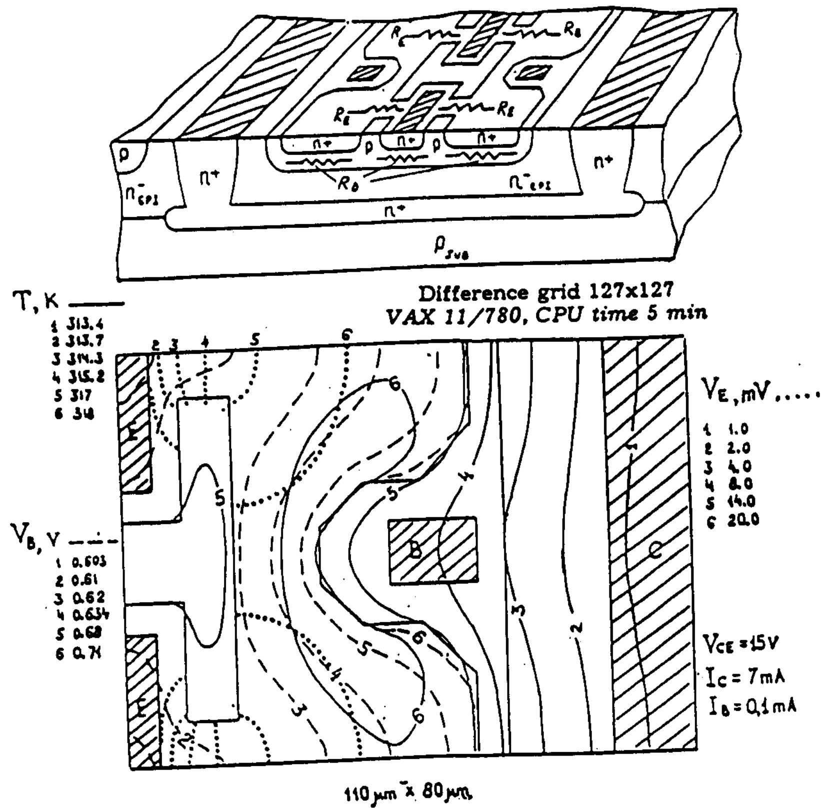


Base and emitter potential 2D-distributions in one section of high current power transistor with H-base region configuration.

Fig. 4 Temperature and potential 2D-distributions in structure of high current multi-emitter transistor of power analog IC.

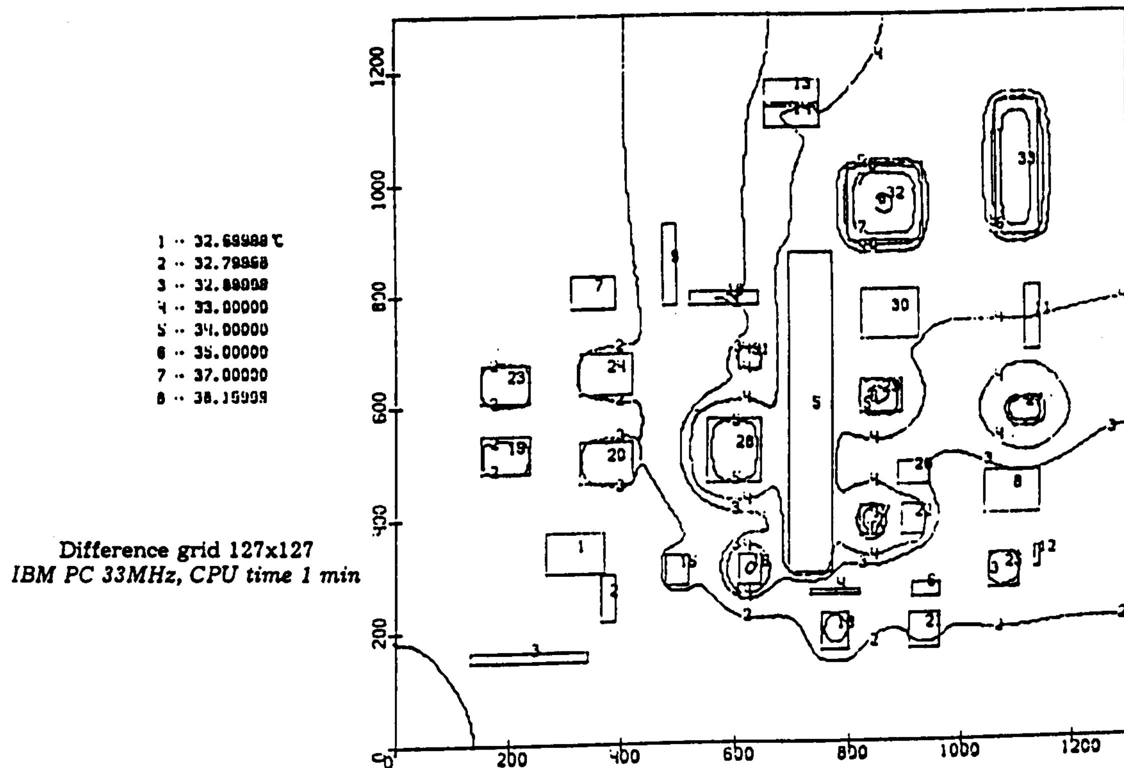


Fig. 5 2D-thermal distribution over the substrate surface of OpAmp 153UD6 chip.

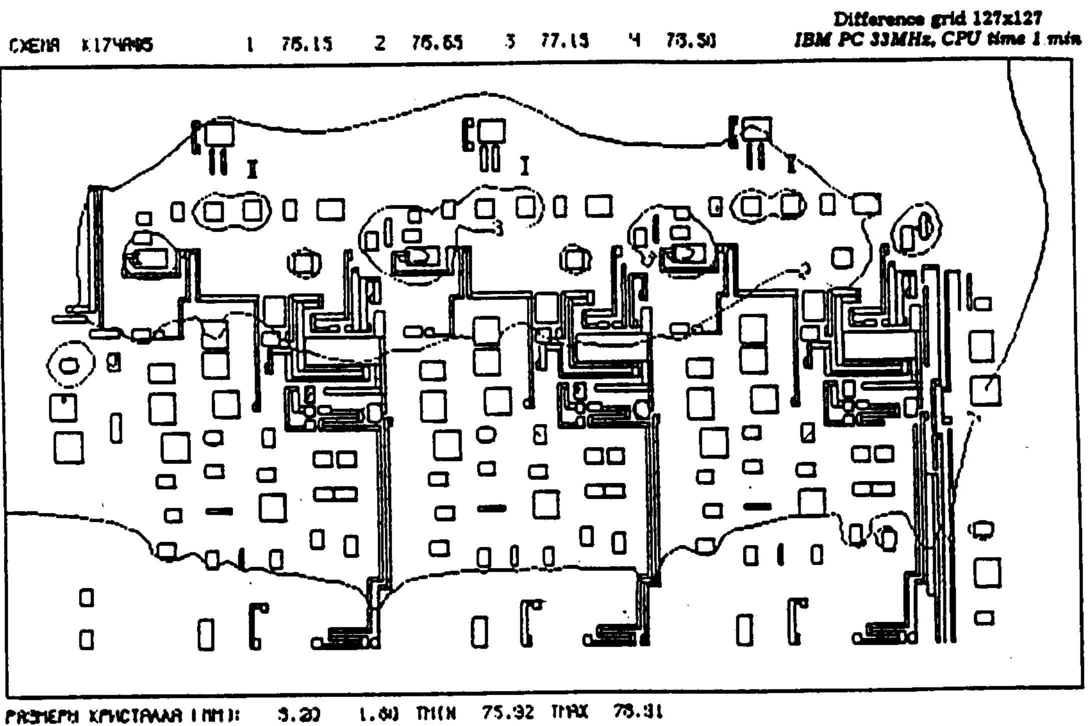


Fig. 6 Map of the temperature distribution over the substrate surface of TV-set R-G-B colour chip K174AF5.

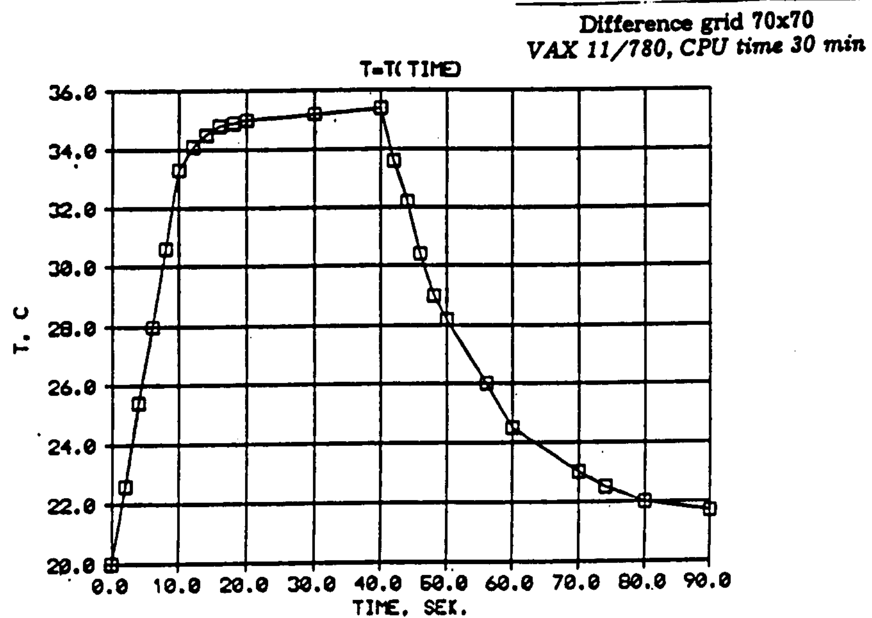
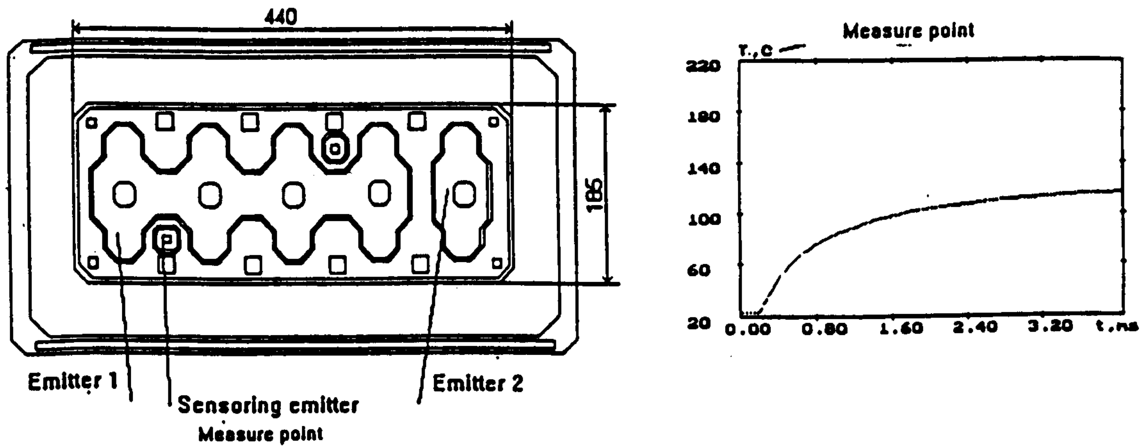


Fig. 7 Transistor T32 thermal transient response after OA153UD6 (see fig. 5) turning on at t=0 and turning off at t=40s.



Test structure of high voltage power transistor with low, middle and high current emitters formed in common base region.

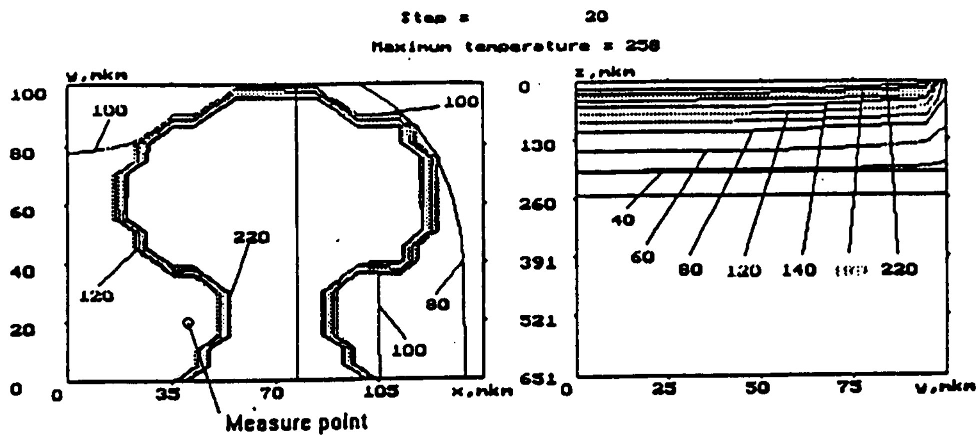


Fig. 8 The temperature rising process in the structure of sensor transistor of smart power IC after switching on.

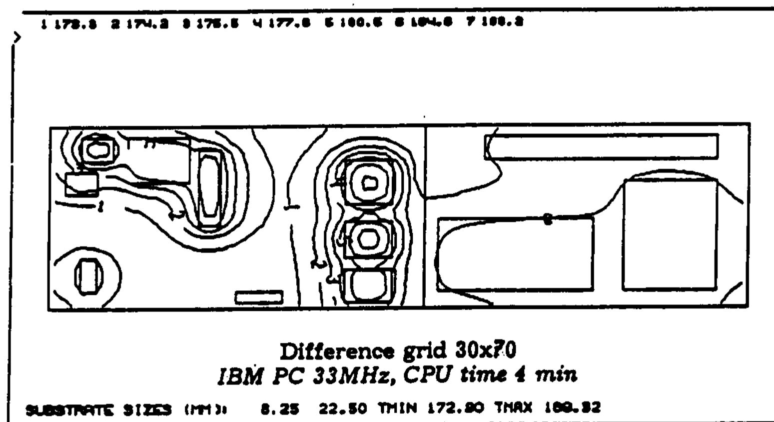


Fig. 9 Thermal modeling of hybrid IC with total power dissipation 15 W.